专 业 英 语

上

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内 容 简 介

本书针对电子类的专业特点，选编了电子学、计算机基础、数字信号处理、多媒体技术、网络技术、纳米技术、自动控制、视觉技术、电子商务、移动通讯、高清晰度电视、数字电视等方面的文章，旨在提高高年级大学生、研究生及科研人员的科技英语阅读和翻译能力。

本书共 13 个单元，每个单元由一篇正文和一篇阅读材料组成，每一篇文章都列出了生词和词组，疑难句子有注解，并配有形式新颖、适用的练习题，书后还附有部分练习答案。

本书内容新颖、难度适中，是一本非常适合于电子类专业教学和自学的专业英语书籍。

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Preface

出版电子信息类的专业英语教材，一直是许多院校多年来的共同愿望。本书根据电子信息类专业的特点，选编了大量电子技术，计算机科学技术，通信技术，控制技术，纳米技术，数字信号处理，电视技术，电子商务，光电子技术等领域的原理性和综述性文章。除了少数几篇课文专业性较强外，绝大多数课文都十分通俗易懂，便于教学。各篇课文既相互独立又有一定内在联系，可根据不同专业灵活选用。

本书的编写思想是以提高学生的阅读、翻译能力为主要目标。通过系统学习读者不仅可掌握大量的词汇和科技专用术语以及分析复杂句子结构的能力，同时还能熟练掌握动词、名词、介词的各种用法，熟悉一些常用的固定搭配，也能提高读者的科技英语写作能力。

全书分为上下两册，每个单元由一篇正文和一篇阅读材料组成。每一篇文章都列有生词，词组和注释，并配有相应的练习，书后附有部分练习答案。

本书上册由昆明理工大学理学院的樊则宾主编，下册由西北第二民族学院信息与自动化学院的杨德仁主编。其中第5，7，10单元由昆明理工大学理学院的张远弟编写，第3，4单元由西北第二民族学院的杨德仁编写，第1，2，6，8，9，11单元由樊则宾执笔，第12，13单元由昆明理工大学理学院的张萍编写。

本教材涉及面较广，对一些新的术语在注解上难免有不妥之处，恳请读者批评指正。

编 者

2003.8

Unit 01

DC Biasing — BJTs

01.1 Introduction

The analysis or design of a transistor amplifier requires knowledge of both the *dc* and the *ac* response of the system. Too often it is assumed that the transistor is a magical device that can raise the level of the applied *ac* input without the assistance of an external energy source. In actuality, the improved output *ac* power level is the result of a transfer of energy from the applied *dc* supplies. The analysis or design of any electronic amplifier, therefore, has two components: the *dc* portion and the *ac* portion. *Fortunately, the superposition theorem is applicable and the investigation of the dc conditions can be totally separated from the ac response.* However, one must keep in mind that during the design or synthesis stage the choice of parameters for the required *dc* levels will affect the ac response, and the vice versa.

The *dc* level of operation of a transistor is controlled by a number of factors, including the range of possible operating points on the device characteristics. In Section 4.2 we specify the range for the BJT amplifier. Once the desired *dc* current and voltage levels have been defined, a number of these networks must be constructed that will establish the desired operating point—a number of these networks are analyzed in this chapter. Each design will also determine the stability of the system. *That is, how sensitive the system is to temperature variations—another topic to be investigated in a later section of this chapter.*

Although a number of networks are analyzed in this chapter, *there is an underlying similarity among the analysis of each configuration due to the recurring use of the following important basic relationships for a transistor*:

$$V_{BE} = 0.7\ \text{V} \tag{1.1}$$

$$I_C = \beta I_B \tag{1.2}$$

$$I_E = (1+\beta) I_B \tag{1.3}$$

In fact, once the analysis of the first few networks is clearly understood, the path toward the

solution of the networks to follow will begin to become quite apparent. In most instances the base current I_B is the first quantity to be determined. Once I_B is known the relationships of Eqs. (1.1) can be applied to find the remaining quantities of interest. The similarities in analysis will be immediately obvious as we progress through the chapter. The equations for I_B are so similar for a number of configurations that one equation can be derived from another simply by dropping or adding a term or two. *The primary function of this chapter is to develop a level of familiarity with BJT transistor that would permit a dc analysis of a system that might employ the BJT amplifier*.

01.2 Operating Point

The term *biasing* appearing in the title of this chapter is an all-inclusive term for the application of *dc* voltage to establish a fixed level of current *dc* voltage. For transistor amplifiers the resulting *dc* current and voltage establish an *operating point* on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is a fixed point on the characteristics it is also called the *quiescent point* (abbreviated Q-point). By definition, *quiescent* means quite, still, inactive. *Figure* 1.1 *shows a general output device characteristics with four operating points indicated*. The biasing circuit can be designed to set the device operation at any of these points or others within the *active region*. The maximum ratings are indicated on the characteristics of Fig. 1.1 by a horizontal line for the maximum collector current I_{Cmax} and a vertical line at the maximum collector-to-emitter voltage V_{CEmax}. The maximum power constraint is defined by the curve P_{Cmax} in the same figure. At the lower end of the scales are the *cutoff* region, defined by $I_B \leqslant 0\ \mu A$, and the *saturation region*, defined by $V_{CE} \leqslant V_{CEsat}$.

The BJT device could be biased to operate outside these maximum limits, but the result of such operation would be either a considerable shortening of the lifetime of the device or destruction of the device. Confining ourselves to the *active region* one can select many different operating areas or points. The chosen Q pt often depends on the intended use of the circuit. Still, we can consider some differences between the various points shown in Fig. 1 to present some basic ideas about the operating point and thereby, the bias circuit.

If no bias were used, the device would initially be completely of, resulting in a *Q* pt at A—namely, zero current through the device (and zero voltage across it). Since it is necessary to bias a device so that it can respond to the entire range of an input signal point A would not be suitable. *For point B if a signal is applied to the circuit, the device will vary in current and voltage from operating point, allowing the device to react to (and possibly amplify) both the positive and negative excursions of the input signal*. If, the input signal is properly chosen, the voltage and current of the device will vary but not enough to drive the device into *cutoff* or *saturation*. Point *C* would allow some positive and negative variation of

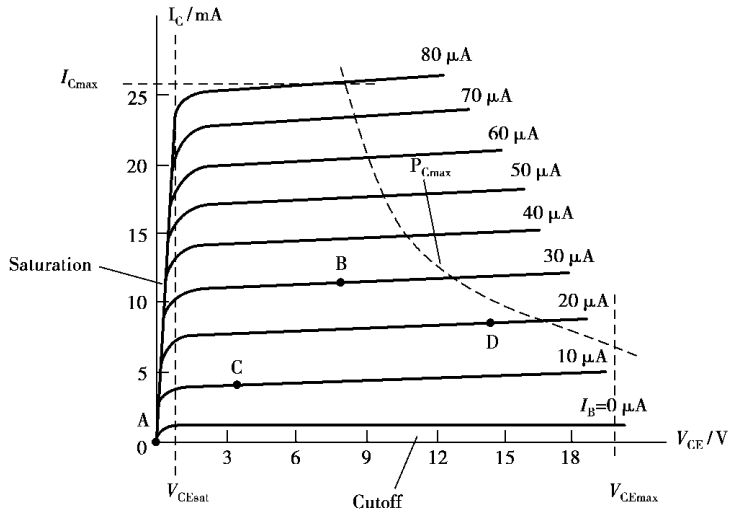


Figure 1.1 Various operating points within the limits of operation of a transistor

the output signal but the peak-to-peak value would be limited by the proximity of $V_{CE}=0$ V/ $I_C=0$ mA. Operating at point *C* also raises some concern about the nonlinearities introduced by the fact that the spacing between I_B curves is rapidly changing in this region. In general, it is preferable to operate where the gain of the device is fairy constant (or linear) to insure that the amplification over the entire swing of input signal is the same. Point *B* is a region of more linear spacing and, therefore, more linear operation, as shown in Fig. 1.1. Point *D* sets the device operating point near the maximum voltage and power lever. The output voltage swing in the positive direction is thus limited if the maximum voltage is not to be exceeded. Point *B*, therefore, seems the best operating point in terms of linear gain and largest possible voltage and current swing. This is usually the desired condition for small-signal amplifiers but not the case necessarily for power amplifiers, which will be considered in Chapter 16. In this discussion, we will be concentrating primarily on biasing the transistor for *small-signal* amplification operation.

One other very important biasing factor must be considered. Having selected and biased the BJT at a desired operating point, the effect of temperature must also be taken into account. Temperature causes the device parameters such as the transistor current gain (β_{ac}) and the transistor leakage current (I_{CEO}) to change. *Higher temperatures result in increased leakage currents in the device, thereby changing the operating condition set by the biasing network*. The result is that the network design must also provide a degree of temperature stability so that temperature changes result in minimum changes in the operating point. This maintenance of operating point can be specified by a stability factor, s, which indicates the degree of change in operating point due to a temperature variation. A highly stable circuit is desirable and the stability of a few basic bias circuits will be compared.

For the BJT to be biased in its linear or active operating point region the following must be true:

1. The base-emitter junction *must be forward-biased* (*p*-region voltage more positive) with a resulting forward-bias voltage of about 0.6 to 0.7 V (Si transistor).
2. The base-collector junction *must* be *reverse-biased* (*n*-region more positive), with the reverse-bias voltage being any value within the maximum limits of the device.

Note that for forward bias the voltage across the p-n junction is p-positive, while for reverse bias it is opposite (reverse) with n-positive, this emphasis on the initial letter should provide a means of helping memorize the necessary voltage polarity.

Operation in the cutoff, saturation, and linear regions of the BJT characteristic are provided as follows:

1. *Linear-region operation*:
   Base-emitter junction forward biased
   Base-collector junction reverse biased
2. *Cutoff-region operation*:
   Base-emitter junction reverse biased
3. *Saturation-region operation*:
   Base-emitter junction forward biased
   Base-collector junction forward biased

Selected from: Robert Boylestad, Louis Nashelsky, "Electronic Devices & Circuit Theory", Fifth Edition, 1992, Prentice-Hall, Inc.

Words and Phrases

1. BJT	**双极型晶体管**
2. transistor *n.*	**晶体管**
3. *dc* and *ac* response of the system	**系统的直流和交流响应**
4. assistance *n.*	**辅助**
5. superposition theorem	**叠加原理**
6. keep in mind	**记在心里**
7. synthesis stage	**综合阶段**
8. vice versa	**反之亦然**
9. operating point	**工作点**
10. underlying (underlie)**的现在分词** *a.*	**根本的,基础的**
11. configuration *n.*	**组态,结构**
12. recur (recurred; recurring) *vi.*	**重复,重现,再发生**
13. derive *vt.*	**推导, 推出**
14. all-inclusive term	**广义术语**
15. quiescent point	**静态工作点**

16. maximum ratings 最大额定值
17. abbreviate *vt.* 缩写
18. constraint *n.* 限制,约束
19. cutoff region 截止区
20. saturation region 饱和区
21. current gain 电流增益(放大倍数)
22. leakage current 漏电流
23. swing *v. n. a.* 摆动 旋转的
24. maintenance *n.* 保持, 维持
25. initially *ad.* 初始, 一开始
26. excursion *n.* 偏离,偏差,幅度
27. proximity *a.* 最接近的,近似的
28. forward-biased *a.* 正偏(置)
29. reverse-biased *a.* 反偏(置)

Notes

1. *Fortunately, the superposition theorem is applicable and the investigation of the dc conditions can be totally separated from the ac response.*
   所幸的是,可用叠加原理来进行分析,而且可将直流响应和交流响应分开来研究。
2. *That is, how sensitive the system is to temperature variations — another topic to be investigated in a later section of this chapter.*
   即,系统对温度变化的灵敏度有多大——在这一章的后部分的另一个主题。
3. *... there is an underlying similarity between the analysis of each configuration due to the recurring use of the following important basic relationships for a transistor.*
   因为一再用到下面的晶体管的这些重要关系,因此在分析每种组态时都有一种最基本的相似性。
4. *In fact, once the analysis of the first few networks is clearly understood, the path toward the solution of the networks to follow will begin to become quite apparent.*
   事实上,一旦对最初的几个网络的分析有了清晰的理解,那么分析随后的网络的思路就会变得十分简单明了。networks to follow **指的是随后的网络,**path **意译为思路。**
5. *The primary function of this chapter is to develop a level of familiarity with BJT transistor that would permit a dc analysis of system that might employ the BJT amplifier.*
   本章的要旨是建立大家起对晶体管的一定的了解,进而能够对用到晶体管进行放大的系统进行直流分析。注意 that **引导的两个定语从句的用法。**
6. *Figure 1.1 shows a general output device characteristics with four operating points indicated.*

图 1.1 给出了一个标有四个工作点的普通器件输出特性.

7. *For point B if a signal is applied to the circuit, the device will vary in current and voltage from operating point, allowing the device to react to (and possibly amplify) both the positive and negative excursions of the input signal.*

对工作点 B, 如果电路加入输入信号,器件的电流和电压就要从工作点变化,这就允许器件能跟着输入信号的正、负幅度作相应的变化(可能放大)。

8. *Higher temperatures result in increased leakage currents in the device, thereby changing the operating condition set by the biasing network.*

较高的温度会导致器件漏电流的增大,从而改变偏置网络设定的工作条件。

Exercises

1. Fill in the blanks with words taken from the text above, then translate the sentences into Chinese:

(1) The *dc* level of operation of a transistor is _____ by a number of factors, including the range of possible operating points _____ the device characteristics.

(2) Although a number of networks are analyzed in this chapter, there is an underlying similarity _____ the analysis of each configuration _____ to the recurring use of the following important basic relationships _____ a transistor.

(3) Once I_B is known the relationships of Eqs. (1.1) can be _____ to find the _____ quantities of interest.

(4) One other very important biasing factor must be considered. Having selected and biased the BJT _____ a desired operating point, the effect of temperature must also be taken into _____.

(5) The BJT device _____ biased to operate outside these maximum limits, but the result of such operation _____ either a considerable _____ of the lifetime of the device _____ destruction of the device.

2. Answer the questions according to the text in English as short as possible

(1) What is called the *quiescent point*?

(2) For the BJT to be biased in its linear or active operating point region what conditions should be satisfied?

3. Translate the following terms into English:

(1)晶体三极管	(2)三极管的特性曲线	(3)信号放大	(4)线性区
(5)截止区	(6)饱和区	(7)三极管的静态工作点	(8)发射结正偏
(9)集电结反偏	(10)直流响应	(11)交流响应	(12)最大额定值

Reading Supplements

DC Biasing — BJTs

1. Transistor Saturation

The term saturation is applied to any system where levels have reached their maximum values. A saturated sponge is one that cannot hold another drop of liquid. For a transistor operating in the saturation region the current is a maximum value for the particular design. *Change the design and the corresponding saturation level may rise or drop. Of course, the highest saturation level is defined by the maximum collector current as provided by the specification sheet.*

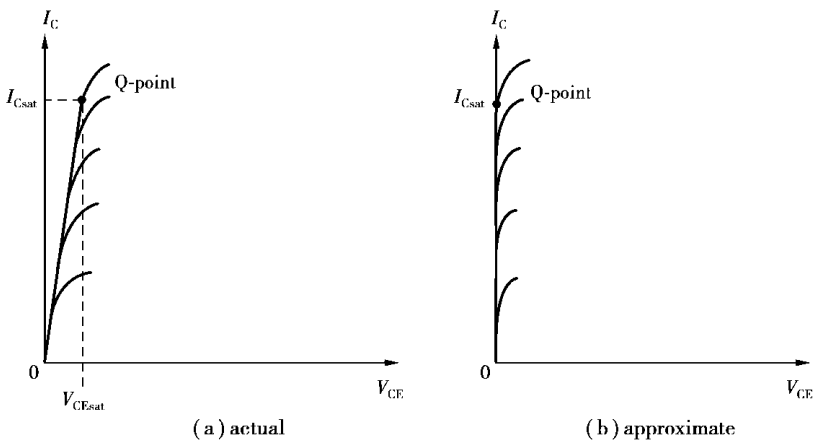


Figure 1.2 Saturation region

Saturation conditions are normally avoided because the base-collector junction is no longer reverse-biased and the output-amplified signal will be distorted. An operating point in the saturation region is depicted in Fig. 1.2(a). Note that it is a region where the characteristic curves join and the collector-to-emitter voltage is at or below V_{CEsat}. In addition, the collector current is relatively high on the characteristics.

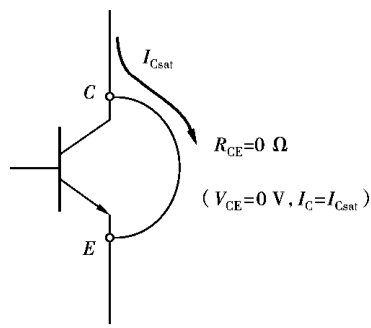


Figure 1.3 Determining I_{Csat}

If we approximate the curves of Fig. 1.2(a) *by those appearing in Fig.* 1.2(b), *a quick direct method for determining the saturation level becomes apparent.* In Fig. 1.2(b) the current is relatively high and the voltage V_{CE} is assumed to be zero volts. Applying Ohm's law the resistance between collector and emitter terminals can be determined as follows:

$$R_{CE} = \frac{V_{CE}}{I_C} = \frac{0\ V}{I_{Csat}} = 0\ \Omega \tag{1.4}$$

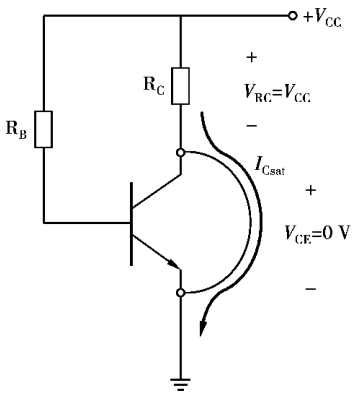


Figure 1.4 Determining I_{Csat} for the fixed-bias configuration

Applying the results to the network schematic would result in the configuration of Fig. 1.3.

For the future, therefore, if there were an immediate need to know the approximate maximum collector current (saturation level) for a particular design, simply insert a short-circuit equivalent between collector and emitter of the transistor and calculate the resulting collector current. In short, set $V_{CE}=0$ V. *For the fixed-bias configuration of Fig. 1.4 the short circuit has been applied, causing the voltage across R_C to be the applied voltage V_{CC}.* The resulting saturation current for the fixed-bias configuration:

$$I_{Csat}=\frac{V_{CC}}{R_C} \tag{1.5}$$

Once I_{Csat} is known we have some idea of the maximum possible collector current for the chosen design and the level to stay below if we expect linear amplification.

Selected from: Robert Boylestad, Louis Nashelsky, "Electronic Devices & Circuit Theory", Fifth Edition, 1992, Prentice-Hall, Inc.

Words and Phrases

1. depict *vt.* **描绘**
2. schematic *a. n.* **图解的,示意的;简图,原理图**
3. short circuit *n.* **短路**
4. fixed-bias *n.* **固定偏置**

Notes

1. *The term saturation is applied to any system where levels have reached their maximum values.*
   饱和这一术语用来描述系统达到最大值的程度。
2. *Saturation conditions are normally avoided because the base-collector junction is no longer reverse-biased and the output-amplified signal will be distorted.*
   通常要避免饱和条件,因为集电结不再处于反偏状态,输出放大信号会失真。
3. *Change the design and the corresponding saturation level may rise or drop. Of course, the highest saturation level is defined by the maximum collector current as provided by*

the specification sheet.

改变设计相应的饱和程度会上升或下降。当然最大的饱和程度是由特定的图表定义的最大集电极电流决定的。Level **译为程度，**specification sheet **指特定的图表。**

4. *If we approximate the curves of Fig. 1.2(a) by those appearing in Fig. 1.2(b), a quick direct method for determining the saturation level becomes apparent.*

   如果我们将图 1.2(a)**用图** 1.2(b)**来近似，那么显然就有了一种快速确定饱和程度的方法.**

5. *For the fixed-bias configuration of Fig. 1.4 the short circuit has been applied, causing the voltage across R_C to be the applied voltage V_{CC}.*

   对于如图 1.4 **所示的固定偏置电路结构，单电流取短路电流时，**R_C **上的电压降就等于所加电源电压** V_{CC}。

Exercises

1. Fill in the blanks with words taken from the text above, then translate the sentences into Chinese.

(1) A saturated sponge is _____ that cannot _____ another drop of liquid.

(2) Saturation conditions are normally avoided _____ the base-collector junction is no longer reverse-biased and the output-amplified signal will be _____.

(3) Once I_{Csat} is known we have some idea of the maximum possible collector current for the chosen design and the level to _____ below if we _____ linear amplification.

(4) Note that it is a region _____ the characteristic curves join and the collector-to-emitter voltage is _____ or below V_{CEsat}. In addition, the collector current is relatively high _____ the characteristics.

2. Translate the following terms into English:

(1)**饱和程度** (2)**集电结** (3)**信号失真** (4)**短路**

(5)**最大集电极电流** (6)**欧姆定理** (7)R_C **上的电压降** (8)**线性放大区**

Unit 02

555 Timers：Basics

02.1 Introduction

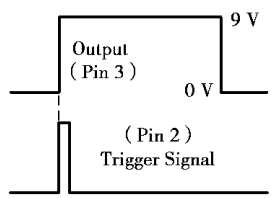
HERE IS THE PINOUT OF A 555 CHIP:
(Note: A 7555 is the CMOS version of the 555 and uses a fraction of the 555's power. Pinouts are the same.)

MULTIVIBRATOR

555s are configured as a multivibrator by adding a few components to the pins. *This is a circuit that oscillates from one state to another over time, in this case, creating a square wave. There are two basic forms of timers, both being multivibrators.*

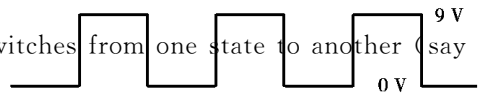
Monostable Multivibrator:

A monostable multivibrator circuit has an output that stays in a given state (say +9 V) until a separate signal triggers the timer. The state of the output is then shifted to 0 V and will remain in that state until a pre-determined time is reached. The output then goes back to +9 Vs, waiting for a new trigger signal to come in. See the figure to the left for a graphical representation of this. This circuit is also called a ONE-SHOT or PULSE-STRETCHER.



The timer the output changes states for is determined by a Resistor/Capacitor combination that will be described in the Monostable section of this site.

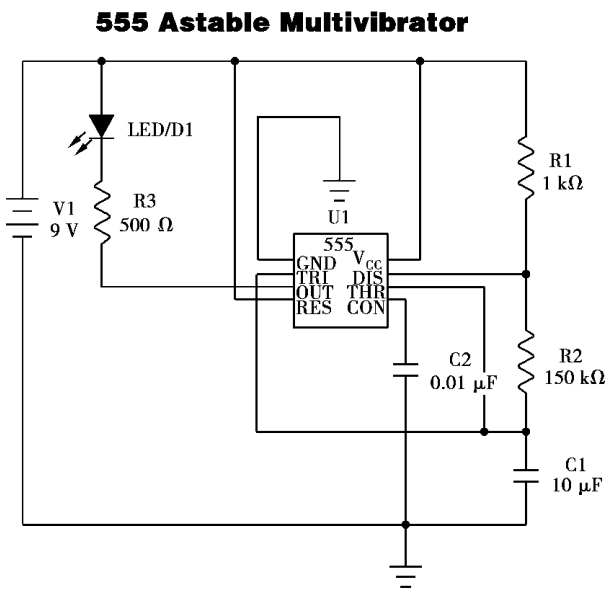
Astable Multivibrator:



An astable multivibrator spontaneously switches from one state to another (say +9 V to 0 V to +9 V...). The time it stays high and the time it stays low are determined by the values of the external components. This will be described in the astable section of this site.

02.2 555 Timers: Astable

A 555 set in the astable mode is basically an oscillator. It changes states by itself according to the support components you choose. On(high) then Off (low) then On then off... See the schematic below. The LED will turn on for approximately one second and off for one second then on... You can download the EWB version of this circuit to run the simulation or the PCB Gif to make a PCB board. I usually just build them on a breadboard myself.



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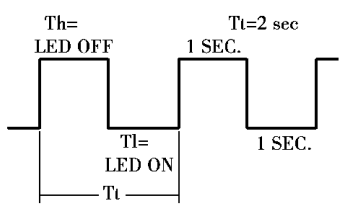
Note: The old version of this circuit was inefficient for certain applications. Please use this newer version in your projects. The LED lights with a low signal from the output pin now and the 1 Ω resistor is replaced with a common 1 KΩ version. Schematic By John Adams: Feel free to use in class or for projects.

Description of Circuit:

This circuit requires very few external components. The main three are R1, R2 and C1. C2 is merely there to prevent instability problems. R3 limits current to the LED. A 9 V battery is shown but you can use anything from 4.5 to 12 Volts. I use either a 9 V Battery or an adaptor set to 6 V. If you want to interface the oscillator to a TTL circuit you must match that voltage, typically +5 V.

Use a 150 K and 1,000 Ω resistor in this newer circuit. The timing is nearly the same as the one that was previously posted.



NOTE: If the LED is not bright enough, use a smaller value resistor in place of R3.

The TIME HIGH (LED OFF) and TIME LOW (LED ON) are determined by R1, R2 and C1. Let's call the TIME HIGH Th and the TIME LOW Tl. The total time is Tt. The formula to solve Th is:

$$Th = 0.693 \times C1 \times (R1 + R2)$$

In our circuit above R1 is 1,000 Ω (1 K), R2 is 150,000 Ω (150 K) and the Capacitor is .000,01 Farads (10 microfarads). Let's solve for Th.

$$Th = .693 \times .000,01 \times (1,000 + 150,000)$$

$$Th = .693 \times .000,01 \times 151,000$$

$$Th = 1.042 \text{ Seconds}$$

Now to figure out the Time low, we use the same formula ignoring R1.

$$Tl = 0.693 \times C1 \times R2$$

$$Tl = .693 \times .000,01 \times 150,000$$

$$Tl = 1.035 \text{ seconds}$$

All that left to figure out is Time Total. Just add the Tl and Th.

$$Tt = Th + Tl$$

$$Tt = 2.077 \text{ seconds}$$

If you want to convert this to frequency instead of time:

$$F = 1/Tt$$

F=.5 Hertz (Hz) or cycles per second.

You may ask why I used such a small resistor for R1. Doing this gives nearly the same time on as off. The ratio of time ON to total time is called Duty Cycle. The example circuit we made has a duty cycle of 1:2 or 50 % (50 % on and 50 % off) The reason the 1 K resistor is used instead of a 1 Ohm unit is because the 1 Ohm was causing a high current situation. The 1 K will produce almost the same results and not fry a low power 555. To see how you would make a circuit with a longer time high (LED OFF) and shorter time low (LED ON), work out this example:

C1=10 microfarad (.000,01 Farad)

R1=150 K

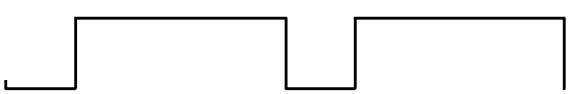
R2=47 K

$Th = .693 \times .000,01 \times 197,000$

Th=1.365 seconds.

$Tl = .693 \times .000,01 \times 47,000$

Tl=.33 seconds



This produces a circuit with the LED on for .33 seconds and off 1.4 seconds. It's duty cycle is now 3:4 or 75 %. There is a simple formula to figure out duty cycle.

Percentage of Duty Cyle=(Th divided by Tt)×100

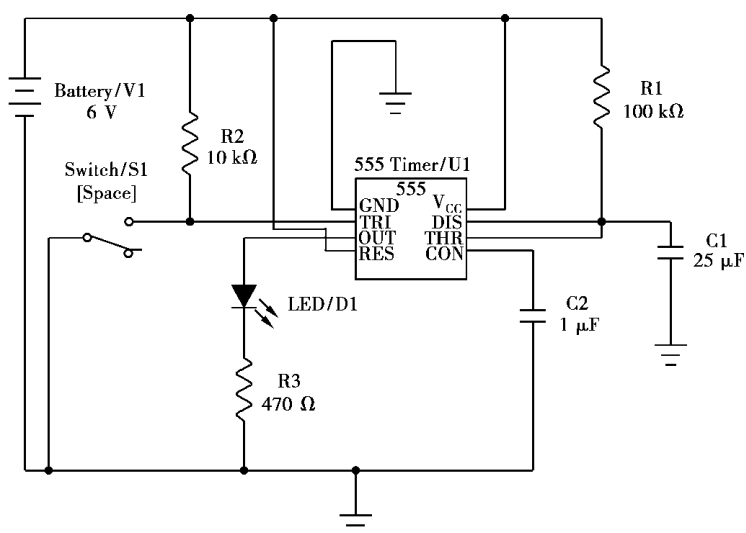
We will go more into duty cycle in later sections.

CHECK OUT THE 555 CALCULATORS TO INSTANTLY FIGURE OUT Th, Tl, Frequency and Duty Cyle.

This example created a square wave form. Using the 555 in the Astable mode you can create other wave forms as well. We will see more circuits that create triangle and others in later 555 sections. A high frequency oscillator built with a 555 can be used to power a speaker, creating a sound waves. An example would be to create an alarm speaker driver. If two 555's are chained together, many sound effects can result.

02.3 555 Timers: Monostable

Monostable multivibrators can be configured in many ways. The following is a one-shot timer hooked to an LED. When the switch is flipped on then off, a signal is sent to the trigger pin. The LED will light for 2 and 3/4 seconds before going out (timing-out). The blue line(TR1) is the trigger signal (positive 6 V to 0 V when switched) and the red line (OUT) is the output. You can download the EWB version of this circuit to run the simulation or the PCB Gif to make a PCB board. I usually just build them on a breadboard myself.



Schematic By John Adams: Feel free to use in class or for projects.

Description of Circuit:

This circuit requires very few external components. The main two are R1 and C1. C2 is merely there to prevent instability problems. R2 is used to hold the trigger high until the switch brings it to ground (low). Note that the IC wants a negative going trigger. R3 limits the current of the LED. A 6 V battery is shown but you can use anything from 4.5 to 12 Volts. I use either a 9 V Battery or an adaptor set to 6 V. If you want to interface the timer