高等学校电子信息类规划教材

科 技 英 语

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（第 二 版）
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内 容 简 介

本书内容紧密结合电子技术，使读者能够顺利地获得阅读科技资料所需的系统而又最关键的语法知识，掌握一定量的科技词汇，提高阅读技能与速度。编者根据数十年的教学经验，采用了我国理工科学生和科技人员易于接受的功能图法、试探法、对比法、公式法和归纳小结法等一系列行之有效的独特新颖的叙述方法，对读者掌握所学内容是非常有帮助的。本书既可用作为电子技术专业及相近专业大专生的教材，同时也适用于具有初步英语基础的厂、所科技人员学习、进修科技英语之用。

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前　　言

本教材系按电子工业部的《1996—2000 年全国电子信息类专业教材编审出版规划》，由全国高校大专电子技术专业教学指导委员会编审、推荐出版。本教材由西安电子科技大学秦荻辉编著，张庭季主审，责任编委郁伯康。

本教材的参考学时数为 60 学时，其主要内容分为三大部分：第一部分为预备知识及相应的练习，供自学复习用；第二部分为本书的核心语言内容，旨在向读者重点而系统地介绍为阅读和翻译电子类产品说明书和有关资料所必须掌握的科技英语的基本语法现象，本部分共设 3 个单元 17 课，每课设有两篇短文（一般都选自国外原版科技书籍而不是科普文章。凡属中学已学过的 1 600 个英语单词均未列在生词表内，但在书后的总词汇表中列出了课文中出现的所有单词），对某一语法内容的讲述以及为提高科技文阅读能力而设计的各种实用练习；第三部分为专业阅读材料，全部选自美国出版的大学教科书，内容包括电子线路、通信、计算机和彩色电视，并对许多语言难点、句型、词汇用法、翻译技巧等作了详尽的注释。

使用本教材时应注意把学习重点放在原来在基础英语学习阶段没有掌握好或没有提及的语言点上，特别要求读者能读懂每篇课文，能独立精心地完成各种练习题（书后给出了课文的参考译文和部分练习题的参考答案，供读者作为自我检查之用，而绝不应先看了参考译文和答案后再进行学习，否则会大大影响学习效果），并应努力学习（主要在课后）本书第三部分的专业阅读材料，没有一定的阅读量是很难掌握好阅读技能的，也是学不好英语的。

由于编者水平有限，书中难免还存在一些缺点和错误，殷切希望广大读者批评指正。

编　者

1998 年 7 月

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Chapter 1

TRANSISTOR AMPLIFIERS

The advent of electronics is reckoned from the discovery that[1] *the current in a vacuum diode can be controlled by introducing a third*[2] *electrode, which makes the triode an exceedingly effective amplifier.* *The possibilities inherent in electronic circuits*[3] *were greatly expanded by the invention of the transistor in* 1948. *Since then a wide variety of semiconductor devices has to a large extent*[4] *supplanted vacuum tubes in most applications.*

Both vacuum tubes, which are discussed in Appendix A, and transistors are nonlinear devices, and their operation in any circuit is determined by graphical analysis using the description of[5] *their electrical properties given by current-voltage characteristics.* *The analysis differs in detail for voltage-controlled devices such as the triode and field-effect transistor compared to*[6] *current-controlled devices such as the junction transistor, but is not different in principle.* *Furthermore, in either case it proves possible to develop useful equivalent-circuit representations which are most satisfactory for circuit analysis.*

1－1　THE OPERATING POINT

1－1.1　Load Lines

The operation of a FET[7] as an amplifier is examined most easily with the aid of the elementary amplifier circuit employing a p6channel FET shown in Fig. 1 - 1. In this circuit the drain is maintained at a negative potential with respect to the source by the battery V_{dd} while[8] the gate is *biased* positively by the gate bias battery V_{gg}**d** Variations in gate voltage resulting from an input signal ΔV_{gs} produce changes in the drain current which are observed as a voltage signal ΔV_{ds} across the load resistor R_L.

Figure 1 - 1 Simple p6channel FET amplifier

The circuit is analyzed using[9] Kirchhoff's rules in the usual way except that**l** since the current6voltage properties of the FET are nonlinear, the solution must be carried out graphically**d** The voltage equation around the output circuit is

$$V_{dd} - I_d R_L + V_{ds} = 0 \qquad (1-1)$$

which may be put in the form

$$I_d = \frac{V_{dd}}{R_L} 、 \frac{\mathrm{N}}{R_L} V_{ds} \qquad (1-2)$$

Equation (1 - 2) plots as[10] a straight line on the drain characteristics of the FET and has intercepts at $I_d = 0$, $V_{ds} = V_{dd}$ and $V_{ds} = 0$, $I_d = V_{dd}$**f**R_L**d** It is**l** in fact**l** the current-voltage characteristic of R_L and is called the *load6line***d**

The load line together with the drain characteristics of the FET represent two relations in the two unknowns V_{ds} and I_d. By plotting[11] the load line on the drain characteristics as in Fig. 1 - 2, the drain current corresponding to each gate voltage is given by the intersection of the load line with[12] the characteristic curve for that gate voltage.

The *operating point* is the intersection of the load line with the characteristic curve corresponding to the gate bias voltage. As[13] the gate voltage varies in accordance with an applied input signal**l** the drain6current excursions move back and forth along the load line so that Eq. (1 - 2) is satisfied at every instant. In Fig. 1 - 2, for example, an input signal of 0. 4 V causes the drain current to change by[14] approximately 0. 6 mA and results in[15] an output signal of about 6 V. That is, the circuit amplifies the input signal by a factor of $\frac{6}{0.4} = 15$.[16]

Note that the input power is very small because the gate current is negligible. In contrast, the output power, which is equal to the product of the change in drain current times the change in drain voltage[17], may be quite appreciable. This power is derived from the drain supply battery**l** V_{dd}**l** and is controlled by the valve6like action of the gate.

Figure 1 - 2 Operating point is the intersection of load line with gate bias curve.

1 - 1.2 Source Bias

A separate gate bias battery is economically impractical in most circuits. Instead[18], gate bias can be obtained by inserting a resistor in series with the source, Fig. 1 - 3.

Figure 1 - 3 Practical n6channel FET amplifier using source bias.

The gate potential is set by a voltage divider connected to the drain voltage source**d** Then the current through the source resistor R_S results in a gate bias of the proper polarity and magnitude to maintain the gate junction under reverse bias. A useful feature of this circuit is that if, for example, a change in ambient temperature increases the drain current, the voltage drop across the source resistor increases the gate bias, which[19] tends to return the drain current to the original value. That is, the drain current and the operating point are stabilized against[20] external influences.

Note that the source resistor is shunted by a large capacitor to prevent ac signals caused by ac drain currents in the source resistor from[21] appearing in the gate circuit. Also, capacitors are included at the input and output to isolate the amplifier from[22] external dc voltages that could change the operating point.

The operating point is determined by writing the equation for the load line from[23] the dc voltage drops in the output circuit**l**

$$V_{dd} - I_d R_L - V_{ds} - I_d R_s = 0 \tag{1 - 3}$$

Since, however, the gate bias voltage is not known, in contrast to the simpler circuit previously analyzed, another relation is required. This is found from the dc voltage drops around the input circuit**l**

$$\frac{V_{dd} R_2}{R_1 + R_2} - V_{gs} - I_d R_s = 0 \tag{1 - 4}$$

Both equations may be put in the same form. The load line is, from Eq. (1 - 3),

$$I_d = \frac{V_{dd}}{R_s + R_L}, \quad \frac{\text{Ⅳ}}{R_s + R_L} V_{ds} \tag{1 - 5}$$

and the *bias line*, from Eq. (1 - 4), is

$$I_d = \frac{V_{dd} R_2}{(R_1 + R_2) R_s}, \quad \frac{\text{Ⅳ}}{R_s} V_{gs} \tag{1 - 6}$$

Note that Eq. (1 - 5) is similar to Eq. (1 - 2), and that Eq. (1 - 6) has the same form. These expressions**l** together with the current6voltage characteristics of the FET, represent three relations in the three unknowns**l** V_{ds}**l** I_d**l** and V_{gs}, and are solved graphically.

The bias line, Eq. (1 - 6), is a straight line on the transfer characteristic, Fig. 1 - 4, and the intersection gives the drain current and gate voltage immediately. The drain voltage is then found from the intersection of the gate bias curve with the load line plotted on the drain characteristics. Thus the operating point is completely determined.

An input signal applied to the gate results in corresponding changes in the drain current, as shown by the transfer characteristic in Fig. 1 - 4. As[24] in the previous circuit, drain signal currents through the load resistor produce an output signal. This is illustrated graphically in Fig. 1 - 4 by plotting the *ac load line* on the drain characteristics. The ac load line is simply the dc load line, Eq. (1 - 5), with the source resistor set equal to zero to[25] account for the shunting action of the source bypass capacitor at signal frequencies.

Note that a sinusoidal input signal results in a sinusoidal output signal of larger amplitude.

Figure 1 - 4 Intersection of bias line with transfer characteristic yields operating point of source6bias amplifier.

The output waveform is not an exact amplified replica of the input signal, however, because of curvature in the transfer characteristic. This *distortion* is minimized by proper circuit design and suitable choice of the operating point. Note also in Fig. 1 - 4 that an increase in gate voltage produces a decrease in the output voltage. This means that the circuit introduces a 180° phase shift between input and output signals.

A simpler version of the circuit in Fig. 1 - 3 eliminates resistor R_1. Quite satisfactory operation is achieved, but because the source resistor must then usually be made small to obtain the correct gate bias, the circuit is not quite so stabilized against shifts in operating point accompanying changes in[26] ambient temperature or supply potential**d** In either circuit it often proves more convenient to find the operating point by a 。cut6and6try7 process[27] rather than by resorting to[28] the graphical technique. This is done by first choosing a reasonable value for the gate bias**l** V_{gs}**l** and estimating I_d from the drain characteristics**d** This value is used to calculate V_{gs} from the bias characteristic, Eq. (1 - 6), to compare with the original estimate. If the two agree[29]**l** the operating point is determinedT if not**l** a revised estimate for V_{gs} is taken and the process repeated[30]. Usually two or three trys[31] are sufficient to attain satisfactory agreement.

It is inconvenient to measure electrode voltages with respect to the source in circuits employing source bias. This is particularly true when more than one transistor is used in a circuit. Rather[32], usual practice is to refer all potentials to a common point called *ground*. The ground point is considered to be electrically neutral so that, for example, the ground points of two separate circuits may be connected with no influence upon[33] the operation of either circuit. A typical use of the circuit symbol for the ground point in Fig. 1 - 3 is at the junction of the lower input and output terminals and the bottom end of the source resistor.

1 - 1.3 Small-Signal Parameters

Very frequently the signal amplitudes applied to an FET amplifier are small compared with the full range of voltages covered by the drain characteristics. In this situation graphical analysis of FET performance is inaccurate because the drain characteristics are not given with sufficient precision. A more satisfactory procedure is to replace the FET with an equivalent circuit which can be studied by conventional circuit analysis. After the operating point is determined graphically, small departures about[34] the operating point caused by small signals are treated by assuming that the FET is a linear device. According to the drain characteristics, drain current depends upon both the gate voltage and the drain voltage. Therefore, a small change in drain current (ΔI_d) away from the operating point may be written

$$\Delta I_d = k_1 \Delta V_{gs} + k_2 \Delta V_{ds} \tag{1 - 7}$$

where ΔV_{gs} and ΔV_{ds} are small changes in the electrode potentials and k_1 and k_2 are constants.

The ratio $\Delta I_d / \Delta V_{ds}$ can be identified as the reciprocal of an equivalent resistance called the *drain resistance*,

$$\frac{1}{r_d} = \frac{\Delta I_d}{\Delta V_{ds}} \tag{1 - 8}$$

Similarly, the ratio $\Delta I_d / \Delta V_{gs}$ gives the change in drain current resulting from a change in voltage in the gate circuit. It has the dimensions of conductance and is called the *mutual transconductance*,

$$g_m = \frac{\Delta I_d}{\Delta V_{gs}} \tag{1 - 9}$$

The total change in drain current is, from Eqs. (1 - 7), (1 - 8), and (1 - 9),

$$\Delta I_d = g_m \Delta V_{gs} + \frac{1}{r_d} \Delta V_{ds} \tag{1 - 10}$$

Consider now that the small departures about the operating point are ac signals, so that Eq. (1 - 10) becomes

$$i_d = g_m v_{gs} + \frac{1}{r_d} v_{ds} \tag{1 - 11}$$

This expression may be interpreted as the circuit equation for a current generator in parallel with a resistor, as in Fig. 1 - 5; summing the currents at the upper node yields Eq. (1 - 11) directly. Figure 1 - 5 is the *ac equivalent circuit* of the FET. Note that it has the configuration of the Norton equivalent circuit discussed in Chap. 1, which is consistant with the constant-current properties of the FET drain characteristics.

Figure 1 - 5 FET ac equivalent circuit

The mutual transconductance and the drain resistance are called the *small signal parame-*

ters of the FET. The mutual transconductance is just the slope of the transfer characteristic at the operating point, and the drain resistance is the reciprocal of the drain characteristic at the operating point. Typical values of small signal parameters given in Table 1 - 1 show that the several different types of FETs are comparable. A rather wide range of parameters may be achieved by suitable choice of the FET design, however. Actually, since the FET is a nonlinear device, the magnitudes of the small signal parameters depend upon the dc drain current as well, Fig. 1 - 6. For this reason**l** it is usually necessary to evaluate g_m and r_d graphically at the operating point. According to Fig. 1 - 6 quite appreciable variations in the small signal parameters can be obtained by selecting the operating point. This is important in the design of FET circuits having specific performance requirements.

Table 1 - 1 FET small signal parameters

Type		g_m, 10^{-6} mho	r_d, *
2C5484	n6channel FET	2000	50,000
2C5268	p6channel FET	1700	15,000
2C3797	n6channel MOSFET (depletion)	2300	40,000
3C157	p6channel MOSFET (enhancement)	2000	17,000

Figure 1 - 6 Variation of small6signal parameters of type 2C5268]6channel FET with drain current.

It is illustrative to analyze the simple FET amplifier in Fig. 1 - 3 by means of the ac equivalent circuit technique. According to Fig. 1 - 5, the equivalent circuit of the amplifier is obtained by replacing the FET with a constant6current generator in parallel with a resistor, Fig. 1 - 7**e**. Note that the gate terminal is not connected to the remainder of the equivalent circuit**d** This is a consequence of the very high input resistance of the reverse6biased gate junction. This circuit ignores the capacitance of the gate junction, however, and is only accurate at frequencies low enough that[36] its capacitive reactance can be neglected. This matter is treated more extensively in Chap. 7.

Figure 1 - 7 (**e**) ac equivalent circuit of FET amplifier in Fig. 1 - 3, and bW simplified version assuming capacitive reactances are negligible.

Similarly, it is usually assumed that the capacitive reactances of the coupling capacitors and the source bypass capacitor are negligible at signal frequencies of interest[37]. This leads to the simpler equivalent circuit shown in Fig. 1 - 7W In spite of these approximations, the circuit in Fig. 1 - 7*b* proves to be a useful representation of the actual amplifier for many purposes.

The output signal may be written down immediately as[38] the voltage drop across the parallel combination of the load resistance and the drain resistance**l**

$$v_o = -g_m v_{gs} \frac{r_d R_L}{r_d + R_L} \qquad (1-12)$$

The ratio of the output signal to the input signal[39] is called the *gain* of the amplifier. Since the gate voltage is equal to the input signal, the gain is