

数字设计和 计算机体系结构

[美] 莎拉 L. 哈里斯 戴维·莫尼·哈里斯 著
(Sarah L. Harris) (David Money Harris)

Digital Design and Computer Architecture

ARM® Edition

(英文版 · 第2版 · ARM版)



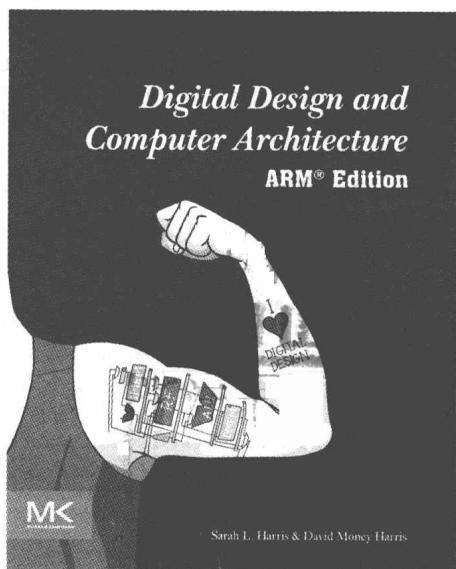
*Digital Design and
Computer Architecture (ARM Edition)*

经典原版书库

数字设计和 计算机体系结构

(英文版·第2版·ARM)

*Digital Design and
Computer Architecture* (ARM Edition)



[美] 莎拉 L. 哈里斯 戴维·莫尼·哈里斯 著
(Sarah L. Harris & David Money Harris)

机械工业出版社
China Machine Press

图书在版编目 (CIP) 数据

数字设计和计算机体系结构 (英文版·第2版·ARM版) / (美) 莎拉 L. 哈里斯 (Sarah L. Harris), (美) 戴维·莫尼·哈里斯 (David Money Harris) 著. —北京: 机械工业出版社, 2018.1 (经典原版书库)

书名原文: Digital Design and Computer Architecture, ARM Edition

ISBN 978-7-111-58679-1

I. 数… II. ①莎… ②戴… III. ①数字电路 - 电路设计 - 英文 ②计算机体系结构 - 英文
IV. ① TN79 ② TP303

中国版本图书馆 CIP 数据核字 (2017) 第 309488 号

本书版权登记号: 图字 01-2017-7110

Elsevier (Singapore) Pte Ltd.
3 Killiney Road, #08-01 Winsland House I, Singapore 239519
Tel: (65) 6349-0200; Fax: (65) 6733-1817

Digital Design and Computer Architecture, ARM Edition
Sarah L. Harris, David Money Harris
Copyright © 2016 Elsevier Inc. All rights reserved.
Materials Provided by ARM are copyright © ARM Limited (or its affiliates).
ISBN-13: 978-0-12-800056-4

This reprint of Digital Design and Computer Architecture, ARM Edition by Sarah L. Harris, David Money Harris was undertaken by China Machine Press and is published by arrangement with Elsevier (Singapore) Pte Ltd.

Digital Design and Computer Architecture, ARM Edition by Sarah L. Harris, David Money Harris 由机械工业出版社进行影印, 并根据机械工业出版社与爱思唯尔 (新加坡) 私人有限公司的协议约定出版。

ISBN: 978-7-111-58679-1

Copyright © 2018 by Elsevier (Singapore) Pte Ltd.

All rights reserved. No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying, recording, or any information storage and retrieval system, without permission in writing from Elsevier (Singapore) Pte Ltd. Details on how to seek permission, further information about the Elsevier's permissions policies and arrangements with organizations such as the Copyright Clearance Center and the Copyright Licensing Agency, can be found at our website: www.elsevier.com/permissions.

This book and the individual contributions contained in it are protected under copyright by Elsevier (Singapore) Pte Ltd. and China Machine Press (other than as may be noted herein).

Online resources are not available with this reprint.

Notice

Practitioners and researchers must always rely on their own experience and knowledge in evaluating and using any information, methods, compounds or experiments described herein. Because of rapid advances in the medical sciences, in particular, independent verification of diagnoses and drug dosages should be made. To the fullest extent of the law, no responsibility is assumed by Elsevier, authors, editors or contributors in relation to the adaptation or for any injury and/or damage to persons or property as a matter of products liability, negligence or otherwise, or from any use or operation of any methods, products, instructions, or ideas contained in the material herein.

Printed in China by China Machine Press under special arrangement with Elsevier (Singapore) Pte Ltd. This edition is authorized for sale in the People's Republic of China only, excluding Hong Kong SAR, Macau SAR and Taiwan. Unauthorized export of this edition is a violation of the contract.

本书英文影印版由 Elsevier (Singapore) Pte Ltd. 授权机械工业出版社在中华人民共和国境内 (不包括香港、澳门特别行政区及台湾地区) 出版与发。未经许可之出口, 视为违反著作权法, 将受民事和刑事法之制裁。

本书封底贴有 Elsevier 防伪标签, 无标签者得销售。

出版发行: 机械工业出版社 (北京市西城区百万庄大街 22 号 邮政编码: 100037)

责任编辑: 曲 熠

责任校对: 殷 虹

印 刷: 北京兆成印刷有限公司

版 次: 2018 年 1 月第 1 版第 1 次印刷

开 本: 186mm × 240mm 1/16

印 张: 36.5

书 号: ISBN 978-7-111-58679-1

定 价: 129.00 元

凡购本书, 如有缺页、倒页、脱页, 由本社发行部调换

客服热线: (010) 88378991 88361066

投稿热线: (010) 88379604

购书热线: (010) 68326294 88379649 68995259

读者信箱: hzsj@hzbook.com

版权所有·侵权必究

封底无防伪标均为盗版

本书法律顾问: 北京大成律师事务所 韩光 / 邹晓东

出版者的话

文艺复兴以来，源远流长的科学精神和逐步形成的学术规范，使西方国家在自然科学的各个领域取得了垄断性的优势；也正是这样的优势，使美国在信息技术发展的六十多年间名家辈出、独领风骚。在商业化的进程中，美国的产业界与教育界越来越紧密地结合，计算机学科中的许多泰山北斗同时身处科研和教学的最前线，由此而产生的经典科学著作，不仅擘划了研究的范畴，还揭示了学术的源变，既遵循学术规范，又自有学者个性，其价值并不会因年月的流逝而减退。

近年，在全球信息化大潮的推动下，我国的计算机产业发展迅猛，对专业人才的需求日益迫切。这对计算机教育界和出版界都既是机遇，也是挑战；而专业教材的建设在教育战略上显得举足轻重。在我国信息技术发展时间较短的现状下，美国等发达国家在其计算机科学发展的几十年间积淀和发展的经典教材仍有许多值得借鉴之处。因此，引进一批国外优秀计算机教材将对我国计算机教育事业的发展起到积极的推动作用，也是与世界接轨、建设真正的世界一流大学的必由之路。

机械工业出版社华章公司较早意识到“出版要为教育服务”。自1998年开始，我们就将工作重点放在了遴选、移译国外优秀教材上。经过多年的不懈努力，我们与 Pearson, McGraw-Hill, Elsevier, MIT, John Wiley & Sons, Cengage 等世界著名出版公司建立了良好的合作关系，从他们现有的数百种教材中甄选出 Andrew S. Tanenbaum, Bjarne Stroustrup, Brian W. Kernighan, Dennis Ritchie, Jim Gray, Alfred V. Aho, John E. Hopcroft, Jeffrey D. Ullman, Abraham Silberschatz, William Stallings, Donald E. Knuth, John L. Hennessy, Larry L. Peterson 等大师名家的一批经典作品，以“计算机科学丛书”为总称出版，供读者学习、研究及珍藏。大理石纹理的封面，也正体现了这套丛书的品位和格调。

“计算机科学丛书”的出版工作得到了国内外学者的鼎力相助，国内的专家不仅提供了中肯的选题指导，还不辞劳苦地担任了翻译和审校的工作；而原书的作者也相当关注其作品在中国的传播，有的还专门为其书的中译本作序。迄今，“计算机科学丛书”已经出版了近百个品种，这些书籍在读者中树立了良好的口碑，并被许多高校采用为正式教材和参考书籍。其影印版“经典原版书库”作为姊妹篇也被越来越多实施双语教学的学校所采用。

权威的作者、经典的教材、一流的译者、严格的审校、精细的编辑，这些因素使我们的图书有了质量的保证。随着计算机科学与技术专业学科建设的不断完善和教材改革的逐渐深化，教育界对国外计算机教材的需求和应用都将步入一个新的阶段，我们的目标是尽善尽美，而反馈的意见正是我们达到这一终极目标的重要帮助。华章公司欢迎老师和读者对我们的工作提出建议或给予指正，我们的联系方式如下：

华章网站：www.hzbook.com

电子邮件：hzsj@hzbook.com

联系电话：(010) 88379604

联系地址：北京市西城区百万庄南街1号

邮政编码：100037



华章科技图书出版中心

In Praise of *Digital Design and Computer Architecture*

ARM® Edition

Harris and Harris have done a remarkable and commendable job in creating a true textbook which clearly shows their love and passion for teaching and educating. The students who read this book will be thankful to Harris and Harris for many years after graduation. The writing style, the clearness, the detailed diagrams, the flow of information, the gradual increase in the complexity of the subjects, the great examples throughout the chapters, the exercises at the end of the chapters, the concise yet clear explanations, the useful real-world examples, the coverage of all aspects of each topic—all of these things are done very well. If you are a student using this book for your course get ready to have fun, be impressed, and learn a great deal as well!

Mehdi Hatamian, Sr. Vice President, Broadcom

Harris and Harris have done an excellent job creating this ARM version of their popular book, *Digital Design and Computer Architecture*. Retargeting to ARM is a challenging task, but the authors have done it successfully while maintaining their clear and thorough presentation style, as well as their outstanding documentation quality. I believe this new edition will be very much welcomed by both students and professionals.

Donald Hung, San Jose State University

Of all the textbooks I've reviewed and assigned in my 10 years as a professor, *Digital Design and Computer Architecture* is one of only two that is unquestionably worth buying. (The other is *Computer Organization and Design*.) The writing is clear and concise; the diagrams are easy to understand; and the CPU the authors use as a running example is complex enough to be realistic, yet simple enough to be thoroughly understood by my students.

Zachary Kurmas, Grand Valley State University

Digital Design and Computer Architecture brings a fresh perspective to an old discipline. Many textbooks tend to resemble overgrown shrubs, but Harris and Harris have managed to prune away the deadwood while preserving the fundamentals and presenting them in a contemporary context. In doing so, they offer a text that will benefit students interested in designing solutions for tomorrow's challenges.

Jim Frenzel, University of Idaho

Harris and Harris have a pleasant and informative writing style. Their treatment of the material is at a good level for introducing students to computer engineering with plenty of helpful diagrams. Combinational circuits, microarchitecture, and memory systems are handled particularly well.

James Pinter-Lucke, Claremont McKenna College

Harris and Harris have written a book that is very clear and easy to understand. The exercises are well-designed and the real-world examples are a nice touch. The lengthy and confusing explanations often found in similar textbooks are not seen here. It's obvious that the authors have devoted a great deal of time and effort to create an accessible text. I strongly recommend *Digital Design and Computer Architecture*.

Peiyi Zhao, Chapman University

Preface

This book is unique in its treatment in that it presents digital logic design from the perspective of computer architecture, starting at the beginning with 1's and 0's, and leading through the design of a microprocessor.

We believe that building a microprocessor is a special rite of passage for engineering and computer science students. The inner workings of a processor seem almost magical to the uninitiated, yet prove to be straightforward when carefully explained. Digital design in itself is a powerful and exciting subject. Assembly language programming unveils the inner language spoken by the processor. Microarchitecture is the link that brings it all together.

The first two editions of this increasingly popular text have covered the MIPS architecture in the tradition of the widely used architecture books by Patterson and Hennessy. As one of the original Reduced Instruction Set Computing architectures, MIPS is clean and exceptionally easy to understand and build. MIPS remains an important architecture and has been infused with new energy after Imagination Technologies acquired it in 2013.

Over the past two decades, the ARM architecture has exploded in popularity because of its efficiency and rich ecosystem. More than 50 billion ARM processors have been shipped, and more than 75% of humans on the planet use products with ARM processors. At the time of this writing, nearly every cell phone and tablet sold contains one or more ARM processors. Forecasts predict tens of billions more ARM processors soon controlling the Internet of Things. Many companies are building high-performance ARM systems to challenge Intel in the server market. Because of the commercial importance and student interest, we have developed this ARM edition of this book.

Pedagogically, the learning objectives of the MIPS and ARM editions are identical. The ARM architecture has a number of features including addressing modes and conditional execution that contribute to its efficiency but add a small amount of complexity. The microarchitectures also are very similar, with conditional execution and the program counter being the largest changes. The chapter on I/O provides numerous examples using the Raspberry Pi, a very popular ARM-based embedded Linux single board computer.

We expect to offer both MIPS and ARM editions as long as the market demands.

FEATURES

Side-by-Side Coverage of SystemVerilog and VHDL

Hardware description languages (HDLs) are at the center of modern digital design practices. Unfortunately, designers are evenly split between the two dominant languages, SystemVerilog and VHDL. This book introduces HDLs in Chapter 4 as soon as combinational and sequential logic design has been covered. HDLs are then used in Chapters 5 and 7 to design larger building blocks and entire processors. Nevertheless, Chapter 4 can be skipped and the later chapters are still accessible for courses that choose not to cover HDLs.

This book is unique in its side-by-side presentation of SystemVerilog and VHDL, enabling the reader to learn the two languages. Chapter 4 describes principles that apply to both HDLs, and then provides language-specific syntax and examples in adjacent columns. This side-by-side treatment makes it easy for an instructor to choose either HDL, and for the reader to transition from one to the other, either in a class or in professional practice.

ARM Architecture and Microarchitecture

Chapters 6 and 7 offer the first in-depth coverage of the ARM architecture and microarchitecture. ARM is an ideal architecture because it is a real architecture shipped in millions of products yearly, yet it is streamlined and easy to learn. Moreover, because of its popularity in the commercial and hobbyist worlds, simulation and development tools exist for the ARM architecture. All material relating to ARM[®] technology has been reproduced with permission from ARM Limited.

Real-World Perspectives

In addition to the real-world perspective in discussing the ARM architecture, Chapter 6 illustrates the architecture of Intel x86 processors to offer another perspective. Chapter 9 (available as an online supplement) also describes peripherals in the context of the Raspberry Pi single-board computer, a hugely popular ARM-based platform. These real-world perspective chapters show how the concepts in the chapters relate to the chips found in many PCs and consumer electronics.

Accessible Overview of Advanced Microarchitecture

Chapter 7 includes an overview of modern high-performance microarchitectural features including branch prediction, superscalar, and out-of-order operation, multithreading, and multicore processors. The treatment is accessible to a student in a first course and shows

how the microarchitectures in the book can be extended to modern processors.

End-of-Chapter Exercises and Interview Questions

The best way to learn digital design is to do it. Each chapter ends with numerous exercises to practice the material. The exercises are followed by a set of interview questions that our industrial colleagues have asked students who are applying for work in the field. These questions provide a helpful glimpse into the types of problems that job applicants will typically encounter during the interview process. Exercise solutions are available via the book's companion and instructor websites.

ONLINE SUPPLEMENTS

Supplementary materials are available online at <http://booksite.elsevier.com/9780128000564>. This companion site (accessible to all readers) includes the following:

- ▶ Solutions to odd-numbered exercises
- ▶ Links to professional-strength computer-aided design (CAD) tools from Altera®
- ▶ Link to Keil's ARM Microcontroller Development Kit (MDK-ARM), a tool for compiling, assembling, and simulating C and assembly code for ARM processors
- ▶ Hardware description language (HDL) code for the ARM processor
- ▶ Altera Quartus II helpful hints
- ▶ Lecture slides in PowerPoint (PPT) format
- ▶ Sample course and laboratory materials
- ▶ List of errata

The instructor site (linked to the companion site and accessible to adopters who register at <http://booksite.elsevier.com/9780128000564>) includes the following:

- ▶ Solutions to all exercises
- ▶ Links to professional-strength computer-aided design (CAD) tools from Altera®
- ▶ Figures from the text in PDF and PPT formats

Additional details on using the Altera, Raspberry Pi, and MDK-ARM tools in your course are provided. Details on the sample laboratory materials are also provided here.

HOW TO USE THE SOFTWARE TOOLS IN A COURSE

Altera Quartus II

Quartus II Web Edition is a free version of the professional-strength Quartus™ II FPGA design tools. It allows students to enter their digital designs in schematic or using either the SystemVerilog or the VHDL hardware description language (HDL). After entering the design, students can simulate their circuits using ModelSim™-Altera Starter Edition, which is available with the Altera Quartus II Web Edition. Quartus II Web Edition also includes a built-in logic synthesis tool supporting both SystemVerilog and VHDL.

The difference between Web Edition and Subscription Edition is that Web Edition supports a subset of the most common Altera FPGAs. The difference between ModelSim-Altera Starter Edition and ModelSim commercial versions is that the Starter Edition degrades performance for simulations with more than 10,000 lines of HDL.

Keil's ARM Microcontroller Development Kit (MDK-ARM)

Keil's MDK-ARM is a tool for developing code for an ARM processor. It is available for free download. The MDK-ARM includes a commercial ARM C compiler and a simulator that allows students to write both C and assembly programs, compile them, and then simulate them.

LABS

The companion site includes links to a series of labs that cover topics from digital design through computer architecture. The labs teach students how to use the Quartus II tools to enter, simulate, synthesize, and implement their designs. The labs also include topics on C and assembly language programming using the MDK-ARM and Raspberry Pi development tools.

After synthesis, students can implement their designs using the Altera DE2 (or DE2-115) Development and Education Board. This powerful and competitively priced board is available from www.altera.com. The board contains an FPGA that can be programmed to implement student designs. We provide labs that describe how to implement a selection of designs on the DE2 Board using Quartus II Web Edition.

To run the labs, students will need to download and install Altera Quartus II Web Edition and either MDK-ARM or the Raspberry Pi tools. Instructors may also choose to install the tools on lab machines. The labs include instructions on how to implement the projects on the DE2 Board. The implementation step may be skipped, but we have found it of great value.

We have tested the labs on Windows, but the tools are also available for Linux.

BUGS

As all experienced programmers know, any program of significant complexity undoubtedly contains bugs. So, too, do books. We have taken great care to find and squash the bugs in this book. However, some errors undoubtedly do remain. We will maintain a list of errata on the book's webpage.

Please send your bug reports to ddcabugs@gmail.com. The first person to report a substantive bug with a fix that we use in a future printing will be rewarded with a \$1 bounty!

ACKNOWLEDGMENTS

We appreciate the hard work of Nate McFadden, Joe Hayton, Punithavathy Govindaradjane, and the rest of the team at Morgan Kaufmann who made this book happen. We love the art of Duane Bibby, whose cartoons enliven the chapters.

We thank Matthew Watkins, who contributed the section on Heterogeneous Multiprocessors in Chapter 7. We greatly appreciate the work of Joshua Vasquez, who developed code for the Raspberry Pi in Chapter 9. We also thank Josef Spjut and Ruye Wang, who class-tested the material.

Numerous reviewers substantially improved the book. They include Boyang Wang, John Barr, Jack V. Briner, Andrew C. Brown, Carl Baumgaertner, A. Utku Diril, Jim Frenzel, Jaeha Kim, Phillip King, James Pinter-Lucke, Amir Roth, Z. Jerry Shi, James E. Stine, Luke Teyssier, Peiyi Zhao, Zach Dodds, Nathaniel Guy, Aswin Krishna, Volnei Pedroni, Karl Wang, Ricardo Jasinski, Josef Spjut, Jürgen Lien, Sameer Sharma, John Nestor, Syed Manzoor, James Hoe, Srinivasa Vemuru, K. Joseph Hass, Jayantha Herath, Robert Mullins, Bruno Quoitin, Subramaniam Ganesan, Braden Phillips, John Oliver, Yahswant K. Malaiya, Mohammad Awedh, Zachary Kurmas, Donald Hung, and an anonymous reviewer. We appreciate Khaled Benkrid and his colleagues at ARM for their careful review of the ARM-related material.

We also appreciate the students in our courses at Harvey Mudd College and UNLV who have given us helpful feedback on drafts of this textbook. Of special note are Clinton Barnes, Matt Weiner, Carl Walsh, Andrew Carter, Casey Schilling, Alice Clifton, Chris Acon, and Stephen Brawner.

And last, but not least, we both thank our families for their love and support.

Contents

Preface	vi
Features	vii
Online Supplements	viii
How to Use the Software Tools in a Course	ix
Labs	ix
Bugs	x
Acknowledgments	xi
Chapter 1 From Zero to One	3
1.1 The Game Plan	3
1.2 The Art of Managing Complexity	4
1.2.1 <i>Abstraction</i>	4
1.2.2 <i>Discipline</i>	5
1.2.3 <i>The Three-Y's</i>	6
1.3 The Digital Abstraction	7
1.4 Number Systems	9
1.4.1 <i>Decimal Numbers</i>	9
1.4.2 <i>Binary Numbers</i>	9
1.4.3 <i>Hexadecimal Numbers</i>	11
1.4.4 <i>Bytes, Nibbles, and All That Jazz</i>	13
1.4.5 <i>Binary Addition</i>	14
1.4.6 <i>Signed Binary Numbers</i>	15
1.5 Logic Gates	19
1.5.1 <i>NOT Gate</i>	20
1.5.2 <i>Buffer</i>	20
1.5.3 <i>AND Gate</i>	20
1.5.4 <i>OR Gate</i>	21
1.5.5 <i>Other Two-Input Gates</i>	21
1.5.6 <i>Multiple-Input Gates</i>	21
1.6 Beneath the Digital Abstraction	22
1.6.1 <i>Supply Voltage</i>	22
1.6.2 <i>Logic Levels</i>	22
1.6.3 <i>Noise Margins</i>	23
1.6.4 <i>DC Transfer Characteristics</i>	24
1.6.5 <i>The Static Discipline</i>	24

1.7	CMOS Transistors	26
1.7.1	<i>Semiconductors</i>	27
1.7.2	<i>Diodes</i>	27
1.7.3	<i>Capacitors</i>	28
1.7.4	<i>nMOS and pMOS Transistors</i>	28
1.7.5	<i>CMOS NOT Gate</i>	31
1.7.6	<i>Other CMOS Logic Gates</i>	31
1.7.7	<i>Transmission Gates</i>	33
1.7.8	<i>Pseudo-nMOS Logic</i>	33
1.8	Power Consumption	34
1.9	Summary and a Look Ahead	35
	Exercises	37
	Interview Questions	52
Chapter 2 Combinational Logic Design		55
2.1	Introduction	55
2.2	Boolean Equations	58
2.2.1	<i>Terminology</i>	58
2.2.2	<i>Sum-of-Products Form</i>	58
2.2.3	<i>Product-of-Sums Form</i>	60
2.3	Boolean Algebra	60
2.3.1	<i>Axioms</i>	61
2.3.2	<i>Theorems of One Variable</i>	61
2.3.3	<i>Theorems of Several Variables</i>	62
2.3.4	<i>The Truth Behind It All</i>	64
2.3.5	<i>Simplifying Equations</i>	65
2.4	From Logic to Gates	66
2.5	Multilevel Combinational Logic	69
2.5.1	<i>Hardware Reduction</i>	70
2.5.2	<i>Bubble Pushing</i>	71
2.6	X's and Z's, Oh My	73
2.6.1	<i>Illegal Value: X</i>	73
2.6.2	<i>Floating Value: Z</i>	74
2.7	Karnaugh Maps	75
2.7.1	<i>Circular Thinking</i>	76
2.7.2	<i>Logic Minimization with K-Maps</i>	77
2.7.3	<i>Don't Cares</i>	81
2.7.4	<i>The Big Picture</i>	82
2.8	Combinational Building Blocks	83
2.8.1	<i>Multiplexers</i>	83
2.8.2	<i>Decoders</i>	86
2.9	Timing	88
2.9.1	<i>Propagation and Contamination Delay</i>	88
2.9.2	<i>Glitches</i>	92

2.10	Summary	95
	Exercises	97
	Interview Questions	106
Chapter 3 Sequential Logic Design		109
3.1	Introduction	109
3.2	Latches and Flip-Flops	109
	3.2.1 <i>SR Latch</i>	111
	3.2.2 <i>D Latch</i>	113
	3.2.3 <i>D Flip-Flop</i>	114
	3.2.4 <i>Register</i>	114
	3.2.5 <i>Enabled Flip-Flop</i>	115
	3.2.6 <i>Resettable Flip-Flop</i>	116
	3.2.7 <i>Transistor-Level Latch and Flip-Flop Designs</i>	116
	3.2.8 <i>Putting It All Together</i>	118
3.3	Synchronous Logic Design	119
	3.3.1 <i>Some Problematic Circuits</i>	119
	3.3.2 <i>Synchronous Sequential Circuits</i>	120
	3.3.3 <i>Synchronous and Asynchronous Circuits</i>	122
3.4	Finite State Machines	123
	3.4.1 <i>FSM Design Example</i>	123
	3.4.2 <i>State Encodings</i>	129
	3.4.3 <i>Moore and Mealy Machines</i>	132
	3.4.4 <i>Factoring State Machines</i>	134
	3.4.5 <i>Deriving an FSM from a Schematic</i>	137
	3.4.6 <i>FSM Review</i>	140
3.5	Timing of Sequential Logic	141
	3.5.1 <i>The Dynamic Discipline</i>	142
	3.5.2 <i>System Timing</i>	142
	3.5.3 <i>Clock Skew</i>	148
	3.5.4 <i>Metastability</i>	151
	3.5.5 <i>Synchronizers</i>	152
	3.5.6 <i>Derivation of Resolution Time</i>	154
3.6	Parallelism	157
3.7	Summary	161
	Exercises	162
	Interview Questions	171
Chapter 4 Hardware Description Languages		173
4.1	Introduction	173
	4.1.1 <i>Modules</i>	173
	4.1.2 <i>Language Origins</i>	174
	4.1.3 <i>Simulation and Synthesis</i>	175

4.2	Combinational Logic	177
4.2.1	<i>Bitwise Operators</i>	177
4.2.2	<i>Comments and White Space</i>	180
4.2.3	<i>Reduction Operators</i>	180
4.2.4	<i>Conditional Assignment</i>	181
4.2.5	<i>Internal Variables</i>	182
4.2.6	<i>Precedence</i>	184
4.2.7	<i>Numbers</i>	185
4.2.8	<i>Z's and X's</i>	186
4.2.9	<i>Bit Swizzling</i>	188
4.2.10	<i>Delays</i>	188
4.3	Structural Modeling	190
4.4	Sequential Logic	193
4.4.1	<i>Registers</i>	193
4.4.2	<i>Resettable Registers</i>	194
4.4.3	<i>Enabled Registers</i>	196
4.4.4	<i>Multiple Registers</i>	197
4.4.5	<i>Latches</i>	198
4.5	More Combinational Logic	198
4.5.1	<i>Case Statements</i>	201
4.5.2	<i>If Statements</i>	202
4.5.3	<i>Truth Tables with Don't Cares</i>	205
4.5.4	<i>Blocking and Nonblocking Assignments</i>	205
4.6	Finite State Machines	209
4.7	Data Types	213
4.7.1	<i>SystemVerilog</i>	214
4.7.2	<i>VHDL</i>	215
4.8	Parameterized Modules	217
4.9	Testbenches	220
4.10	Summary	224
	Exercises	226
	Interview Questions	237

Chapter 5 Digital Building Blocks 239

5.1	Introduction	239
5.2	Arithmetic Circuits	239
5.2.1	<i>Addition</i>	239
5.2.2	<i>Subtraction</i>	246
5.2.3	<i>Comparators</i>	246
5.2.4	<i>ALU</i>	248
5.2.5	<i>Shifters and Rotators</i>	251
5.2.6	<i>Multiplication</i>	252

5.2.7	<i>Division</i>	254
5.2.8	<i>Further Reading</i>	255
5.3	Number Systems	255
5.3.1	<i>Fixed-Point Number Systems</i>	255
5.3.2	<i>Floating-Point Number Systems</i>	256
5.4	Sequential Building Blocks	259
5.4.1	<i>Counters</i>	260
5.4.2	<i>Shift Registers</i>	261
5.5	Memory Arrays	264
5.5.1	<i>Overview</i>	264
5.5.2	<i>Dynamic Random Access Memory (DRAM)</i>	266
5.5.3	<i>Static Random Access Memory (SRAM)</i>	267
5.5.4	<i>Area and Delay</i>	267
5.5.5	<i>Register Files</i>	268
5.5.6	<i>Read Only Memory</i>	268
5.5.7	<i>Logic Using Memory Arrays</i>	270
5.5.8	<i>Memory HDL</i>	271
5.6	Logic Arrays	271
5.6.1	<i>Programmable Logic Array</i>	272
5.6.2	<i>Field Programmable Gate Array</i>	274
5.6.3	<i>Array Implementations</i>	279
5.7	Summary	281
	Exercises	282
	Interview Questions	293
Chapter 6 Architecture		295
6.1	Introduction	295
6.2	Assembly Language	296
6.2.1	<i>Instructions</i>	297
6.2.2	<i>Operands: Registers, Memory, and Constants</i>	298
6.3	Programming	303
6.3.1	<i>Data-processing Instructions</i>	303
6.3.2	<i>Condition Flags</i>	306
6.3.3	<i>Branching</i>	308
6.3.4	<i>Conditional Statements</i>	309
6.3.5	<i>Getting Loopy</i>	312
6.3.6	<i>Memory</i>	313
6.3.7	<i>Function Calls</i>	317
6.4	Machine Language	329
6.4.1	<i>Data-processing Instructions</i>	329
6.4.2	<i>Memory Instructions</i>	333
6.4.3	<i>Branch Instructions</i>	334
6.4.4	<i>Addressing Modes</i>	336