

经 典 原 版 书 库

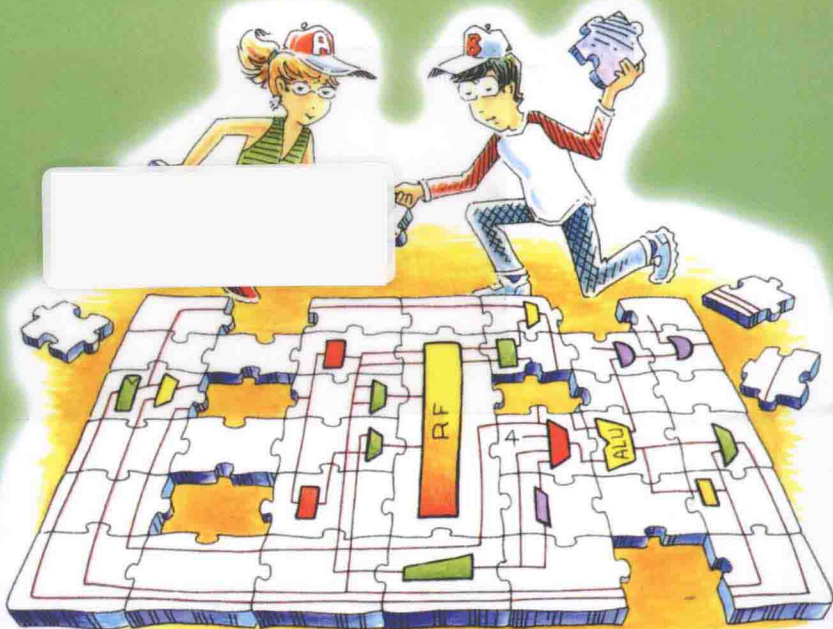
数字设计和计算机体系结构

(美) David Money Harris Sarah L. Harris 著
哈维玛德学院 哈维玛德学院

(英文版·第2版)

Digital Design and Computer Architecture

SECOND EDITION



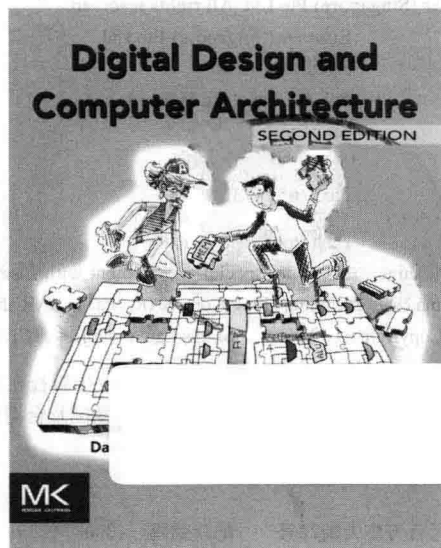
David Money Harris & Sarah L. Harris

经典原版书库

数字设计和计算机体系结构

(英文版·第2版)

*Digital Design and
Computer Architecture* (Second Edition)



(美) David Money Harris Sarah L. Harris 著
哈维玛德学院 哈维玛德学院



机械工业出版社
China Machine Press

图书在版编目 (CIP) 数据

数字设计和计算机体系结构 (英文版·第2版) / (美) 哈里斯 (Harris, D. M.), (美) 哈里斯 (Harris, S. L.) 著
—北京: 机械工业出版社, 2014.1

(经典原版书库)

书名原文: Digital Design and Computer Architecture, Second Edition

ISBN 978-7-111-44810-5

I. 数… II. ① 哈… ② 哈… III. ① 数字电路—逻辑设计—英文 ② 计算机体系结构—英文
IV. ① TN79 ② TP303

中国版本图书馆CIP数据核字 (2013) 第273901号

版权所有·侵权必究

封底无防伪标均为盗版

本书法律顾问 北京市展达律师事务所

本书版权登记号: 图字: 01-2012-7896

David Money Harris and Sarah L. Harris: Digital Design and Computer Architecture, Second Edition (ISBN 978-0-12-394424-5).

Copyright © 2013 by Elsevier Inc. All rights reserved.

Authorized English language reprint edition published by the Proprietor.

Copyright © 2013 by Elsevier (Singapore) Pte Ltd. All rights reserved.

Elsevier (Singapore) Pte Ltd.

3 Killiney Road

#08-01 Winsland House I

Singapore 239519

Tel: (65) 6349-0200

Fax: (65) 6733-1817

First Published 2014

Printed in China by China Machine Press under special arrangement with Elsevier (Singapore) Pte Ltd. This edition is authorized for sale in China only, excluding Hong Kong SAR, Macau SAR and Taiwan. Unauthorized export of this edition is a violation of the Copyright Act. Violation of this Law is subject to Civil and Criminal Penalties.

本书英文影印版由Elsevier (Singapore) Pte Ltd. 授权机械工业出版社在中国大陆境内独家出版和发行。本版仅限在中国境内 (不包括香港特别行政区、澳门特别行政区及台湾地区) 出版及标价销售。未经许可之出口, 视为违反著作权法, 将受法律之制裁。

本书封底贴有Elsevier防伪标签, 无标签者不得销售。

机械工业出版社 (北京市西城区百万庄大街22号 邮政编码 100037)

责任编辑: 迟振春

藁城市京瑞印刷有限公司印刷

2014年1月第1版第1次印刷

186mm×240mm·41.25印张

标准书号: ISBN 978-7-111-44810-5

定 价: 129.00元

凡购本书, 如有缺页、倒页、脱页, 由本社发行部调换

客服热线: (010) 88378991 88361066

投稿热线: (010) 88379604

购书热线: (010) 68326294 88379649 68995259 读者信箱: hzsj@hzbook.com

出版者的话

文艺复兴以降，源远流长的科学精神和逐步形成的学术规范，使西方国家在自然科学的各个领域取得了垄断性的优势；也正是这样的传统，使美国在信息技术发展的六十多年间名家辈出、独领风骚。在商业化的进程中，美国的产业界与教育界越来越紧密地结合，计算机学科中的许多泰山北斗同时身处科研和教学的最前线，由此而产生的经典科学著作，不仅擘划了研究的范畴，还揭示了学术的源变，既遵循学术规范，又自有学者个性，其价值并不会因年月的流逝而减退。

近年，在全球信息化大潮的推动下，我国的计算机产业发展迅猛，对专业人才的需求日益迫切。这对计算机教育界和出版界都既是机遇，也是挑战；而专业教材的建设在教育战略上显得举足轻重。在我国信息技术发展时间较短的现状下，美国等发达国家在其计算机科学发展的几十年间积淀和发展的经典教材仍有许多值得借鉴之处。因此，引进一批国外优秀计算机教材将对我国计算机教育事业的发展起到积极的推动作用，也是与世界接轨、建设真正的世界一流大学的必由之路。

机械工业出版社华章公司较早意识到“出版要为教育服务”。自1998年开始，我们就将工作重点放在了遴选、移译国外优秀教材上。经过多年的不懈努力，我们与Pearson, McGraw-Hill, Elsevier, MIT, John Wiley & Sons, Cengage等世界著名出版公司建立了良好的合作关系，从他们现有的数百种教材中甄选出Andrew S. Tanenbaum, Bjarne Stroustrup, Brian W. Kernighan, Dennis Ritchie, Jim Gray, Alfred V. Aho, John E. Hopcroft, Jeffrey D. Ullman, Abraham Silberschatz, William Stallings, Donald E. Knuth, John L. Hennessy, Larry L. Peterson等大师名家的一批经典作品，以“计算机科学丛书”为总称出版，供读者学习、研究及珍藏。大理石纹理的封面，也正体现了这套丛书的品位和格调。

“计算机科学丛书”的出版工作得到了国内外学者的鼎力襄助，国内的专家不仅提供了中肯的选题指导，还不辞劳苦地担任了翻译和审校的工作；而原书的作者也相当关注其作品在中国的传播，有的还专程为其书的中译本作序。迄今，“计算机科学丛书”已经出版了近两百个品种，这些书籍在读者中树立了良好的口碑，并被许多高校采用为正式教材和参考书籍。其影印版“经典原版书库”作为姊妹篇也被越来越多实施双语教学的学校所采用。

权威的作者、经典的教材、一流的译者、严格的审校、精细的编辑，这些因素使我们的图书有了质量的保证。随着计算机科学与技术专业学科建设的不断完善和教材改革的逐渐深化，教育界对国外计算机教材的需求和应用都将步入一个新的阶段，我们的目标是尽善尽美，而反馈的意见正是我们达到这一终极目标的重要帮助。华章公司欢迎老师和读者对我们的工作提出建议或给予指正，我们的联系方式如下：

华章网站：www.hzbook.com

电子邮件：hzjsj@hzbook.com

联系电话：(010) 88379604

联系地址：北京市西城区百万庄南街1号

邮政编码：100037



华章科技图书出版中心

In Praise of *Digital Design and Computer Architecture*

Harris and Harris have taken the popular pedagogy from Computer Organization and Design to the next level of refinement, showing in detail how to build a MIPS microprocessor in both SystemVerilog and VHDL. With the exciting opportunity that students have to run large digital designs on modern FGPAs, the approach the authors take in this book is both informative and enlightening.

David A. Patterson University of California, Berkeley

Digital Design and Computer Architecture brings a fresh perspective to an old discipline. Many textbooks tend to resemble overgrown shrubs, but Harris and Harris have managed to prune away the deadwood while preserving the fundamentals and presenting them in a contemporary context. In doing so, they offer a text that will benefit students interested in designing solutions for tomorrow's challenges.

Jim Frenzel University of Idaho

Harris and Harris have a pleasant and informative writing style. Their treatment of the material is at a good level for introducing students to computer engineering with plenty of helpful diagrams. Combinational circuits, microarchitecture, and memory systems are handled particularly well.

James Pinter-Lucke Claremont McKenna College

Harris and Harris have written a book that is very clear and easy to understand. The exercises are well-designed and the real-world examples are a nice touch. The lengthy and confusing explanations often found in similar textbooks are not seen here. It's obvious that the authors have devoted a great deal of time and effort to create an accessible text. I strongly recommend Digital Design and Computer Architecture.

Peiyi Zhao Chapman University

Harris and Harris have created the first book that successfully combines digital system design with computer architecture. Digital Design and Computer Architecture is a much-welcomed text that extensively explores digital systems designs and explains the MIPS architecture in fantastic detail. I highly recommend this book.

James E. Stine, Jr., Oklahoma State University

Digital Design and Computer Architecture is a brilliant book. Harris and Harris seamlessly tie together all the important elements in microprocessor design—transistors, circuits, logic gates, finite state machines, memories, arithmetic units—and conclude with computer architecture. This text is an excellent guide for understanding how complex systems can be flawlessly designed.

Jaeha Kim, Rambus, Inc.

Digital Design and Computer Architecture is a very well-written book that will appeal to both young engineers who are learning these subjects for the first time and also to the experienced engineers who want to use this book as a reference. I highly recommend it.

A. Utku Diril, Nvidia Corporation

Preface

Why publish yet another book on digital design and computer architecture? There are dozens of good books in print on digital design. There are also several good books about computer architecture, especially the classic texts of Patterson and Hennessy. This book is unique in its treatment in that it presents digital logic design from the perspective of computer architecture, starting at the beginning with 1's and 0's, and leading students through the design of a MIPS microprocessor.

We have used several editions of Patterson and Hennessy's *Computer Organization and Design (COD)* for many years at Harvey Mudd College. We particularly like their coverage of the MIPS architecture and microarchitecture because MIPS is a commercially successful microprocessor architecture, yet it is simple enough to clearly explain and build in an introductory class. Because our class has no prerequisites, the first half of the semester is dedicated to digital design, which is not covered by *COD*. Other universities have indicated a need for a book that combines digital design and computer architecture. We have undertaken to prepare such a book.

We believe that building a microprocessor is a special rite of passage for engineering and computer science students. The inner workings of a processor seem almost magical to the uninitiated, yet prove to be straightforward when carefully explained. Digital design in itself is a powerful and exciting subject. Assembly language programming unveils the inner language spoken by the processor. Microarchitecture is the link that brings it all together.

This book is suitable for a rapid-paced, single-semester introduction to digital design and computer architecture or for a two-quarter or two-semester sequence giving more time to digest the material and experiment in the lab. The course can be taught without prerequisites. The material is usually taught at the sophomore- or junior-year level, but may also be accessible to bright freshmen.

FEATURES

This book offers a number of special features.

Side-by-Side Coverage of SystemVerilog and VHDL

Hardware description languages (HDLs) are at the center of modern digital design practices. Unfortunately, designers are evenly split between the two dominant languages, SystemVerilog and VHDL. This book introduces HDLs in Chapter 4 as soon as combinational and sequential logic design has been covered. HDLs are then used in Chapters 5 and 7 to design larger building blocks and entire processors. Nevertheless, Chapter 4 can be skipped and the later chapters are still accessible for courses that choose not to cover HDLs.

This book is unique in its side-by-side presentation of SystemVerilog and VHDL, enabling the reader to learn the two languages. Chapter 4 describes principles applying to both HDLs, then provides language-specific syntax and examples in adjacent columns. This side-by-side treatment makes it easy for an instructor to choose either HDL, and for the reader to transition from one to the other, either in a class or in professional practice.

Classic MIPS Architecture and Microarchitecture

Chapters 6 and 7 focus on the MIPS architecture adapted from the treatment of Patterson and Hennessy. MIPS is an ideal architecture because it is a real architecture shipped in millions of products yearly, yet it is streamlined and easy to learn. Moreover, hundreds of universities around the world have developed pedagogy, labs, and tools around the MIPS architecture.

Real-World Perspectives

Chapters 6, 7, and 8 illustrate the architecture, microarchitecture, and memory hierarchy of Intel x86 processors. Chapter 8 also describes peripherals in the context of Microchip's PIC32 microcontroller. These real-world perspective chapters show how the concepts in the chapters relate to the chips found in many PCs and consumer electronics.

Accessible Overview of Advanced Microarchitecture

Chapter 7 includes an overview of modern high-performance microarchitectural features including branch prediction, superscalar and out-of-order operation, multithreading, and multicore processors. The treatment is accessible to a student in a first course and shows how the microarchitectures in the book can be extended to modern processors.

End-of-Chapter Exercises and Interview Questions

The best way to learn digital design is to do it. Each chapter ends with numerous exercises to practice the material. The exercises are followed by a set of interview questions that our industrial colleagues have asked students applying for work in the field. These questions provide a helpful glimpse into the types of problems job applicants will typically encounter during the interview process. (Exercise solutions are available via the book's companion and instructor webpages. For more details, see the next section, Online Supplements.)

ONLINE SUPPLEMENTS

Supplementary materials are available online at textbooks.elsevier.com/9780123944245. This companion site (accessible to all readers) includes:

- ▶ Solutions to odd-numbered exercises
- ▶ Links to professional-strength computer-aided design (CAD) tools from Altera[®] and Synopsys[®]
- ▶ Link to QtSpim (referred to generically as SPIM), a MIPS simulator
- ▶ Hardware description language (HDL) code for the MIPS processor
- ▶ Altera Quartus II helpful hints
- ▶ Microchip MPLAB IDE helpful hints
- ▶ Lecture slides in PowerPoint (PPT) format
- ▶ Sample course and lab materials
- ▶ List of errata

The instructor site (linked to the companion site and accessible to adopters who register at textbooks.elsevier.com) includes:

- ▶ Solutions to all exercises
- ▶ Links to professional-strength computer-aided design (CAD) tools from Altera[®] and Synopsys[®]. (Synopsys offers Synplify[®] Premier to qualified universities in a package of 50 licenses. For more information on the Synopsys University program, go to the instructor site for this book.)
- ▶ Figures from the text in JPG and PPT formats

Additional details on using the Altera, Synopsys, Microchip, and QtSpim tools in your course are provided in the next section. Details on the sample lab materials are also provided here.

HOW TO USE THE SOFTWARE TOOLS IN A COURSE

Altera Quartus II

Quartus II Web Edition is a free version of the professional-strength Quartus™ II FPGA design tools. It allows students to enter their digital designs in schematic or using either the SystemVerilog or VHDL hardware description language (HDL). After entering the design, students can simulate their circuits using ModelSim™-Altera Starter Edition, which is available with the Altera Quartus II Web Edition. Quartus II Web Edition also includes a built-in logic synthesis tool supporting both SystemVerilog and VHDL.

The difference between Web Edition and Subscription Edition is that Web Edition supports a subset of the most common Altera FPGAs. The difference between ModelSim-Altera Starter Edition and ModelSim commercial versions is that Starter Edition degrades performance for simulations with more than 10,000 lines of HDL.

Microchip MPLAB IDE

Microchip MPLAB Integrated Development Environment (IDE) is a tool for programming PIC microcontrollers and is available for free download. MPLAB integrates program writing, compiling, simulating, and debugging into a single interface. It includes a C compiler and debugger, allowing the students to develop C and assembly programs, compile them, and optionally program them onto a PIC microcontroller.

Optional Tools: Synplify Premier and QtSpim

Synplify Premier and QtSpim are optional tools that can be used with this material.

The Synplify Premier product is a synthesis and debug environment for FPGA and CPLD design. Included is HDL Analyst, a unique graphical HDL analysis tool that automatically generates schematic views of the design with cross-probing back to the HDL source code. This is immensely useful in the learning and debugging process.

Synopsys offers Synplify Premier to qualified universities in a package of 50 licenses. For more information on the Synopsys University program or the Synopsys FPGA design software, visit the instructor site for this book (textbooks.elsevier.com/9780123944245).

QtSpim, also called simply SPIM, is a MIPS simulator that runs MIPS assembly code. Students enter their MIPS assembly code into a text file and run it using QtSpim. QtSpim displays the instructions, memory, and register values. Links to the user's manual and example files are available at the companion site (textbooks.elsevier.com/9780123944245).

LABS

The companion site includes links to a series of labs that cover topics from digital design through computer architecture. The labs teach students how to use the Quartus II tools to enter, simulate, synthesize, and implement their designs. The labs also include topics on C and assembly language programming using the Microchip MPLAB IDE.

After synthesis, students can implement their designs using the Altera DE2 Development and Education Board. This powerful and competitively priced board is available from www.altera.com. The board contains an FPGA that can be programmed to implement student designs. We provide labs that describe how to implement a selection of designs on the DE2 Board using Cyclone II Web Edition.

To run the labs, students will need to download and install Altera Quartus II Web Edition and Microchip MPLAB IDE. Instructors may also choose to install the tools on lab machines. The labs include instructions on how to implement the projects on the DE2 Board. The implementation step may be skipped, but we have found it of great value.

We have tested the labs on Windows, but the tools are also available for Linux.

BUGS

As all experienced programmers know, any program of significant complexity undoubtedly contains bugs. So too do books. We have taken great care to find and squash the bugs in this book. However, some errors undoubtedly do remain. We will maintain a list of errata on the book's webpage.

Please send your bug reports to ddcabugs@onehotlogic.com. The first person to report a substantive bug with a fix that we use in a future printing will be rewarded with a \$1 bounty!

ACKNOWLEDGMENTS

First and foremost, we thank David Patterson and John Hennessy for their pioneering MIPS microarchitectures described in their *Computer Organization and Design* textbook. We have taught from various editions of their book for many years. We appreciate their gracious support of this book and their permission to build on their microarchitectures.

Duane Bibby, our favorite cartoonist, labored long and hard to illustrate the fun and adventure of digital design. We also appreciate the enthusiasm of Nate McFadden, Todd Green, Danielle Miller, Robyn Day, and the rest of the team at Morgan Kaufmann who made this book happen.

We'd like to thank Matthew Watkins who contributed the section on Heterogeneous Multiprocessors in Chapter 7. We also appreciate the

work of Chris Parks, Carl Pearson, and Johnathan Chai who tested code and developed content for the second edition.

Numerous reviewers substantially improved the book. They include John Barr, Jack V. Briner, Andrew C. Brown, Carl Baumgaertner, A. Utku Diril, Jim Frenzel, Jaeha Kim, Phillip King, James Pinter-Lucke, Amir Roth, Z. Jerry Shi, James E. Stine, Luke Teyssier, Peiyi Zhao, Zach Dodds, Nathaniel Guy, Aswin Krishna, Volnei Pedroni, Karl Wang, Ricardo Jasinski, and an anonymous reviewer.

We also appreciate the students in our course at Harvey Mudd College who have given us helpful feedback on drafts of this textbook. Of special note are Matt Weiner, Carl Walsh, Andrew Carter, Casey Schilling, Alice Clifton, Chris Acon, and Stephen Brawner.

And, last but not least, we both thank our families for their love and support.

About the Authors

David Money Harris is a professor of engineering at Harvey Mudd College. He received his Ph.D. in electrical engineering from Stanford University and his M.Eng. in electrical engineering and computer science from MIT. Before attending Stanford, he worked at Intel as a logic and circuit designer on the Itanium and Pentium II processors. Since then, he has consulted at Sun Microsystems, Hewlett-Packard, Evans & Sutherland, and other design companies.

David's passions include teaching, building chips, and exploring the outdoors. When he is not at work, he can usually be found hiking, mountaineering, or rock climbing. He particularly enjoys hiking with his three sons. David holds about a dozen patents and is the author of three other textbooks on chip design, as well as four guidebooks to the Southern California mountains.

Sarah L. Harris is an associate professor of engineering at Harvey Mudd College. She received her Ph.D. and M.S. in electrical engineering from Stanford University. Before attending Stanford, she received a B.S. in electrical and computer engineering from Brigham Young University. Sarah has also worked at Hewlett-Packard, the San Diego Supercomputer Center, and Nvidia.

Sarah loves teaching and experimenting in the lab. When she is not working or running after her two sons, you can find her playing music with friends, hiking, kayaking, biking, and traveling.

Contents

In Praise of Digital Design and Computer Architecture	iv
Preface	vi
About the Authors	xii
Chapter 1 From Zero to One	3
1.1 The Game Plan	3
1.2 The Art of Managing Complexity	4
1.2.1 <i>Abstraction</i>	4
1.2.2 <i>Discipline</i>	5
1.2.3 <i>The Three-Y's</i>	6
1.3 The Digital Abstraction	7
1.4 Number Systems	9
1.4.1 <i>Decimal Numbers</i>	9
1.4.2 <i>Binary Numbers</i>	9
1.4.3 <i>Hexadecimal Numbers</i>	11
1.4.4 <i>Bytes, Nibbles, and All That Jazz</i>	13
1.4.5 <i>Binary Addition</i>	14
1.4.6 <i>Signed Binary Numbers</i>	15
1.5 Logic Gates	19
1.5.1 <i>NOT Gate</i>	20
1.5.2 <i>Buffer</i>	20
1.5.3 <i>AND Gate</i>	20
1.5.4 <i>OR Gate</i>	21
1.5.5 <i>Other Two-Input Gates</i>	21
1.5.6 <i>Multiple-Input Gates</i>	21
1.6 Beneath the Digital Abstraction	22
1.6.1 <i>Supply Voltage</i>	22
1.6.2 <i>Logic Levels</i>	22
1.6.3 <i>Noise Margins</i>	23
1.6.4 <i>DC Transfer Characteristics</i>	24
1.6.5 <i>The Static Discipline</i>	24

1.7	CMOS Transistors	26
1.7.1	<i>Semiconductors</i>	27
1.7.2	<i>Diodes</i>	27
1.7.3	<i>Capacitors</i>	28
1.7.4	<i>nMOS and pMOS Transistors</i>	28
1.7.5	<i>CMOS NOT Gate</i>	31
1.7.6	<i>Other CMOS Logic Gates</i>	31
1.7.7	<i>Transmission Gates</i>	33
1.7.8	<i>Pseudo-nMOS Logic</i>	33
1.8	Power Consumption	34
1.9	Summary and a Look Ahead	35
	Exercises	37
	Interview Questions	52
Chapter 2 Combinational Logic Design		55
2.1	Introduction	55
2.2	Boolean Equations	58
2.2.1	<i>Terminology</i>	58
2.2.2	<i>Sum-of-Products Form</i>	58
2.2.3	<i>Product-of-Sums Form</i>	60
2.3	Boolean Algebra	60
2.3.1	<i>Axioms</i>	61
2.3.2	<i>Theorems of One Variable</i>	61
2.3.3	<i>Theorems of Several Variables</i>	62
2.3.4	<i>The Truth Behind It All</i>	64
2.3.5	<i>Simplifying Equations</i>	65
2.4	From Logic to Gates	66
2.5	Multilevel Combinational Logic	69
2.5.1	<i>Hardware Reduction</i>	70
2.5.2	<i>Bubble Pushing</i>	71
2.6	X's and Z's, Oh My	73
2.6.1	<i>Illegal Value: X</i>	73
2.6.2	<i>Floating Value: Z</i>	74
2.7	Karnaugh Maps	75
2.7.1	<i>Circular Thinking</i>	76
2.7.2	<i>Logic Minimization with K-Maps</i>	77
2.7.3	<i>Don't Cares</i>	81
2.7.4	<i>The Big Picture</i>	82
2.8	Combinational Building Blocks	83
2.8.1	<i>Multiplexers</i>	83
2.8.2	<i>Decoders</i>	86
2.9	Timing	88
2.9.1	<i>Propagation and Contamination Delay</i>	88
2.9.2	<i>Glitches</i>	92

2.10	Summary	95
	Exercises	97
	Interview Questions	106
Chapter 3 Sequential Logic Design		109
3.1	Introduction	109
3.2	Latches and Flip-Flops	109
3.2.1	<i>SR Latch</i>	111
3.2.2	<i>D Latch</i>	113
3.2.3	<i>D Flip-Flop</i>	114
3.2.4	<i>Register</i>	114
3.2.5	<i>Enabled Flip-Flop</i>	115
3.2.6	<i>Resettable Flip-Flop</i>	116
3.2.7	<i>Transistor-Level Latch and Flip-Flop Designs</i>	116
3.2.8	<i>Putting It All Together</i>	118
3.3	Synchronous Logic Design	119
3.3.1	<i>Some Problematic Circuits</i>	119
3.3.2	<i>Synchronous Sequential Circuits</i>	120
3.3.3	<i>Synchronous and Asynchronous Circuits</i>	122
3.4	Finite State Machines	123
3.4.1	<i>FSM Design Example</i>	123
3.4.2	<i>State Encodings</i>	129
3.4.3	<i>Moore and Mealy Machines</i>	132
3.4.4	<i>Factoring State Machines</i>	134
3.4.5	<i>Deriving an FSM from a Schematic</i>	137
3.4.6	<i>FSM Review</i>	140
3.5	Timing of Sequential Logic	141
3.5.1	<i>The Dynamic Discipline</i>	142
3.5.2	<i>System Timing</i>	142
3.5.3	<i>Clock Skew</i>	148
3.5.4	<i>Metastability</i>	151
3.5.5	<i>Synchronizers</i>	152
3.5.6	<i>Derivation of Resolution Time</i>	154
3.6	Parallelism	157
3.7	Summary	161
	Exercises	162
	Interview Questions	171
Chapter 4 Hardware Description Languages		173
4.1	Introduction	173
4.1.1	<i>Modules</i>	173
4.1.2	<i>Language Origins</i>	174
4.1.3	<i>Simulation and Synthesis</i>	175

4.2	Combinational Logic	177
4.2.1	<i>Bitwise Operators</i>	177
4.2.2	<i>Comments and White Space</i>	180
4.2.3	<i>Reduction Operators</i>	180
4.2.4	<i>Conditional Assignment</i>	181
4.2.5	<i>Internal Variables</i>	182
4.2.6	<i>Precedence</i>	184
4.2.7	<i>Numbers</i>	185
4.2.8	<i>Z's and X's</i>	186
4.2.9	<i>Bit Swizzling</i>	188
4.2.10	<i>Delays</i>	188
4.3	Structural Modeling	190
4.4	Sequential Logic	193
4.4.1	<i>Registers</i>	193
4.4.2	<i>Resettable Registers</i>	194
4.4.3	<i>Enabled Registers</i>	196
4.4.4	<i>Multiple Registers</i>	197
4.4.5	<i>Latches</i>	198
4.5	More Combinational Logic	198
4.5.1	<i>Case Statements</i>	201
4.5.2	<i>If Statements</i>	202
4.5.3	<i>Truth Tables with Don't Cares</i>	205
4.5.4	<i>Blocking and Nonblocking Assignments</i>	205
4.6	Finite State Machines	209
4.7	Data Types	213
4.7.1	<i>SystemVerilog</i>	214
4.7.2	<i>VHDL</i>	215
4.8	Parameterized Modules	217
4.9	Testbenches	220
4.10	Summary	224
	Exercises	226
	Interview Questions	237
Chapter 5 Digital Building Blocks		239
5.1	Introduction	239
5.2	Arithmetic Circuits	239
5.2.1	<i>Addition</i>	239
5.2.2	<i>Subtraction</i>	246
5.2.3	<i>Comparators</i>	246
5.2.4	<i>ALU</i>	248
5.2.5	<i>Shifters and Rotators</i>	250
5.2.6	<i>Multiplication</i>	252