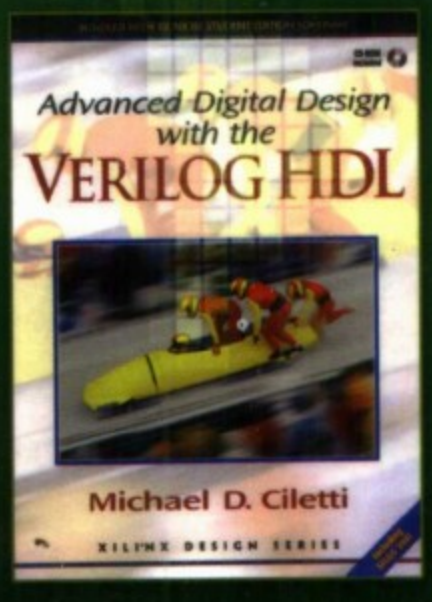
国外电子与通信教材系列

英文版

Verilog HDL 高级数字设计

Advanced Digital Design with the Verilog HDL



[美] Michael D. Ciletti 著

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Verilog HDL高级数字设计

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Advanced Digital Design with the Verilog HDL

用HDL（硬件描述语言）进行行为建模是现代ASIC（专用集成电路）设计的关键。要想成为某个杰出设计团队的一员，必须掌握设计流关键阶段中HDL的使用。本书内容并不囿于基本原理和方法，比较适合数字设计入门课程之后较深入些的课程。

本书重点讨论使用HDL进行数字设计的方法。如果读者学过逻辑设计的入门课程，将对阅读本书有很大帮助。作者希望通过以下手段逐步实现重点目标：

- 复习组合和时序逻辑的基本原理
- 介绍在设计中如何使用硬件描述语言
- 提供大量翔实的讲解，使读者能很快上手进行ASIC和/或FPGA（现场可编程门阵列）设计
- 提供较深入的、使用现代设计工具的实例，引导读者简化、验证自己的设计并使其更明晰

本书使用Verilog硬件描述语言作为通用的框架来支持所讲述的设计活动，但本书的重点是开发、验证并合成数字电路的设计，而不是Verilog语言。大多数选过数字设计方面两门以上课程的学生都应该熟悉至少一门编程语言，而且能够在阅读本书时进行相关的绘图工作。

本书附有辅助软件包，可到电子工业出版社网站（www.phei.com.cn）资源下载栏目浏览下载，或以书名为关键字搜索下载。

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Advanced Digital Design With the Verilog HDL

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北京 · BEIJING

内 容 简 介

本书通过大量完整的实例讲解了使用Verilog HDL进行超大规模集成电路设计的结构化建模方法、关键步骤和设计验证方法等实用内容。全书共分11章，涵盖了建模、结构平衡、功能验证、故障模拟和逻辑合成等关键问题，还有合成后设计确认、定时分析及可测性设计等内容。

本书结构清晰，内容组织合理，适用于计算机、电子等相关专业本科高年级学生或研究生课程，同时也适用于对学习Verilog HDL及其在现代集成电路设计流中的应用感兴趣的专业工程师和技术人员。

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序

2001年7月间，电子工业出版社的领导同志邀请各高校十几位通信领域方面的老师，商量引进国外教材问题。与会同志对出版社提出的计划十分赞同，大家认为，这对我国通信事业、特别是对高等院校通信学科的教学工作会很有好处。

教材建设是高校教学建设的主要内容之一。编写、出版一本好的教材，意味着开设了一门好的课程，甚至可能预示着一个崭新学科的诞生。20世纪40年代MIT林肯实验室出版的一套28本雷达丛书，对近代电子学科、特别是对雷达技术的推动作用，就是一个很好的例子。

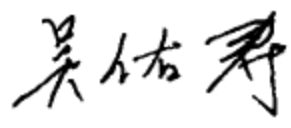
我国领导部门对教材建设一直非常重视。20世纪80年代，在原教委教材编审委员会的领导下，汇集了高等院校几百位富有教学经验的专家，编写、出版了一大批教材；很多院校还根据学校的特点和需要，陆续编写了大量的讲义和参考书。这些教材对高校的教学工作发挥了极好的作用。近年来，随着教学改革不断深入和科学技术的飞速进步，有的教材内容已比较陈旧、落后，难以适应教学的要求，特别是在电子学和通信技术发展神速、可以讲是日新月异的今天，如何适应这种情况，更是一个必须认真考虑的问题。解决这个问题，除了依靠高校的老师和专家撰写新的符合要求的教科书外，引进和出版一些国外优秀电子与通信教材，尤其是有选择地引进一批英文原版教材，是会有好处的。

一年多来，电子工业出版社为此做了很多工作。他们成立了一个“国外电子与通信教材系列”项目组，选派了富有经验的业务骨干负责有关工作，收集了230余种通信教材和参考书的详细资料，调来了100余种原版教材样书，依靠由20余位专家组成的出版委员会，从中精选了40多种，内容丰富，覆盖了电路理论与应用、信号与系统、数字信号处理、微电子、通信系统、电磁场与微波等方面，既可作为通信专业本科生和研究生的教学用书，也可作为有关专业人员的参考材料。此外，这批教材，有的翻译为中文，还有部分教材直接影印出版，以供教师用英语直接授课。希望这些教材的引进和出版对高校通信教学和教材改革能起一定作用。

在这里，我还要感谢参加工作的各位教授、专家、老师与参加翻译、编辑和出版的同志们。各位专家认真负责、严谨细致、不辞辛劳、不怕琐碎和精益求精的态度，充分体现了中国教育工作者和出版工作者的良好美德。

随着我国经济建设的发展和科学技术的不断进步，对高校教学工作会不断提出新的要求和希望。我想，无论如何，要做好引进国外教材的工作，一定要联系我国的实际。教材和学术专著不同，既要注意科学性、学术性，也要重视可读性，要深入浅出，便于读者自学；引进的教材要适应高校教学改革的需要，针对目前一些教材内容较为陈旧的问题，有目的地引进一些先进的和正在发展中的交叉学科的参考书；要与国内出版的教材相配套，安排好出版英文原版教材和翻译教材的比例。我们努力使这套教材能尽量满足上述要求，希望它们能放在学生们的课桌上，发挥一定的作用。

最后，预祝“国外电子与通信教材系列”项目取得成功，为我国电子与通信教学和通信产业的发展培土施肥。也恳切希望读者能对这些书籍的不足之处、特别是翻译中存在的问题，提出意见和建议，以便再版时更正。



中国工程院院士、清华大学教授

“国外电子与通信教材系列”出版委员会主任

出 版 说 明

进入21世纪以来，我国信息产业在生产和科研方面都大大加快了发展速度，并已成为国民经济发展的支柱产业之一。但是，与世界上其他信息产业发达的国家相比，我国在技术开发、教育培训等方面都还存在着较大的差距。特别是在加入WTO后的今天，我国信息产业面临着国外竞争对手的严峻挑战。

作为我国信息产业的专业科技出版社，我们始终关注着全球电子信息技术的发展方向，始终把引进国外优秀电子与通信信息技术教材和专业书籍放在我们工作的重要位置上。在2000年至2001年间，我社先后从世界著名出版公司引进出版了40余种教材，形成了一套“国外计算机科学教材系列”，在全国高校以及科研部门中受到了欢迎和好评，得到了计算机领域的广大教师与科研工作者的充分肯定。

引进和出版一些国外优秀电子与通信教材，尤其是有选择地引进一批英文原版教材，将有助于我国信息产业培养具有国际竞争能力的技术人才，也将有助于我国国内在电子与通信教学工作中掌握和跟踪国际发展水平。根据国内信息产业的现状、教育部《关于“十五”期间普通高等教育教材建设与改革的意见》的指示精神以及高等院校老师们反映的各种意见，我们决定引进“国外电子与通信教材系列”，并随后开展了大量准备工作。此次引进的国外电子与通信教材均来自国际著名出版商，其中影印教材约占一半。教材内容涉及的学科方向包括电路理论与应用、信号与系统、数字信号处理、微电子、通信系统、电磁场与微波等，其中既有本科专业课程教材，也有研究生课程教材，以适应不同院系、不同专业、不同层次的师生对教材的需求，广大师生可自由选择和自由组合使用。我们还将与国外出版商一起，陆续推出一些教材的教学支持资料，为授课教师提供帮助。

此外，“国外电子与通信教材系列”的引进和出版工作得到了教育部高等教育司的大力支持和帮助，其中的部分引进教材已通过“教育部高等学校电子信息科学与工程类专业教学指导委员会”的审核，并得到教育部高等教育司的批准，纳入了“教育部高等教育司推荐——国外优秀信息科学与技术系列教学用书”。

为做好该系列教材的翻译工作，我们聘请了清华大学、北京大学、北京邮电大学、东南大学、西安交通大学、天津大学、西安电子科技大学、电子科技大学等著名高校的教授和骨干教师参与教材的翻译和审校工作。许多教授在国内电子与通信专业领域享有较高的声望，具有丰富的教学经验，他们的渊博学识从根本上保证了教材的翻译质量和专业学术方面的严格与准确。我们在此对他们的辛勤工作与贡献表示衷心的感谢。此外，对于编辑的选择，我们达到了专业对口；对于从英文原书中发现的错误，我们通过与作者联络、从网上下载勘误表等方式，逐一进行了修订；同时，我们对审校、排版、印制质量进行了严格把关。

今后，我们将进一步加强同各高校教师的密切关系，努力引进更多的国外优秀教材和教学参考书，为我国电子与通信教材达到世界先进水平而努力。由于我们对国内外电子与通信教育的发展仍存在一些认识上的不足，在选题、翻译、出版等方面的工作中还有许多需要改进的地方，恳请广大师生和读者提出批评及建议。

电子工业出版社

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Preface

Simplify, Clarify, and Verify

Behavioral modeling with a hardware description language (HDL) is the key to modern design of application-specific integrated circuits (ASICs). Today, most designers use an HDL-based design method to create a high-level, language-based, abstract description of a circuit, synthesize a hardware realization in a selected technology, and verify its functionality and timing.

Students preparing to contribute to a productive design team must know how to use an HDL at key stages of the design flow. Thus, there is a need for a course that goes beyond the basic principles and methods learned in a first course in digital design. This book is written for such a course.

Many books discussing HDLs are now available, but most are oriented toward robust explanations of language syntax, and are not well-suited for classroom use. Our focus is on design methodology enabled by an HDL.

Our goal in this book is to build on a student's background from a first course in logic design by (1) reviewing basic principles of combinational and sequential logic, (2) introducing the use of HDLs in design, (3) emphasizing descriptive styles that will allow the reader to quickly design working circuits suitable for ASICs and/or field-programmable gate array (FPGA) implementation, and (4) providing in-depth design examples using modern design tools. Readers will be encouraged to simplify, clarify, and verify their designs.

The widely used Verilog hardware description language (IEEE Standard 1364) serves as a common framework supporting the design activities treated in this book, **but our focus is on developing, verifying, and synthesizing designs of digital circuits, not on the Verilog language**. Most students taking a second course in digital design will be familiar with at least one programming language and will be able to draw on that background in reading this textbook. We cover only the core and most widely used features of Verilog. In order to emphasize *using* the language in a synthesis-oriented design environment, we have purposely placed many details, features, and explanations of syntax in the Appendices for reference on an "as-needed" basis.

Most entry-level courses in digital design introduce state machines, state-transition graphs, and algorithmic-state machine (ASM) charts. We make heavy use of ASM charts and demonstrate their utility in developing behavioral models of sequential machines. The important problem of

designing a finite-state machine to control a complex datapath in a digital machine is treated in-depth with ASMD charts (i.e., ASM charts annotated to display the register operations of the controlled datapath). The design of a reduced intruction-set computer central processing unit (RISC CPU) and other important hardware units are given as examples. Our companion website includes the RISC machine's source code and an assembler that can be used to develop programs for applications. The machine also serves as a starting point for developing a more robust instruction set and architectural variants.

The Verilog language is introduced in an integrated, but selective manner, only as needed to support design examples. The text has a large set of examples illustrating how to address the key steps in a very large scale integrated (VLSI) circuit design methodology using the Verilog HDL. Examples are complete, and include source code that has been verified with the Silos-III simulator to be correct. Source code for all of the examples will be available (with important test suites) at our website.

The Intended Audience

This book is for students in an advanced course in digital design, and for professional engineers interested in learning Verilog by example, in the context of its use in the design flow of modern integrated circuits. The level of presentation is appropriate for seniors and first-year graduate students in electrical engineering, computer engineering, and computer science, as well as for professional engineers who have had an introductory course in logic design. The book presumes a basic background in Boolean algebra and its use in logic circuit design and a familiarity with finite-state machines. Building on this foundation, the book addresses the design of several important circuits used in computer systems, digital signal processing, image processing, data transfer across clock domains, built-in self-test (BIST), and other applications. The book covers the key design problems of modeling, architectural tradeoffs, functional verification, timing analysis, test generation, fault simulation, design for testability, logic synthesis, and postsynthesis verification.

Special Features of the Book

- Begins with a brief review of basic principles in combinational and sequential logic
- Focuses on modern digital design methodology
- Illustrates and promotes a synthesis-ready style of register transfer level (RTL) and algorithmic modeling with Verilog
- Demonstrates the utility of ASM charts for behavioral modeling
- In-depth treatment of algorithms and architectures for digital machines (e.g., an image processor, digital filters and circular buffers)
- In-depth treatment of synthesis for cell-based ASICs and FPGAs
- A practical treatment of timing analysis, fault simulation, testing, and design for testability, with examples
- Comprehensive treatment of behavioral modeling
- Comprehensive design examples, including a RISC machine and datapath controller
- Numerous graphical illustrations
- Provides several problems with a wide range of difficulty after each chapter
- Contains a worked example with JTAG and BIST for testing

- Contains over 250 fully verified examples
- An indexed list of all models developed in the examples
- A set of Xilinx FPGA-based laboratory-ready exercises linked to the book (e.g., arithmetic and logic unit [ALU], a programmable lock, a key pad scanner with a FIFO, a serial communications link with error correction, an SRAM controller, and first in, first out [FIFO] memory)
- Contains an up-to-date chapter on programmable logic device (PLDs) and FPGAs
- Contains a packaged CD-ROM with the popular Silos-III Verilog design environment and simulator and the Xilinx integrated synthesis environment (ISE) synthesis tool for FPGAs
- Contains an Appendix with full formal syntax of the Verilog HDL
- Covers major features of Verilog 2001, with examples
- Supported by an ongoing website containing:

1. Source files of models developed in the examples
2. Source files of testbenches for simulating examples
3. An Instructor's Classroom Kit containing transparency files for a course based on the subject matter
4. Solutions to selected problems
5. Jump-start tutorials helping students get immediate results with the Silos-III simulation environment, the Xilinx FPGA synthesis tool, the Synopsys synthesis tools, and the Synopsys Prime Time static timing analyzer
6. ASIC standard-cell library with synthesis and timing database
7. Answers to frequently asked questions (FAQs)
8. Clever examples submitted by readers
9. Revisions

Sequences for Course Presentation

The material in the text begins with a review of combinational and sequential logic design, but then progresses in the order dictated by the design flow for an ASIC or an FPGA. Chapters 1 to 6 treat design topics through synthesis, and should be covered in order, but Chapters 7 to 10 can be covered in any order. The homework exercises are challenging, and the laboratory-ready Xilinx-based exercises are suitable for a companion laboratory or for end-of-semester projects. Chapter 10 presents several architectures for arithmetic operations, affording a diversity of coverage. Chapter 11 treats postsynthesis design validation, timing analysis, fault simulation, and design for testability. The coverage of these topics can be omitted, depending on the level and focus of the course. Tools supporting Verilog 2001 are emerging, so an appendix discusses and illustrates the important new features of the language.

Chapter Descriptions

Chapter 1 briefly discusses the role of HDLs in design flows for cell-based ASICs and FPGAs. Chapters 2 and 3 review mainstream topics that would be covered in a first course in digital design, using classical methods (i.e. Karnaugh maps). This material will refresh the reader's background, and the examples will be used later to introduce HDL-based methods of design. Chapters 4 and 5

introduce modeling of combinational and sequential logic with the Verilog HDL, and place emphasis on coding styles that are used in behavioral modeling. Chapter 6 addresses cell-based synthesis of ASICs, and introduces synthesis of combinational and sequential logic. Here we pursue two main objectives: (1) present synthesis-friendly coding styles, and (2) form a foundation that will enable the reader to anticipate the results of synthesis, especially when synthesizing sequential machines. Many sequential machines are partitioned into a datapath and a controller. Chapter 7 covers examples that illustrate how to design a controller for a datapath. The designs of a simple RISC CPU and a UART[1] serve as platforms for the subject matter. Chapter 8 covers PLDs, complex PLDs (CPLDs), ROMs, and static random-access memories (SRAMs), then expands the synthesis target to include FPGAs. Verilog has been used extensively to design computers and signal processors. Chapter 9 treats the modeling and synthesis of computational units and algorithms found in computer architectures, digital filters, and other processors. Chapter 10 develops and refines algorithms and architectures for the arithmetic units of digital machines. In Chapter 11 we use the Verilog HDL in conjunction with fault simulators and timing analyzers to revisit a selection of previously designed machines and consider performance/timing issues and testability, to complete the treatment of design flow tasks that rely heavily on designer intervention. Chapter 11 models the test access port (TAP) controller defined by the IEEE 1149.1 standard (commonly known as the JTAG standard), and presents an example of its use. Another elaborate example covers built-in self test (BIST).

Acknowledgments

The author is grateful for the support of colleagues and students who expanded his vision of Verilog and contributed to this textbook. The reviewers of the original manuscript provided encouragement, critical judgment, and many helpful suggestions. Stu Sutherland helped the author gain a deeper appreciation for the issue of race conditions that can creep into the models of a digital system. These insights led to the disciplined style of adhering to nonblocking assignments for modeling edge-sensitive behavior and blocked assignments for modeling level-sensitive behavior. I owe a debt of gratitude to Dr. Jim Tracy and Dr. Rodger Ziemer, who supported my efforts to develop courses in VLSI circuit design; to Bill Fuchs, who introduced me to the Silos-III Verilog simulator from Simucad, Inc., and placed a user-friendly design environment in the hands of our students. Kirk Sprague and Scott Kukel were helpful in developing a Hamming encoder to work with the UART. Cris Hagan's thesis led to the models presented in Chapter 9 for decimators and other functional units found in digital signal processors. Rex Anderson proofread several chapters and scrubbed down my work. Terry Hansen and Lisa Horton provided the inspiration for the coffee vending machine example, and developed the assembler that supports the RISC CPU. Dr. Greg Sajdak developed material relating chip defects to test coverage and process yield. Dr. Bruce Harmon provided material for a FIR filter example. My editors, Tom Robbins and Eric Frank, have been a delight to work with. They supported the concept, encouraged my work and guided this book through the production process. My deep thanks to all of you.

[1]Universal asynchronous receiver and transmitter (UART), a circuit used in data transmission between systems.

Dedication

This book is dedicated to the memory of Sr. Laurencia Rihn, RSM, and Fr. Jerry Wilson, CSC. My life has been shaped by their faith, encouragement, and love. To my wife, Jerilynn, and our children, Monica, Lucy, Rebecca, Christine, and Michael and their spouses, Mike McCormick, David Steigerwald, Peter Van Dusen, and Michelle Puhr Ciletti, and our grandchildren, Michael, Katherine, Brigid, David, Jackson, Samantha, Peter, Anthony, and Matthew—thank you for the journey and the love we've shared.

Contents