Technical Session Contents

December 1, 1975—2·00 p.m

Session 7: Electron Tubes 1—High Power Microwave Tubes

Lincoln Room

Chairman· Les Winslow

Organizer. Burton Smith

December 2, 1975—9:00 a m.

Session 8: Solid State Devices 2—High Power, High Voltage Devices

International Ballroom+East

Chairman and Organizer: Harvey Nathanson

December 2, 1975—9 00 a.m.

Session 9: Image Transducers and Optoelectronic Devices 2—Display I Electroluminescence

International Ballroom—Center

Chairman: J. A. Hall

Organizer: L. Esterowitz

December 2, 1975—9·00 a m.

Session 10: Quantum Electronics 2—Silicon Solar Cells: Surface Junctions

Georgetown Room

Chairman and Organizer: H. W. Brandhorst, Jr.

December 2, 1975—9:00 a.m.

Session 11: Solid State Devices 3—GaAs FETs

Lincoln Room

Chairman: F. Fang

Organizer: S. G. Liu

December 2, 1975—9 00 a.m.

Session 12: Electron Tubes 2—TWT Theory and Tube Design

Thoroughbred Room

Chairman, J R M Vaughan

Organizer I Tammaru

December 2, 1975—12:00 noon

Luncheon Session: "ERDA—The Option Generator"

International Ballroom—West

December 2, 1975—2:00 p.m.

Session 13: Device Technology 2—IC Fabrication I

International Ballroom—East

Chairman: Peter W J. Verhofstadt

Organizer: W. E. Engeler

December 2, 1975—2 00 p m.

Session 14: Integrated Circuits 2—Memory Technology

International Ballroom—Center

Chairman and Organizer: R. A. Belt

December 2, 1975—2:00 p.m.

Session 15: Quantum Electronics 3—Silicon Solar Cells: P-N Junctions

Georgetown Room

Chairman and Organizer: H. Kressel

December 2, 1975—2:00 p.m

Session 16: Solid State Devices 4—Thyristors

Lincoln Room

Chairman P L Hower

Organizer: D J Coleman Jr

December 2, 1975—2 00 p.m.

Session 17: Image Transducers and Optoelectronic Devices 3—Display II

Monroe Room

Chairman B F Williams

Organizer K Nummedal

December 2, 1975—2·00 p m.

Session 18: Electron Tubes 3—Advanced Communications TWTs

Thoroughbred Room

Chairman: H. J. Wolkstein

Organizer: J L. Putz

December 3, 1975—9·00 a.m.

Session 19: Device Technology 3—IC Fabrication II

International Ballroom—East

Chairman: J. H Scott

Organizer: N. Goldsmith

December 3, 1975—9.00 a m

Session 20: Solid State Devices 5—Bipolar and MOS II

International Ballroom—West

Chairman and Organizer: R E Thomas

December 3, 1975—9:00 a m.

Session 21: Quantum Electronics 4—Devices for Fiber Optic Communications I

Georgetown Room

Chairman and Organizer: D J. Albares

December 3, 1975—9:00 a.m.

Session 22: Image Transducers and Optoelectronic Devices 4—IR Detectors and Materials

Lincoln Room

Chairman: E H. Putley

Organizer: S. P Emmons

December 3, 1975—9 00 a.m.

Session 23: Electron Tubes 4—Electron-Metal Interaction

Thoroughbred Room

Chairman: Peter Varnish

Organizer: Donald Laycock

December 3, 1975—2:00 p.m.

Session 24: Integrated Circuits 3—Logic

International Ballroom—East

Chairman and Organizer: F. H. Dill

December 3, 1975—2.00 p.m.

Session 25: Device Technology 4—Modeling and Ion Implantation

International Ballroom—West

Chairman: J. Choma

Organizer: J. N. Zemel

December 3, 1975—2 00 p.m.

Session 26: Quantum Electronics 5—Devices for Fiber Optic Communications II

Georgetown Room

Chairman and Organizer: C. L. Tang

December 3, 1975—2·00 p.m.

Session 27: Solid State Devices 6—New Devices and Device Phenomena

Thoroughbred Room

Chairman and Organizer: H. D. Hendricks

December 1, 1975—10:00 a.m.

Session 1: Invited Papers

International Ballroom—Center

Chairman: C. Neil Berglund

PATHWAYS AND PITFALLS IN DEVICE LITHOGRAPHY

Eugene I. Gordon

Bell Laboratories

Murray Hill, New Jersey 07974

ABSTRACT

The device engineer, working in silicon integrated circuits, bubble memory, microwave devices and other emerging areas consistently finds that pattern generation sets major limits on his ability to achieve higher complexity, higher performance, lower cost, greater reliability and faster design turnaround time. As a consequence major efforts are being directed to pattern generation technology. The motivation for the various activities will be examined and reviewed, and an attempt will be made to assess the relevance of these activities, pointing out potential pitfalls or areas that should be considered early in the technology development.

Exposure of a semiconductor or garnet substrate to produce contemporary microdevices follows a well-trodden path. Recent activities have made possible a wide range of alternate paths for extending the state of the art (1). These are summarized in Fig. 1. While manual generation of patterns is still utilized to some extent, the use of a software description to drive pattern generation apparatus is becoming ubiquitous.

The conventional path is shown second from the left; generation of a reticle, 10:1 reduction and step-and-repeat generation of a high quality master, and finally generation of working copies, frequently by use of intermediary submasters. Damage to the working copy during contact printing requires massive numbers of copies to be produced. A single printer operating at full capacity can chew up several hundred thousand dollars worth of masks per year. The logistics of supply imposes a harsh tyranny on the process engineer. Furthermore he must use masks which because of the multistep process initially cannot be as good as the best available and these masks degrade significantly during use.

As a result, noncontact printing has consistently been of interest. And consistently, projection printing has been disappointing despite its promise. Recently, a scanning type of projection printer (2) has had considerable success and appears to have overcome many of the deficiencies of stationary projection printers. Nevertheless, it has improvident limitations which make uncertain its use for tighter design rules than currently in commercial use.

An alternate path which uses reduction step-and-repeat printing directly on the substrate to be patterned has proven effective for applications such as microwave transistors, where fine lines, good linewidth control and excellent registration are essential. Unfortunately practical versions are expensive (~$250K) and slow (>10 minutes per exposure) and do not appear to be acceptable for use in LSI. The major drawback would appear to be the large capital expenditure that is required. However, such equipment would allow a significant extension of the state of the art.

Completing the left-hand side of Fig. 1 is an electron beam version of reduction, step-and-repeat printing. The reticle can be made optically because of its larger size. This technique is still highly exploratory and many practical problems remain.

Current hopes and interests are focused on the elements shown on the right-hand side of the figure. The use of a serial scanning electron beam for one-step fabrication of masters (3-5) has been established as a cost-effective source of very high quality, hard surface masters for conventional lithography as well as the source of very high resolution masks for 1:1 electron exposure systems (6) and X-ray proximity systems (7). Both of these are exploratory in nature. They have proven to be capable of very high resolution and high hopes reside therein. However, there are some significant pitfalls. Nonflatness of the substrate can cause severe distortion in the electron system and random misalignment or runout errors in the X-ray system. Special attention to electrostatic (for the electron system) and vacuum (for the X-ray system) chucks is required. New techniques for polishing wafers and special attention during high temperature processing may prove to be prerequisites to successful use

of these techniques in silicon technology. It is not meant to imply that such attention would not be advantageous for existing lithographic practice. It would, it just seems, not be done as much as it should be. On the other hand, substrates for bubble devices appear to be suitably flat. Other pitfalls relate to use of electron sensitive resists which cannot be used simply in place of present photoresists. Hence new processing techniques must be developed in parallel with the new exposure systems. The required changes may be so substantial that considerable investment in auxiliary equipment is entailed as well as loss of the background and experience associated with conventional lithography. Moreover, the use of electrons and soft X-rays for exposure can change the surface characteristics of electron devices, particularly silicon MOS devices, and the possibility for much grief exists. Finally, the major stumbling block, which seems to be ignored completely in the hurrah and huzza afforded these emerging techniques is that they are to be used with finer dimensions than currently used and in large area devices. The potential for problems with reliability is enormous, particularly inherent in the small dimensions, and possibly associated with the process changes.

These same pitfalls are inherent in the use of scanning electron beam systems. However, such systems exhibit the ultimate in resolution and registration capability, and wafer flatness is not nearly as relevant. Hence interest is exceptionally high. They have already proven to be of importance in fabricating microwave transistors. However, a major hurdle for LSI has been identified as the long exposure time. The current state of the art is about one-half hour for a 3-inch wafer with fine-line capability. However, this is improving rapidly, and I would not be surprised to hear reports before the end of this decade of commercial systems operating in the range of 5-10 minutes with excellent registration and fine-line capability. Unfortunately such systems will cost upwards of $\$10^6$. Some simple calculations by anyone with access to data will lead to the conclusion that one should ultimately produce higher performance LSI devices at lower cost using scanning electron beam lithography. Unfortunately the necessary capital investment in the high-speed machines alone might exceed the annual value of the product. This may prove to be a major pitfall. However, there is little doubt that there are those anxious to make the journey. For those sufficiently adroit it will probably prove to be a valuable trip.

REFERENCES

(1) E. I. Gordon and D. R. Herriott, "Pathways in Device Lithography," IEEE Trans. ED-22, 371, July 1975.

(2) D. A. Marble, "A New Projection Printer," Solid-State Technology, pp. 50-53, June 1974.

(3) J. P. Beasly and D. G. Squire, "An Electron Beam Maskmaker," IEEE Trans. ED-22, 376, July 1975.

(4) D. R. Herriott, R. J. Collier, D. S. Alles and J. W. Stafford, "EBES, A Practical Electron Lithographic System," IEEE Trans. ED-22, 385, July 1975.

(5) R. F. W. Pease, J. P. Ballantyne, R. C. Henderson, A. M. Voshchenkov, and L. D. Yau, "Applications of the Electron Beam Exposure System," IEEE Trans. ED-22, 393, July 1975.

(6) T. W. O'Keefe, J. Vinl and R. M. Handy, "An Electron Imaging System for the Fabrication of Integrated Circuits," Solid State Electronics 12, New York, Pergamon Press, 1969, pp. 841-848

(7) D. Maydan, et al., "High Speed Replication of Submicron Features by X-Ray Lithography," IEEE Trans. ED-22, 429, July 1975.

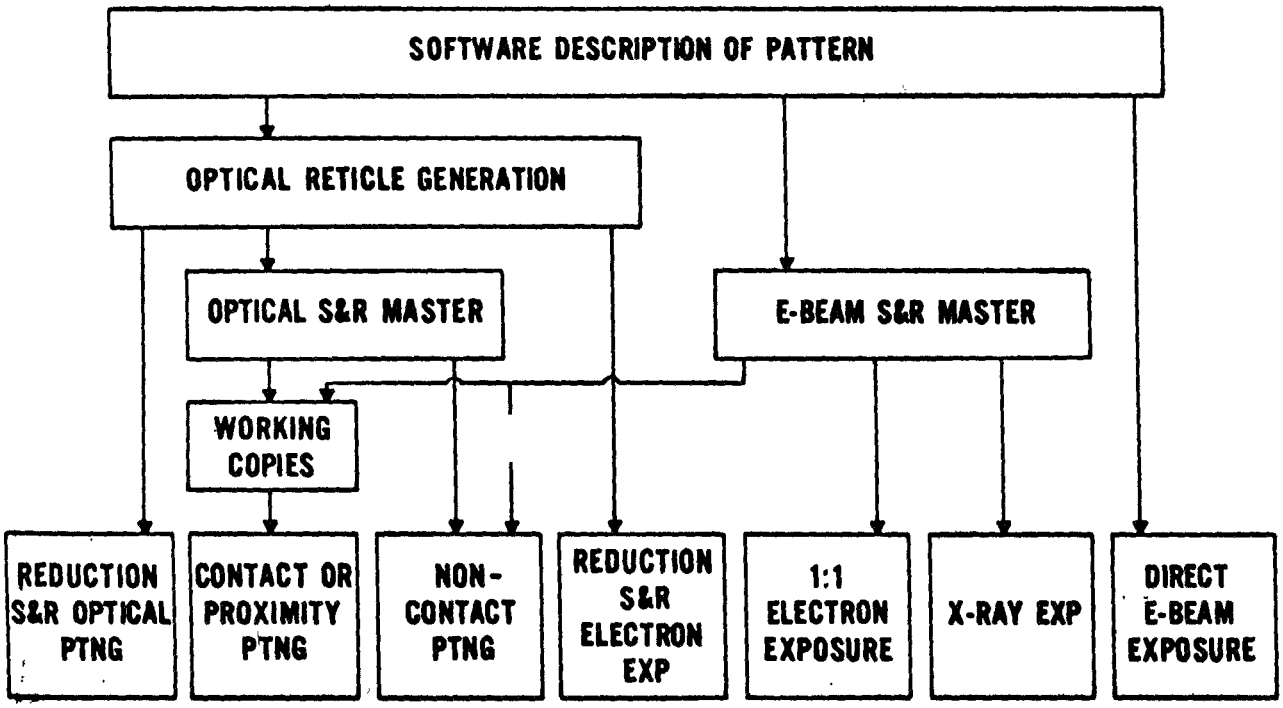

Fig. 1 - PATHWAYS TO PATTERN GENERATION

RECENT ADVANCES IN HIGH-FREQUENCY FIELD-EFFECT TRANSISTORS

Charles A. Liechti

Hewlett-Packard Company

Palo Alto, California 94304

During the 27 years since the discovery of the transistor, the advancement of transistors to higher and higher operating frequencies has been one of the most persistent objectives of semiconductor device R&D. Today, highest frequency operation and fastest switching speed are obtained from GaAs metal-semiconductor FETs (MESFETs). Above 6 GHz, MESFETs have higher gain, lower noise-figure and about the same power capability as bipolar transistors. Also, p-n junction FETs (JFETs) and insulated gate FETs (IGFETs) have advanced to microwave frequencies. The cross-sections of the various high-frequency FET structures are illustrated in Fig. 1, and their performance data are listed in Table I.

For high frequency operation, the intrinsic time-constant for charging the gate capacitance must be as short as possible. In addition, the parasitic reactances and the transit time of charge carriers through the high-field region must be minimized. These objectives are achieved (a) by shrinking the channel length to the minimum realizable size, (b) by selecting a device structure with low drain-to-channel and drain-to-gate capacitances, and (c) by choosing a semiconductor with large carrier mobility and large drift velocity at high fields. In GaAs, the conduction electrons have six-times larger mobility and two-times larger peak drift-velocity than in silicon. Therefore, GaAs FETs exhibit higher frequency operation than Si FETs. Electrons have larger mobility than holes in both GaAs and Si. Consequently, n-channel FETs are used exclusively for highest frequency applications (see Table I).

Silicon IGFETs with 1 μm channel length have been built with the vertical gate geometry (V-MOST) (2) and with double diffusion of the channel and source impurities under the same oxide layer (D-MOST) (3). IGFETs fabricated in silicon-on-sapphire (SOS-MOST) (4) exhibit very low drain-to-channel and drain-to-source capacitance. Up to 2 GHz, IGFETs are applied in high speed logic, ultralinear power amplifiers, low noise receivers and mixers. So far, practical IGFETs have been made only on silicon. Recent advances in anodic native oxides on GaAs (16), with an interface-state density of 1×10^{11} $cm^{-2}eV^{-1}$, might lead to GaAs IGFETs in the near future.

FETs with a p-n junction gate of 1-2 μm length have been realized in silicon and in GaAs. In silicon, the p-regions are selectively implanted (5); in GaAs they are presently diffused (6), or they are grown epitaxially and etched in mesa structures (7,8). Low noise JFET amplifiers have been built up to 4 GHz. A GaAs power JFET delivers 1 W output power with 6 dB gain and 26% (power added) efficiency at 6 GHz (7).

At this time, GaAs MESFETs have the largest current-gain bandwidth (20 GHz) and the highest frequency of oscillation (80 GHz) of all transistors. They operate like JFETs in a depletion mode, but instead of a p-n junction, the gate consists of a metal-to-semiconductor Schottky-barrier. The depletion layer under the metal gate restricts the conductive cross-section in the channel and controls the current flowing drom drain to source. A scanning electron micrograph of a MESFET with 1 μm gate length is shown in Fig. 2. The active n-type layer is grown epitaxially on a semi-insulating GaAs substrate. This structure offers the same advantages as silicon-on-sapphire, i.e., very low parasitic capacitances. The device geometry is simple, easy to fabricate and can be applied to a variety of semiconductors. MESFETs have been built in Si (9), GaAs (10-13), InP (14) and GaInAs (15). Their performance characteristics are listed in Table I.

GaAs MESFETs are used for microwave amplification up to 18 GHz. They have very low noise performance (NF = 2.7 dB at 10 GHz (10)), only surpassed by parametric amplifiers. In Fig. 3, the noise figures of MESFET amplifiers are shown. MESFETs with multiple gate structures are also efficient power amplifiers. At 6 GHz, 0.9 W output power with 6 dB gain and 30% (power added) efficiency has been obtained (12). In addition, MESFETs are applied as microwave oscillators, mixers and modulators.

The GaAs MESFET with 1 μm gate length and 15 GHz current-gain bandwidth is a fast switch, ideally suited for high-speed logic. The basic NAND/NOR logic gate, shown in Fig. 4, has a signal propagation delay of 100 ps* (17) and a speed-power product of 4 pJ (18). Using this logic gate, a monolithic 1:8 frequency divider with three cascaded master-slave flip-flops has been built on GaAs (Fig. 5). This circuit provides stable frequency dividion from dc up to 2 GHz (18).

* Measured for a fanout of 3. Fastest bipolar logic gates exhibit a propagation delay twice as long.

FETs promise a great deal of potential for advances to even higher speed operation. Various device structures and semiconductor materials await further development. Progress with submicrometer channels using electro-beam lithography, with ion-implanted layers, and with suitable insulators on III-V compound semiconductors will open new perspectives for high-frequency FETs.

REFERENCES

(1) Y. Morita et al., "Si UHF MOS High-Power FET," IEEE TRANS. ELECTRON DEVICES, Vol. ED-21, pp 733-734; Nov. 1974.

(2) T. Heng, Westinghouse Research Labs., private communication.

(3) R. Hansen, Signetics Corp., private communication (see also Signetics Data Sheet, SD-203/SD-308).

(4) R. Ronen and L. Strauss, "The Silicon-On-Sapphire MOS Tetrode, Some Small-Signal Features LF to UHF," IEEE TRANS. ELECTRON DEVICES, Vol. ED-21, pp 100-109; Jan. 1974.

(5) D. Lecrosnier and G. Pelous, "Ion-Implanted FET for Power Applications," IEEE TRANS. ELECTRON DEVICES, Vol. ED-21, pp 113-118; Jan. 1974.

(6) R. Zuleeg, E. Bledl and A. Behle, "Broadband GaAs Field-Effect Transistor Amplifier," Air Force Avionics Lab., Technical Report AFAL-TR-73-109, Wright-Patterson AFB, Ohio, Mar. 1973.

(7) C. Vergnolle, R. Funck and M. Laviron, "An Adequate Structure for Power Microwave FETs," 1975 Int. Solid-State Circuits Conf., DIG. TECH. PAPERS, pp 66-67.

(8) S. Umebachi et al., "A New Heterojunction Gate GaAs FET," IEEE TRANS. ELECTRON DEVICES, Vol. ED-22, pp 613-614; Aug. 1975.

(9) W. Baechtold et al., "Si and GaAs 0.5 μm-Gate Schottky-Barrier Field-Effect Transistors," ELECTRON. LETT., Vol. 9, pp 232-234; May 1973.

(10) M. Ogawa et al., "Sub-Micron Single-Gate and Dual-Gate GaAs MESFET's with Improved Low Noise and High Gain Performances," to be published in IEEE TRANS. MICROWAVE THEORY AND TECHNIQUES, Vol. MTT-24; June 1976.

(11) C. Liechti, "Performance of Dual-Gate GaAs MESFETs as Gain-Controlled Low-Noise Amplifiers and High-Speed Modulators," IEEE TRANS. MICROWAVE THEORY AND TECHNIQUES, Vol. MTT-23, pp 461-469; June 1975.

(12) M. Fukuta et al., "GaAs Microwave Power FET," to be published in IEEE TRANS. ELECTRON DEVICES.

(13) I. Drukier et al., "Medium Power J-Band MESFET's," Conf. on Active Semiconductor Devices for Microwaves and Integrated Optics, Cornell Univ.; Aug. 1975.

(14) J. Barrera and R. Archer, "InP Schottky-Gate Field-Effect Transistors," to be published in IEEE TRANS. ELECTRON DEVICES, Vol. ED-22; Nov. 1975.

(15) D. Decker, R. Fairman and C. Nishimoto, "Microwave InGaAs Schottky-Barrier-Gate Field-Effect Transistors--Preliminary Results," Conf. on Active Semiconductor Devices for Microwaves and Integrated Optics, Cornell Univ.; Aug. 1975.

(16) H. Hasegawa, K. Forward and H. Hartnagel, "New Anodic Native Oxide of GaAs with Improved Dielectric and Interface Properties," APPL. PHYS. LETT., Vol. 26, pp 567-569; May 1975.

(17) R. Van Tuyl and C. Liechti, "High-Speed Integrated Logic With GaAs MESFETs," IEEE J. SOLID-STATE CIRCUITS, Vol. SC-9, pp 269-276; Oct. 1974.

(18) R. Van Tuyl and C. Liechti, "High-Speed GaAs MSI," to be presented at the Int. Solid-State Circuits Conf.; Feb. 1976.

TABLE I. Performance Data of the High Frequency FET Structures Shown in Fig. 1.

Type*	Semi-conductor	Single/ Dual Gate	Channel			Appli-cation*	Fre-quency (GHz)	Output Power CW (W)	Assoc. Power Gain (dB)	Small Signal Gain (dB)	Power Added Effic. (%)	Noise Figure (dB)	Assoc. Gain (dB)	Noise Measure + 1 (dB)	Max. Avail. Gain (dB)	Ref.
			Type	Length (μm)	Width (mm)											
IGFET																
MOST	Si	SG	n	5	20	P	0.7	16	6	10	26					(1)
V-MOST	Si	SG	n	1	18	P	2	4	5	6	32					(2)
SG D-MOST	Si	SG	n	1		LN	1					3.0	9.0	3.3		(3)
DG D-MOST	Si	DG	n	1		LN,M	1					4.5	14	4.6	15	(3)
DG SOS-MOST	Si	DG	n	4		M	0.5								25	(4)
JFET																
Silicon	Si	SG	n	1	1.8	P	2.7	0.2	6.0		19					(5)
Diff. Junction	GaAs	SG	n	2		LN	4					2.5	10	2.7	10	(6)
Grown Junction	GaAs	SG	n	1.5	6.1	P	6	1.0	6.0	7.0	26					(7)
Heterojunction	GaAs	SG	n	2		LN										(8)
MESFET																
Silicon	Si	SG	n	0.5		LN	10					5.8			5.9	(9)
LN SG GaAs	GaAs	SG	n	0.5		LN	10					2.7	10.5	3.1	13	(10)
LN SG GaAs	GaAs	SG	n	1		LN	10					3.2	8.0	3.6	10	(11)
LN DG GaAs	GaAs	DG	n	1		LN,M	10					4.0	12	4.2	18	(11)
P SG GaAs	GaAs	SG	n	1.5	5.2	P	6	0.9	6.0	7.0	30					(12)
P SG GaAs	GaAs	SG	n	1.3	1.2	P	11	0.5	6.1	7.6	13					(13)
LN SG InP	InP	SG	n	1		LN	10					4.7	6.6	5.4	7.8	(14)
LN SG GaInAs	GaInAs	SG	n	1		LN	7					6.7	5.0	8.1	18	(15)

* LN - low noise amplification; P - power amplification; M - modulation, switching or amplification with controlled gain; SG - single-gate FET; DG - dual-gate FET.

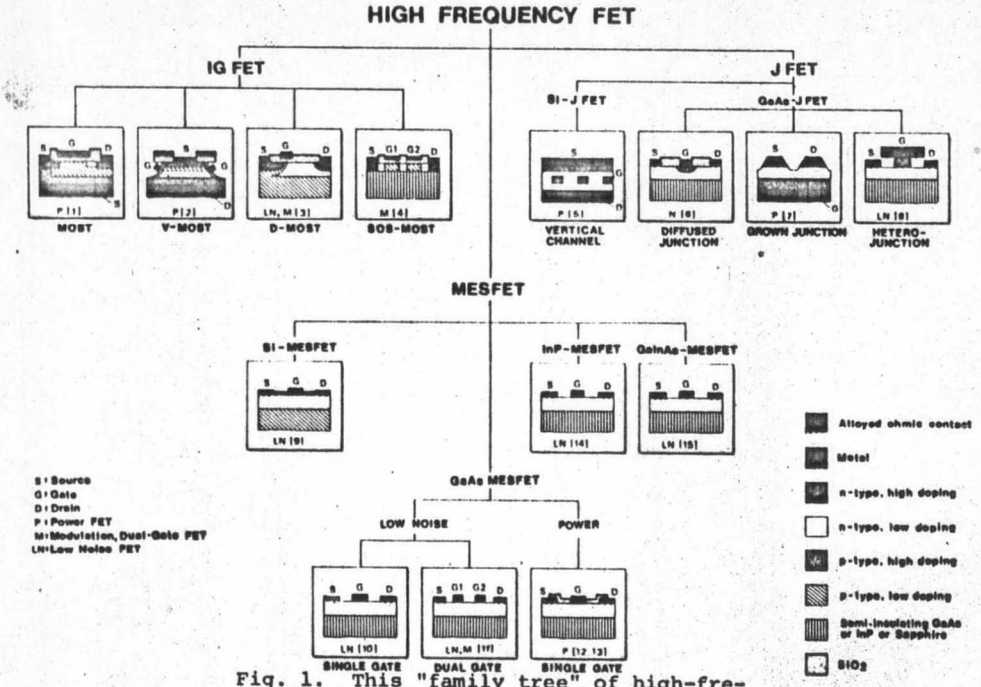

Fig. 1. This "family tree" of high-frequency FETs shows the cross-sections of the FET structures. Their performance characteristics are listed in Table I.

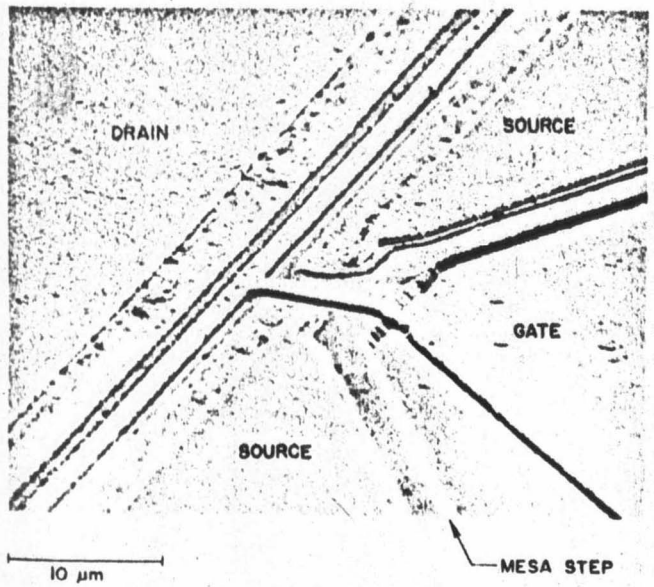

Fig. 2. The scanning electron micrograph shows the center section of a low-noise GaAs MESFET. The source and drain are alloyed ohmic contacts to the underlying conductive layer. The gate is the 1 μm wide metal stripe forming a Schottky contact. To the right, the gate metal runs over a mesa step and widens on the semi-insulating GaAs substrate into a large bonding pad.

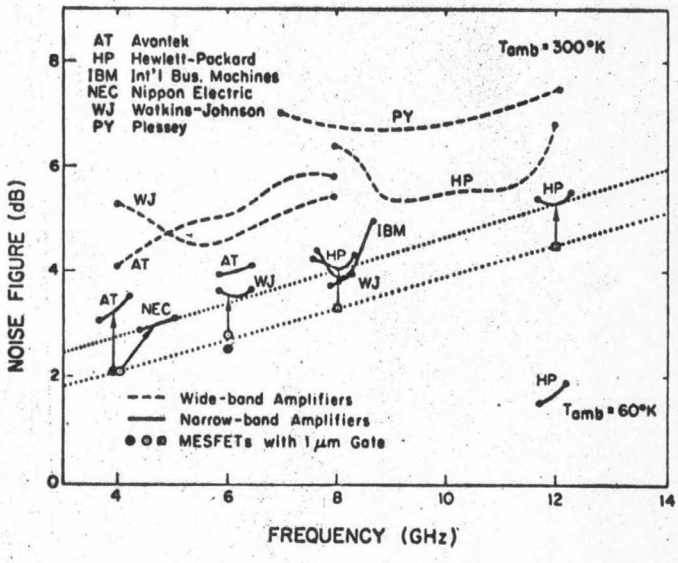

Fig. 3. The noise figure versus frequency graph summarizes performance of experimental MESFET amplifiers. The solid lines represent narrow-band amplifiers, and the circles show noise figures of the MESFETs used in the first stages. The broken lines illustrate the noise performance of wide-band amplifiers.

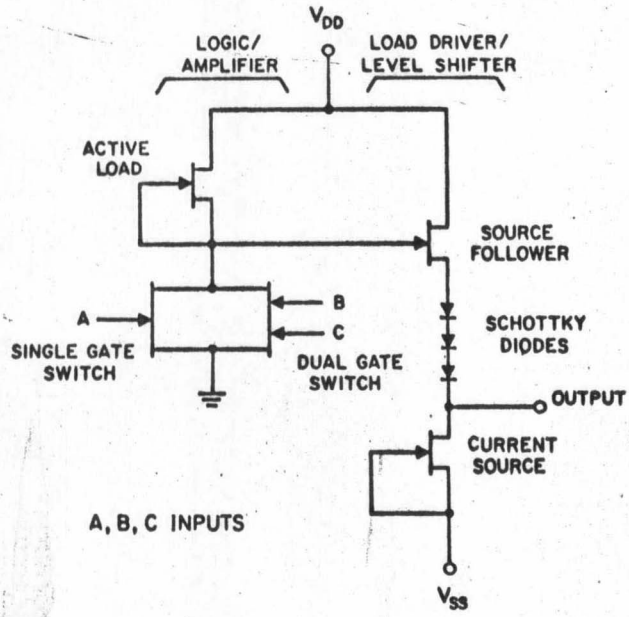

Fig. 4. This logic gate with GaAs MESFETs exhibits 100 ps signal propagation delay (17). The dual-gate MESFET performs the NAND function and the single-gate MESFET in parallel the NOR function. Since these MESFETs operate in the depletion mode, dc level shifting with forward-biased Schottky diodes is required.

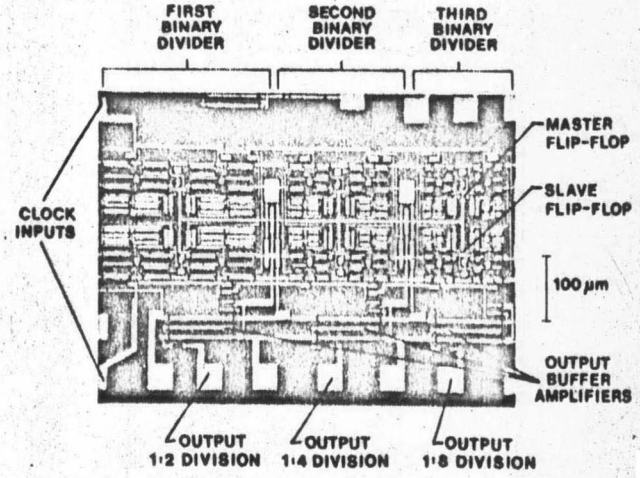

Fig. 5. This MSI circuit on GaAs provides stable 1:8 frequency division from dc to 2 GHz (18). Each binary divider consists of a master-slave flip-flop incorporating four of the logic gates shown in Fig. 4.

PROGRESS IN DIGITAL INTEGRATED ELECTRONICS

Gordon E. Moore

Intel Corporation

Santa Clara, California

Complexity of integrated circuits has approximately doubled every year since their introduction. Cost per function has decreased several thousand-fold, while system performance and reliability have been improved dramatically. Many aspects of processing and design technology have contributed to make the manufacture of such functions as complex single chip microprocessors or memory circuits economically feasible. It is possible to analyze the increase in complexity plotted in Figure 1 into different factors that can, in turn, be examined to see what contributions have been important in this development and how they might be expected to continue to evolve. The expected trends can be recombined to see how long exponential growth in complexity can be expected to continue.

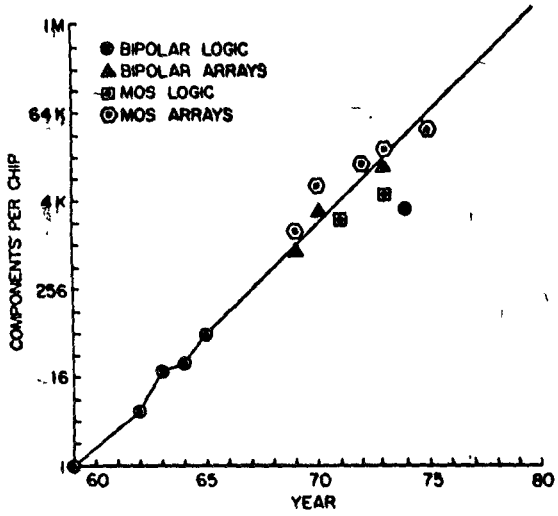

Fig. 1. Approximate component count for complex integrated circuits vs. year of introduction.

A first factor is the area of the integrated structures. Chip areas for some of the largest of the circuits used in constructing Figure 1 are plotted in Figure 2. Here again, the trend follows an exponential quite well, but with significantly lower slope than the complexity curve. Chip area for maximum complexity has increased by a factor of approximately 20 from the first planar transistor in 1959 to the 16,384-bit charge-coupled device memory chip that corresponds to the point plotted for 1975, while complexity, according to the annual doubling law, should have increased about 65,000-fold. Clearly much of the increased complexity had to result from higher density of components on the chip, rather than from the increased area available through the use of larger chips.

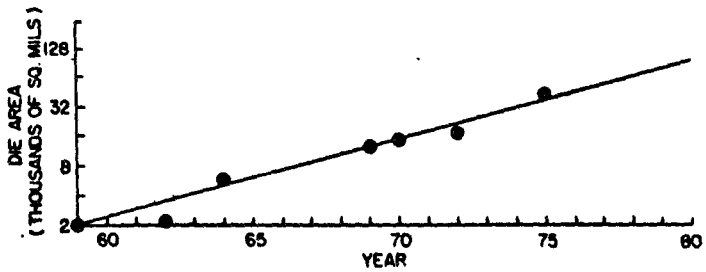

Fig. 2. Increase in die area for most complex integrated devices commercially available.

Density was increased partially by using finer scale microstructures. The first integrated circuits of 1961 used line widths of 1 mil (≈ 25 micrometers) while the 1975 device uses 5 micrometer lines. Both line width and spacing between lines are equally important in improving density. Since they have not always been equal, the average of the two is a good parameter to relate to the area that a structure might occupy. Density can be expected to be proportional to the reciprocal of area, so the contribution to improved density vs. time from the use of smaller dimensions is plotted in Figure 3.