78 CH1324-3ED

international ELECTRON DEVICES meeting

1978

WASHINGTON, D.C.

December 4–5–6

TECHNICAL DIGEST

Sponsored by Electron Devices Society of IEEE

1978 International Electron Devices Meeting
TECHNICAL DIGEST

Papers have been printed without editing as received from the authors.

All opinions expressed in the Digest are those of the authors and are not binding on The Institute of Electrical & Electronics Engineers, Inc.

Publication of a paper in this Digest in no way is intended to preclude publication of a fuller account of the paper elsewhere.

Copies of available volumes of this Digest may be obtained from The Institute of Electrical & Electronics Engineers, Inc., 445 Hoes Lane, Piscataway, N.J. Library of Congress Catalog Card Number: 78-20188.

WELCOMING STATEMENT FROM GENERAL CHAIRMAN

Alfred U. MacRae
General Chairman

Raye E. Thomas
Technical Program
Chairman

Welcome to the 24th International Electron Devices Meeting, which is sponsored by the Electron Devices Society of the IEEE. This meeting provides the primary forum in the IEEE for the presentation of recent results in research and development on electron devices, spanning a wide range of subjects that includes solid state devices and technology, integrated circuit techniques, electron tubes, energy conversion devices, detectors, sensors and displays.

The importance of solid state to electronics is emphasized by the fact that approximately 85% of the submitted papers are solid state related. The remaining papers are associated with electron tubes and plasma display devices. The international flavor of the meeting is indicated by the many countries represented in the submitted papers, with 30% of these papers coming from abroad.

The rapid increase in interest in VLSI is indicated by the many papers on this topic, covering such subjects as fine line pattern definition, short channel effects, high packing density devices and advanced fabrication techniques. The availability of microprocessors has had an impact on this meeting also with an increased number of papers on sensors and electrically alterable memory devices in evidence. Papers on mixed compound material devices are in an upward trend. Electron tube reliability and fast wave interactions will also be covered.

The success of a high technology meeting such as this one is based on the contributions of many people. The formal contributions of the authors, the questions that are asked by the people in the audience and the many hall-way discussions are all important to the exchange of information that accompanies such a meeting. The increased quality of the contributed papers is a challenge to the committee members who review these papers and form the program. On behalf of all the people who are involved in the organization of this meeting, I invite you to attend the 1978 IEDM with the anticipation that this meeting will result in a stimulating exchange of ideas between all participants.

Alfred U. MacRae
General Chairman

SPECIAL PRESENTATIONS AT IEDM LUNCHEON TUESDAY, DECEMBER 5

JACK A. MORTON AWARD:

For outstanding contributions in the field of solid-state devices.

To: Dr. Juri Matisoo

MORRIS N. LIEBMANN AWARD:

For important contribution to emerging technologies recognized not earlier than three calendar years preceding the adjudication year.

To: Dr. Kuen Charles Kao

Dr. Robert Distler Maurer

Dr. John B. MacChesney

1978 INTERNATIONAL ELECTRON DEVICES MEETING
Conference Committee

Alfred U. MacRae
General Chairman
Bell Laboratories
Murray Hill, NJ, USA

Raye E. Thomas
Technical Program Chairman
Carleton University
Ottawa, Ontario, Canada

James A. Hutchby
Technical Program Vice-Chairman
NASA Langley Research Center
Hampton, VA, USA

Harvey C. Nathanson
Chairman, Electron Devices Society
Westinghouse Corporation
Pittsburgh, PA, USA

Dave Hamilton
Publications Chairman
Bell-Northern Research
Ottawa, Ontario, Canada

Michael Fournell
Publicity Chairman
Hewlett-Packard Company
Palo Alto, CA, USA

Horst W. Gerlach
Treasurer
U.S. Army ERADCOM
Harry Diamond Labs
Adelphi, MD, USA

George Douglass, Jr.
Local Arrangements Chairman
Teledyne, MEC
Bethesda, MD, USA

Hugo Ruchardt
International Arrangements Chairman
Siemens AG
Munich, West Germany

Yoshiyuki Takeishi
International Arrangements Vice-Chairman
Tokyo Shibaura Electric Co., Ltd.
Kanagawa, Japan

Susan P. Reutershan
Conference Manager
Courtesy Associates, Inc.
Washington, DC, USA

Program Committee for the 1978 International Electron Devices Meeting held its first meeting in St. Louis, Missouri, in March. Left to right, seated are: Dave Hamilton, Publications Chairman; Raye E. Thomas, Technical Program Chairman; Alfred U. MacRae, General Chairman; and James A. Hutchby, Technical Program Vice-Chairman. Standing left to right are: Philip L. Hower, Solid State Devices; Erling Lien, Electron Tubes; Richard S. Payne, Device Technology; Don Scharfetter, Integrated Circuits; Errol EerNisse, Detectors, Sensors and Displays; Richard Stirn, Quantum Electronics and Energy Conversion Devices; and Michael Fournell, Publicity Chairman. (Not pictured, Hugo Ruchardt, International Arrangements Chairman; Yoshiyuki Takeishi, International Arrangements Vice-Chairman; George Douglass, Jr., Local Arrangements Chairman; Horst W. Gerlach, Treasurer; and Harvey C. Nathanson, Electron Devices Society.)

Subcommittee on Detectors, Sensors, and Displays

Errol P. EerNisse, Chairman
Sandia Laboratories
Albuquerque, NM, USA

Dean Baker
Naval Research Laboratory
Washington, DC, USA

Thomas P. Brody
Westinghouse Corporation
Pittsburgh, PA, USA

Savvas G. Chamberlain
University of Waterloo
Waterloo, Ontario, Canada

Stephen K. Knight
Bell Laboratories
Murray Hill, NJ, USA

J.T. Longo
Rockwell Science Center
Thousand Oaks, CA, USA

Francois Micheron
Laboratoire Central
de Recnerches
Domaine de Corbeville
Orsay, France

I. Reingold
U.S. Army Electronics
Command
Fort Monmouth, NJ, USA

G. Slottow
University of Illinois
Urbana, IL, USA

Steve Terry
Stanford University
Stanford, CA, USA

Subcommittee on Device Technology

Richard S. Payne, Chairman
Bell Laboratories
Murray Hill, NJ, USA

Martin G. Beuhler
National Bureau of Standards
Gaithersburg, MD, USA

Billy Crowder
IBM Thomas Watson Research
Center
Yorktown Heights, NY, USA

Jeffry Frey
Cornell University
Ithaca, NY, USA

Hank Geipel
IBM
Essex Junction, VT, USA

Jurgen Graul
Siemens AG Bereich Bauelemente
Munich, West Germany

Heiner Ryssel
Institute für Festkorper–
Technologie
Munich, West Germany

Alan Seales
Advanced Micro Devices
Sunnyvale, CA, USA

Al Tasch
Texas Instruments Inc.
Dallas, TX, USA

Alan Tempkin
TRW Systems
Redondo Beach, CA, USA

Takashi Tokuyama
Hitachi, Ltd.
Tokyo, Japan

Subcommittee on Electron Tubes

Erling L. Lien, Chairman
Varian Associates
Palo Alto, CA, USA

Marvin Chodorow
Stanford University
Stanford, CA, USA

Denis Connolly
NASA Lewis Research Center
Cleveland, OH, USA

Günter Döhler
Northrop Corporation
Des Plaines, IL, USA

Ward A. Harman
Hughes Aircraft Company
Torrance, CA, USA

Takao Kageyama
Nippon Electric Company, Ltd.
Kawasaki, Japan

Richard Knight
Tektronix, Inc.
Beaverton, OR, USA

U. J. Pittack
Raytheon Company
Waltham, MA, USA

Peter Varnish
British Embassy
Washington, DC, USA

Tore Wessel-Berg
University of Trondheim
Norway

N. Wilson
U.S Army Electronics
Command
Fort Monmouth, NJ, USA

Subcommittee on Integrated Circuits

Don L. Scharfetter, Chairman
Xerox Corporation
Palo Alto, CA, USA

John Barnes
Fairchild Semiconductor
Palo Alto, CA, USA

Bill Dawes
Sandia Laboratories
Albuquerque, NM, USA

Jim Dunkley
Signetics Corporation
Oren, UT, USA

Steve Evans
Texas Instruments, Inc
Dallas, TX, USA

W. J. Evans
Bell Laboratories
Murray Hill, NJ, USA

Peter H. Hudson
U S Army Electronics
Command
Fort Monmouth, NJ, USA

David V. Kerns
Auburn University
Auburn, AL, USA

William G. Oldham
University of California
Berkeley, CA, USA

Dave Sealer
MOSTEK Corporation
Carrollton TX, USA

Keming W. Yeh
Xerox Corporation
El Segundo, CA, USA

Subcommittee on Quantum Electronics and Energy Conversion Devices

Richard A. Stirn, Chairman
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, CA, USA

P. D. Dapkus
Rockwell International
Anaheim, CA, USA

E. Fabre
Laboratoires d'Electronique
et de Physique Applique
Limeil-Brevannes, France

Jerry G. Fossum
Sandia Laboratories
Albuquerque, NM, USA

Y. Hamakawa
Osaka University
Osaka, Japan

Henry Kressel
RCA Laboratories
Princeton, NJ, USA

Fredrik A. Lindholm
University of Florida
Gainesville, FL, USA

Aram Mooridian
MIT Lincoln Laboratory
Lexington, MA, USA

Gerald Stringfellow
Hewlett-Packard Laboratories
Palo Alto, CA, USA

Sigurd Wagner
Solar Energy Research
Institute
Golden, CO, USA

Subcommittee on Solid State Devices

Philip L. Hower, Chairman
Westinghouse R&D Center
Pittsburgh, PA, USA

Michael S. Adler
General Electric
Corporate R&D Center
Schenectady, NY, USA

David L. Blackburn
Institute for Applied
Technology
National Bureau of Standards
Washington, DC, USA

Terence Heng
Motorola, Inc
Phoenix, AZ, USA

Reider Kuvas
Rockwell International
Thousand Oaks, CA, USA

Youssef El-Mansy
Bell Northern Research
Ottawa, Ontario, Canada

Alan Marshak
Louisiana State University
Baton Rouge, LA, USA

Ray Martinelli
RCA Laboratories
David Sarnoff Research Center
Princeton, NJ, USA

Roger J. Van Overstraeten
Katholieke Universiteit
Leuven
Heverlee, Belgium

Max N. Yoder
Office of Naval Research
Arlington, VA, USA

1978 IEDM SCHEDULE

		INTERNATIONAL BALLROOM EAST	INTERNATIONAL BALLROOM CENTER	INTERNATIONAL BALLROOM WEST	GEORGETOWN ROOM	JEFFERSON ROOM	THOROUGHBRED ROOM	MONROE ROOM	LINCOLN ROOM WEST
MONDAY DECEMBER 4	9:30 A.M.-12 Noon		1 INVITED PAPER SESSION						
	2:00 P.M.-5:00 P.M.	2 SOLID STATE DEVICES–MOS DEVICES	3 DEVICE TECHNOLOGY FINE-LINE TECHNOLOGY	4 QUANTUM ELECTRONICS & ENERGY CONVERSION DEVICES–SILICON PHOTOVOLTAIC DEVICES	5 DETECTORS, SENSORS & DISPLAYS–SENSORS & DETECTORS	6 SOLID STATE DEVICES–MICROWAVE III-V DEVICES	7 ELECTRON TUBES–CATHODES & ELECTRON GUNS		
	6-7 P.M.					RECEPTION			
TUESDAY DECEMBER 5	9:00 A.M.-12 Noon	8 DEVICE TECHNOLOGY–DEVICE APPLICATIONS OF NEW TECHNOLOGY	9 INTEGRATED CIRCUITS–LSI STRUCTURES		10 QUANTUM ELECTRONICS & ENERGY CONVERSION DEVICES–THIN FILM & CONCENTRATOR SOLAR CELLS		11 DETECTORS, SENSORS & DISPLAYS–DISPLAY DEVICES		12 SOLID STATE DEVICES–OTHER DEVICES
	12:20 P.M.			LUNCHEON					
	2:15 P.M.-5:15 P.M.	13 SOLID STATE & ENERGY CONVERSION DEVICES HEAVY DOPING EFFECTS	14 INTEGRATED CIRCUITS–MOS VLSI MEMORY		15 SOLID STATE DEVICES–GaAs POWER FETS		16 ELECTRON TUBES–POWER TUBES & E B.S		17 DETECTORS, SENSORS & DISPLAYS–VISIBLE SOLID-STATE IMAGING DEVICES & INFRARED DETECTORS
WEDNESDAY DECEMBER 6	9:00 A.M.-12:30 P.M.	18 DEVICE TECHNOLOGY–PROCESS CHARACTERIZATION		19 SOLID STATE DEVICES–MOS VLSI DEVICE CHARACTERIZATION	20 DETECTORS, SENSORS & DISPLAYS–INFRARED IMAGING DEVICES		21 ELECTRON TUBES–TRAVELING WAVE TUBES	22 SOLID STATE DEVICES–THYRISTORS & RECTIFIERS	
	1.30 P.M.-5:00 P.M.	23 DEVICE TECHNOLOGY–ADVANCE PROCESS TECHNOLOGIES		24 INTEGRATED CIRCUITS–CHARGE COUPLED DEVICES	25 QUANTUM ELECTRONICS & ENERGY CONVERSION DEVICES–LASERS, LED'S & PHOTODETECTORS		26 SOLID STATE DEVICES–TRANSISTORS & OTHER DEVICES		

FINE LINE LITHOGRAPHY SYSTEMS FOR VLSI

A.N. Broers

IBM T.J. Watson Research Center
P.O. Box 218 Yorktown Heights, N.Y. 10598, U.S.A.

ABSTRACT

This paper discusses advantages and disadvantages of advanced lithography techniques under investigation for the fabrication of semiconductor integrated circuits. These techniques are replacing conventional ultra-violet (UV) contact/proximity printing. They employ standard UV radiation (λ = 3500Å-4000ÅA), deep UV radiation (λ = 2000Å-2600Å), soft x-rays (λ = 4Å-40Å), and electrons. It is assumed that the reader is familiar with the basic principles of the new methods.

INTRODUCTION

It used to be thought that for dimensions below about 2.5μ, light optical lithography processes would have to be abandonned and electron beam or x-ray methods adopted. This was when there was little interest in reduced dimensions in the microcircuit industry. Now this interest is widespread, but the situation has changed in two important ways: 1) optical systems have been developed which are capable of reaching dimensions close to 1μ, and 2) recognized problems with the new technologies, for example, cost for scanning electron beam systems, and throughput and mask stability for x-ray lithography , are taking longer to resolve than optimistic proponents of these methods had originally predicted. The situation is further complicated by electron beam projection methods which in ten years have neither succeeded nor failed. As a result they remain as further alternatives and bring to seven the number of distinctly different potential solutions to the sub-two micron lithography problem. The list includes contact/proximity printing with deep UV radiation, x-ray lithography, 1:1 scanning optical projection, step and repeat reduction optical projection, scanning electron beam, 1:1 photocathode electron beam projection, and step and repeat reduction electron beam projection. This paper discusses the status and some of the advantages and disadvantages of these methods. It is assumed that the reader is familiar with the principles of the different methods. They have recently been reviewed elsewhere (1). A few representative references are included to give the reader a path into the extensive literature on the subject.

CONTACT/PROXIMITY METHODS

Conventional UV proximity printing methods can be extended to resolutions below 2μ through the use of deep UV (λ = 2000 Å-2500 Å) radiation (2) (see for example figure 1). Further improvement to below 1μ is available through the simultaneous use of conformal printing methods (3) in which the gap between mask and wafer is minimized. Alignment techniques are available which can in principle reach accuracies of $\pm$0.25μ. These combined capabilities give contact/proximity printing the potential to reach resolutions beyond those of present 1X optical projection systems. Throughput can be comparable and system cost is lower.

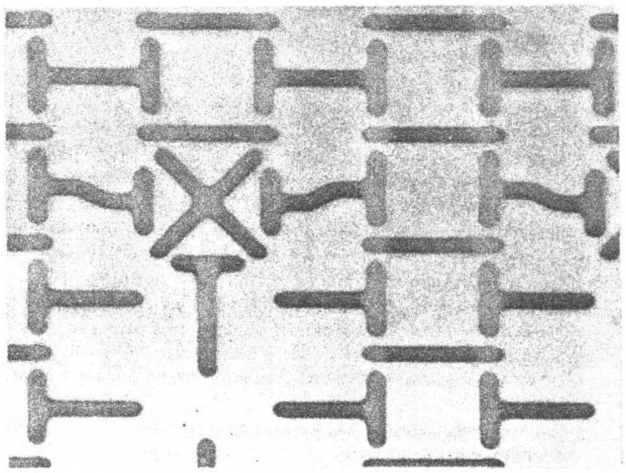

Figure 1. Proximity printed image using deep UV (2000Å-2600Å) radiation in PMMA resist. 5μ gap was maintained between mask and wafer (Lin (2)). Linewidth 1.5μ.

The reason not to use contact/proximity printing is that the close proximity between mask and wafer inevitably results in mask damage which reduces yield and increases the number of masks required for a given wafer volume. This disadvantage has clearly justified the change to projection printing at 3-4μ linewidths. The situation should be reexamined, however, in light of the potential density improvement achievable at linewidths of 1-2μ.

X-RAY LITHOGRAPHY

X-ray lithography (4,5) (proximity printing with soft x-rays) offers one outstanding advantage over other methods. Image fidelity is preserved in very thick resist layers and is not degraded by diffraction effects as it is with light optical exposure, or scattering as it is with electron exposure. This allows high aspect ratio resist patterns to be produced (see figure 1), and means that there are no proximity effects as there are with electron exposure. On the other hand, the mask is fragile and may not be dimensionally stable, and the large divergence of conventional x-ray sources gives rise to image distortion if the mask or wafer is not flat.

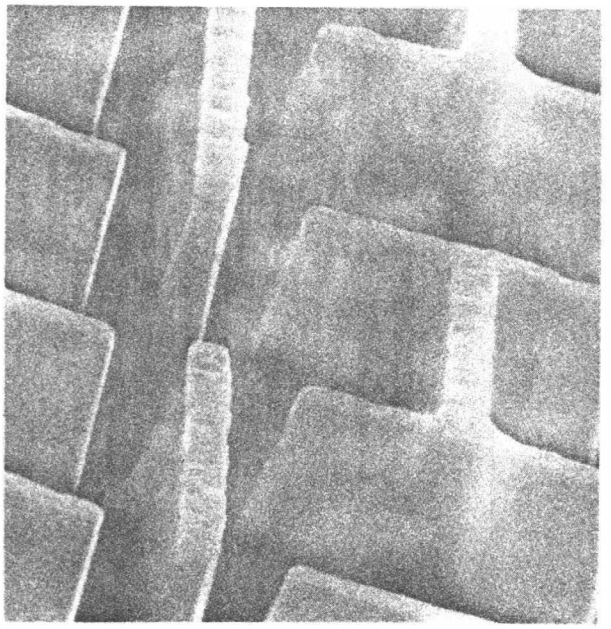

Figure 2. High aspect ratio pattern in PMMA resist obtained by x-ray lithography (Spiller *et.al.*, J. de Physique, 1978, to be published). 1μ linewidths.

A step and repeat x-ray approach in which the mask size is limited to the maximum "stable" area (this area can be set by mask and/or wafer instabilities) overcomes the problems of mask stability and source divergence, but exposure time with present resists and sources becomes excessive. A synchrotron storage ring (6) with a circulating current of at least tens of milliamps is a bright enough source to reduce exposure times to an acceptable level, but its great cost and overcapacity makes it difficult to utilize efficiently. The most satisfactory solution to this set of problems would appear to be the development of a compact and relatively inexpensive high output soft x-ray source, or a significant improvement in resist sensitivity. Recent experiments using x-rays from laser produced plasmas (7) offer some hope for the former. For the latter, it must be remembered that sensitivity has to be defined in terms of the resist (wall) profile and the acceptable thickness loss in the resist areas that remain after development (8). These requirements generally become more stringent for smaller dimensions, and resist processes that have been adequate for larger dimensions may no longer be useful. Resists that have proved to be satisfactory for 1μ device fabrication do not have adequate sensitivity for the step and repeat approach unless a storage ring is used as the x-ray source.

The alternative to the step and repeat approach is the original concept of full-wafer printing. Here a resilient substrate with adequate dimensional stability must be found. The formidable technological challenges must also be met of controlling temperature stability and sample and mask chucking forces to the point that 2 ppm overall dimensional repeatability (0.2 μ over 10cm) is achieved. Many laboratories are concentrating their efforts on these problems which enhances the likelihood of their being resolved.

Experimental results already indicate that alignment of mask and wafer should be possible to better than 0.1 μ (9).

1X SCANNING OPTICAL PROJECTION

1:1 optical scanning projection systems use the same masks and resists as contact printing, but they improve yield greatly by keeping mask and wafer separated. They also utilize master masks and thus dispense with the need for working masks. Throughput is high and approaches one hundred 8 cm diameter wafers per hour in some instances (10). Resolution at present is adequate for 3μ linewidths, and new systems promise improvement to 2 μ or below. Overlay accuracy is predicted to improve from ± 1 μ -1.5 μ to $\pm$ 0.25 μ.

In the new systems (11) tighter tolerances are met in the fabrication of optical components, temperature control is improved, and deep UV (λ = 2000Å-2600Å) radiation may be used, rather than conventional wavelengths (λ = 3000Å-4000Å).

1X scanning systems are full-wafer exposure systems and will encounter severe overall dimensional stability problems as dimensions approach 1 μ. The numerical aperture of the mirror imaging system will also have to be increased from the present value of 0.16 to about 0.3, and even with partially coherent illumination, depth of field will become very small. This may be intolerable because it will be very difficult to adjust focus and level the sample for different portions of the sample surface.

STEP AND REPEAT REDUCTION PROJECTION

Step and repeat reduction projection cameras offer the same yield advantage as 1:1 scanning projection plus a demonstrated improvement in resolution. High quality lenses have been made which achieve diffraction limited resolution at a numerical aperture of 0.34 N.A. (60% contrast for 1.25 μ lines) over a field of 1 cm x 1 cm (12). Advances in the design of illumination systems allow similar fields to be exposed in less than 0.5 sec (see for example (13)). When such an illumination system is combined with a high speed interferometrically controlled table,

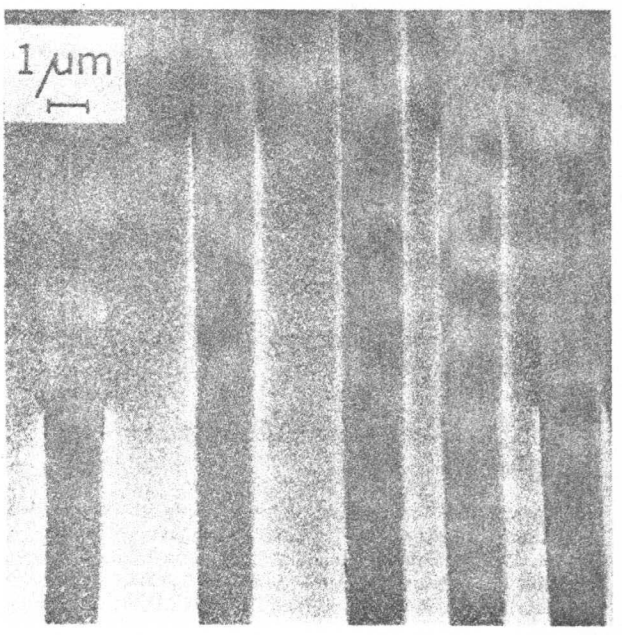

Figure 3. 1.25μ linewidths in resist produced by 5X projection camera (Wilczynski, J.S., Tibbetts, R., Lin, B.J., and Santy, W., IBM Research, Yorktown Heights, N. Y.).

throughputs of 50 75mm diameter wafers per hour can be obtained (14). Throughput has previously been considered to be too low for many applications.

As already mentioned, a major difficulty with any optical system at resolutions below 2 μ is the very small depth of field. In the step and repeat case, however, focusing and wafer leveling can be carried out at every chip site and the problem more readily contained than with the full wafer scanning systems. Even with this adjustment resist processes have to be very closely controlled and multi-level resists in which the imaging layer is kept thin will be particularly advantageous.

Alignment can be carried out once per wafer, as with 1:1 scanning systems, or preferably at every chip site. In the first instance laser interferometry is relied upon to maintain alignment and overlay accuracy of ± 0.5 μ should be achievable. In the second case improvement to $\pm$ 0.25 μ should be possible.

Although the resolution (see figure 3 and reference 15), throughput and overlay accuracy are very encouraging for step and repeat cameras, full complexity LSI devices with dimensions below 2 μ have yet to be fabricated. The most serious unknown is the ability to maintain pattern fidelity on rough surfaces.

SCANNING ELECTRON BEAM

This is the only method used so far to successfully make full-complexity silicon devices with a capability that exceeds conventional contact printing in terms of linewidth and overlay tolerance. See, for example, devices described in references (16) and (17). Full lithography capability has been established for 0.6 μ dimensions as is shown in figure 4.

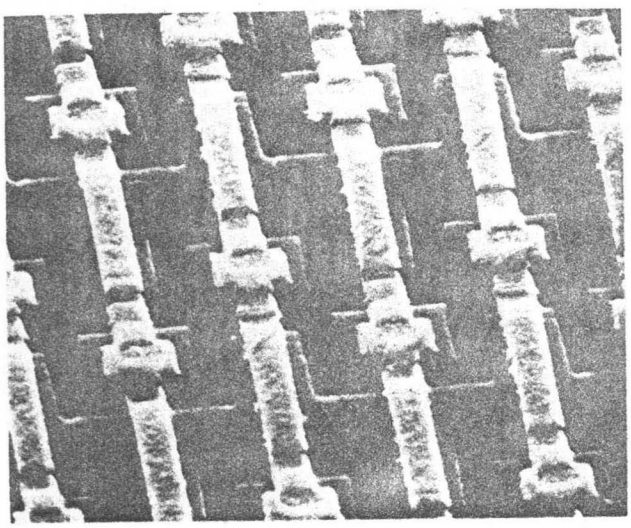

Figure 4. 0.6μ gate length F.E.T. test chip fabricated by VS-1 scanning electron beam system (Chang, T.H.P., *et.al.*, Proc. 7th Internat. Symp. Electron Ion Beam Sci. Technol. (Electrochem. Soc. Princeton, N.J., p. 392, (1976).)

Masks made by a scanning electron beam are also needed for replication methods such as x-ray lithography and deep UV conformal printing.

For conventional masks, scanning electron beam systems offer better resolution, lower defect levels, and quicker turn-round than conventional mechanical pattern generation techniques (18-21). Higher throughput electron beam systems can generate several master masks for 8 cm diameter samples in less than 1 hour, whereas it can take several hours to generate the reticule alone with standard methods. This reticule then has to be stepped and repeated in a reduction projection camera to produce a master mask. The quick turn-round of scanning electron beam fabrication has also been used to advantage in the direct-write mode for custom interconnection of integrated circuits (22).

Although scanning electron beam systems have proved themselves in the fabrication of devices, they are not yet cost competitive with optical approaches for the direct fabrication of most LSI devices. Nonetheless, their performance in this respect is improving rapidly. The improvement is due to the introduction of advanced electron optical design methods (23) and concepts (for example, the variable shaped beam concept (24,25)), higher speed electronics, and large reductions in the cost of the digital control electronics. Efforts are also being made to evolve optimum system architectures. In particular, the possibility of minimizing overhead times spent on mechanical sample movement and registration has become apparent through a combination of large area two dimensional electronic scanning, vector pattern addressing, and a fast variable speed mechanical table. The table would be moved under the control of a laser interferometer without interrupting the pattern writing process (26).

Resolution in electron beam fabricated structures is not ultimately set by the resolution of the electron optical system, but by electron scattering in the image-forming layer (resist), and by electron backscattering from the substrate. These scattering phenomena also give rise to proximity effects which make it necessary to adjust the exposure for different areas of the pattern. Experiments with automatic proximity effect correction indicate that correction is essential for dimensions below 1 μ and is of great value at 1.25μ (27, 17).

STEP AND REPEAT REDUCTION ELECTRON BEAM PROJECTION

In principle reduction electron beam projection systems (28,29) are very much more efficient than scanning systems because millions of resolution elements are projected simultaneously. They are also simpler because pattern data are stored in a mask rather than fed on-line to the system during each exposure. Electron optical projection columns have been built which operate according to their design specification, but fundamental problems remain with the mask and with distortion in the projected image.

The difficulty with the mask is that there is no available substrate that is adequately transparent to electrons, so the mask must either be self-supporting or be a patterned photocathode. Thin metal foil masks have been fabricated and methods found to overcome the problem that certain areas of the pattern are unsupported; but adequate dimensional stability has not been demonstrated, nor have full complexity LSI masks been made. Photocathodes have relatively low electron brightness and would greatly increase exposure time over a thin foil mask illuminated with a high brightness electron beam. The electron optical system used to accelerate electrons from the photocathode surface has also been shown to increase pattern distortion (29).

Distortion control has proven difficult over the large fields (10,000 times the minimum linewidth) needed to give these

systems higher throughput than scanning systems. As with any step and repeat approach, the throughput of a reduction projection system will depend to a large extent on the time taken to mechanically step the sample and to register the pattern to the sample. With scanning systems writing is already becoming comparable to these overhead times For projection systems to be faster, therefore, shorter exposure time is not adequate, the field size must also be larger so that the step and register sequence does not have to be performed so frequently. Field size for an optimum 4X projection system has been estimated to be 2cm x 2cm for 1μ minimum linewidth (25). This is considerably higher than the maximum of about 0 5cm x 0.5cm predicted for scanning systems at the same resolution. Exposure time can be less than a second but distortion will be $\leq$ 0.5%. Scanning systems with dynamic distortion correction achieve 0.0003% distortion. The relatively high distortion of the projection system may be tolerable for microcircuits provided all exposures are made on a single system, but it will preclude system to system compatibility, or the possibility of combining this method with other lithography techniques

Electron beam proximity effects are difficult to compensate with any full-pattern electron beam projection systems. Correction will have to be made by preadjusting the shapes in the mask because it will not be possible to adjust the electron charge per unit area from point to point in the image, as can be done with scanning electron beam systems.

1.1 PHOTOCATHODE ELECTRON BEAM PROJECTION

This approach offers the resolution and depth of field of electron optics together with the parallelism and simplicity of proximity printing Problems with the lifetime of the patterned photocathode delayed progress for many years but the introduction of cesium iodide as the photoemitter largely removed this problem Successful methods for aligning the projected image to the sample have also been developed The problems that remain are pattern distortion, reduction of image contrast because of backscattered electrons being returned to the sample surface, and correction for proximity effects

The sample is part of the electron optical system, and distortion is introduced if it is not absolutely flat Calculations show that a 30μ wafer bow will introduce a 1μ error in pattern position (30) Electrostatic wafer chucking is being applied to solve this problem So far 2μ LSI devices have been successfully made with a 1 1 electron beam projector, and it is predicted that 60 10cm diameter wafers can be exposed in one hour (30) For dimensions below 1μ, the dimensional stability required to satisfy overlay requirements will become extremely severe

Demonstration of a method for correcting proximity effects by adjusting the shapes in the mask has been reported (30)

OVERALL COMPARISON

Figure 5 shows five ways in which the various lithography methods can be combined to produce microcircuits The first is the historically established route the others are the methods most likely to appear in the future Their relative success will obviously depend on requirements for device performance, cost and volume A key factor will be the ratio of lithography cost to overall wafer cost If overall wafer cost is high, then changing from a low resolution low cost lithography to a higher resolution higher cost approach may well reduce overall cost per device by increasing density. It is likely that combinations of the different approaches, for example, 2 and 4, may also prove optimum under some circumstances.

Approximate estimates of comparative cost per resolution element for some of the different exposure systems are given in table II A resolution element is defined as a pattern square one minimum linewidth on the side. The numbers in brackets in the system column are predictions of field size, minimum linewidth and exposure time per field (including overheads such as sample loading, mechanical stepping, and registration), that may be achievable in the future. In all cases a large degree of uncertainty is involved. Electron beam and x-ray systems can readily reach dimensions below 1μ, but, in general, field size will be reduced and resolution elements per field will remain approximately equal.

In order to obtain the cost factor, the following capital costs were assumed: 1:1 scanning optical projection -- $200k; S/R reduction optical projection --$500k, scanning electron beam $1500k, x-ray full field $250k, x-ray step and repeat $500k (this could be the cost of one port on an electron synchrotron storage ring) $1250k, 1:1 electron beam projection. Capital cost was distributed over five years and operating costs adjusted over a small range according to system complexity. One operator at a cost of $50k per year was assumed for each system.

According to table II, a cost penalty will be incurred for all but one of the advanced approaches. This cost penalty will have to be accounted for by increased density, higher yield, improved device performance, or on the basis of a logistical or cost advantage arising from the elimination of masks.

REFERENCES

1 Broers, A.N., Instit. of Phys. Conf. Series 40 (Instit. of Phys. London), p. 155, (1978).
2 Lin, B.J., J. Vac. Sci. & Technol., 12, p. 1317, (1975)
3 Smith, H.I., Rev. Sci. Instr., 40, p. 729, (1969).
4 Spears, D.L. and H.I. Smith, Electron Lett., 8, p. 102, (1972)
5 Spiller, E , and R. Feder, "X-ray Lithography," Chap. 3 in X-ray Optics, Ed. H.J. Queisser, Springer, Berlin (1977)
6 Spiller, E , *et. al* , J. Appl. Phys., 47, p 5450, (1976)
7 Peckerar, M C , *et. al.*, Proc. 8th Internat. Conf. on Electron and Ion Beam Sci. Technol. (Electrochemical Soc Princeton, N J USA. To be published 1978.
8 Hatzakis, M., J Vac Sci. and Technol., 12, p. 1276, (1975)
9 Flanders, D , *et al*, Appl. Phys. Lett., 31, p. 426, (1977)
10 Markle, D A., Solid State Technol., p. 50, (June 1974).
11 Offner, A , SPSE 31st Annual Conf., J. Appl. Phot Eng , (May 1978). Proc. to be published
12 Wilczynski, J S and R., Tibbetts, Unpublished (1976) See also Wilczynski, J.S , and R. Tibbetts, IBM J. Res. Develop , 13, p 192, (1969).
13 Roussel, J., Sol State Technol., p. 67, (May 1978).
14 Tobey, W , Electronics, 50, p. 115, (Aug 1977).
15 Hugues M , *et.al* , Proc Internat. Conf. on Microlithography, Paris, p 71, (1977).

16. Yu, H N., *et al*, J Vac Sci Technol., 12, p 1297, (1975)
17. Reisman, A., *et al*, and W D Grobman, *et.al*, (1978) This Proceedings
18. Varnell, G., *et al*., Proc 6th Internat Conf on Electron and Ion Beam Sci and Technol., Ed., R Bakish, Electrochemical Soc., Princeton, N J., p 97, (1974)
19. Beasley, J.P., and D G Squire, IEEE Trans on Electron Devices, ED-22, p 3, (1975)
20 Herriott, D R., *et al*, IFFE Trans on Electron Devices ED-22, p 399 (1975)
21. Ting, C H., *et al*., J Vac Sci Technol., 15, p 948, (1978)
22 Yourke, H S., and F V Weber, Proc Internat. Electron Devices Conf., Washington, D C., p. 431, (1976).
23 Munro, E., Optik, 39,p. 450, (1974).
24 Pfeiffer, H C., J Vac. Sci. Technol., 15, p. 887, (1978).
25 Goto, E., *et al*., J. Vac Sci. Technol., 15, p 883, (1978).
26. Wilson, A D., *et.al*, Proc 8th Internat. Conf on Electron and Ion Beam Sci and Technol., (Electrochemical Soc. Princeton, N.J., USA). To be published (1978).
27. Parikh, M., J. Vac. Sci Technol. 15, p. 931, (1978)
28. Heritage, M B., J. Vac. Sci. Technol., 12, p. 1135, (1975).
29. Lischke, B., *et al*., Proc Internat. Conf on Microlithography, Paris, p 163, (1977).
30. Scott, J.P., J. Vac. Sci. Technol., 15, p. 1016, (1978).

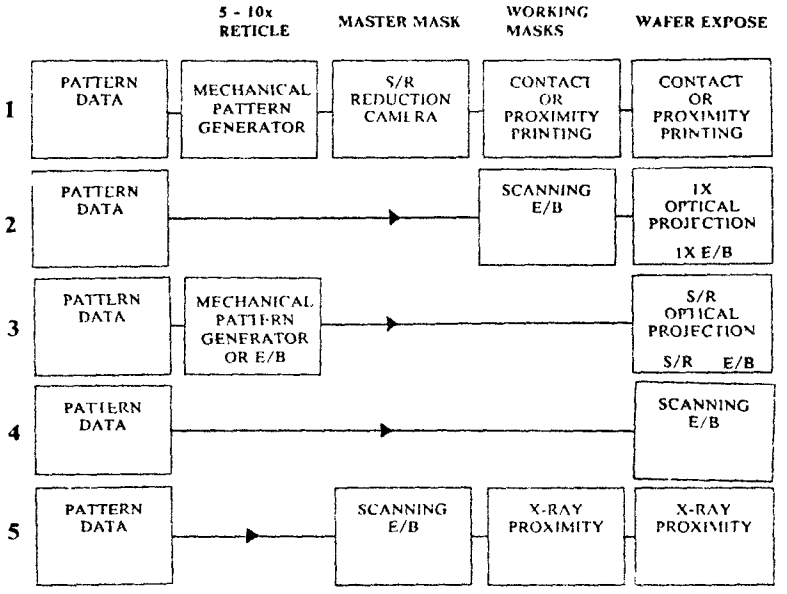

TABLE 1

Alternative methods for employing new lithography approaches in the manufacture of microcircuits

SYSTEM	PATTERN ELEMENTS PER SECOND	COST FACTOR	COST PER PATTERN ELEMENT (NORMALIZED TO F F OPTICAL PROJECTION)
FULL-FIELD OPTICAL PROJECTION (70cm², 2μ, 75 Sec)	7×10^7	1	**1**
STEP/REPEAT OPTICAL PROJECTION (1cm², 1.5μ, 1 Sec)	4.4×10^7	1.5	**2.4**
SCANNING ELECTRON BEAM (0.16 cm² 1μ, 1 Sec)	1.6×10^7	4	**11**
X-RAY FULL FIELD (70 cm², 1μ, 200 Sec)	3.5×10^7	1.2	**2.4**
X-RAY STEP REPEAT (1 cm², 1μ 10 Sec)	10^7	2	**14**
1:1 ELECTRON BEAM PROJECTION (70 cm², 1μ, 60 Sec)	7×10^8	3	**0.3**

IGNORING YIELD, TURN-AROUND TIME, MASK COST, OVERLAY ACCURACY, SYSTEM AVAILABILITY DATE, ETC

TABLE 2

Approximate estimates of comparative cost per resolution element for several lithography systems

GaAs INTEGRATED CIRCUITS: MSI STATUS AND VLSI PROSPECTS*

Richard C. Eden

Rockwell International/Science Center
Thousand Oaks, California 91360

ABSTRACT

The very high electron mobility of GaAs, aided by the use of semi-insulating GaAs substrate material, makes possible the achievement of very high switching speed ($\tau_d < 100ps$) integrated circuits which can simultaneously exhibit very low dynamic switching energies ($P_D\tau_d < 100fJ$). Planar GaAs circuits of this performance have already been demonstrated. Such circuits, with $< 1000\mu m^2$ gate areas, open the way to an extremely high performance, very dense, low power VLSI technology. It is the purpose of this paper to summarize the reasons why GaAs is so attractive for high performance ICs, to review the present status of GaAs IC development efforts and their results for MSI and upper MSI (near LSI) circuits, and to explore the prospects for the extension of this technology into the VLSI regime.

INTRODUCTION

Since the principal advantage of GaAs is its high electron mobility, a feature best exploited in a majority-carrier device technology, it is hardly surprising that most GaAs integrated circuit efforts have been based on the use of N-channel FETs of various types. Fig. 1 gives an overview of the various device and circuit technologies under investigation for GaAs FET digital integrated circuits. Some of the development history of GaAs integrated circuits is discussed in Ref. 1. The first GaAs digital IC's developed were of the buffered-FET logic type,[2,8,9] principally because they used the same depletion-mode MESFET device and mesa fabrication technologies developed for discrete microwave GaAs FETs. While the $\tau_d < 100ps$ switching speeds attained with $L_g = 1\mu m$ MESFET geometries in this approach are excellent, the P_D = 20 to 40 mW gate dissipations limit the chip complexities to MSI levels. It was the desire to reduce this gate dissipation, as well as to achieve simpler, single power supply, higher density circuits that motivated the efforts in enhancement-mode FET logic. The logic circuit approach used is principally simple direct-coupled FET logic, (DCFL) with normally-off FETs and resistor loads (depletion-mode loads should be superior but have not been implemented thus far). The work here differs principally in the type of enhancement-mode GaAs FET used. The most complex DCFL circuits have been achieved using E-MESFETs, with $\tau_d \sim 400ps$ speeds with extremely low ($< 100fJ$) $P_D\tau_d$ products attained in SSI sequential logic circuits. Individual logic gates and inverter ring oscillators using E-JETs have also been fabricated.[5] In these approaches, the onset of gate conduction limits the available logic voltage swing, which places stringent requirements on the FET threshold control and also significantly limits the attainable switching speeds (Fig. 3). The use of heterojunction gate or insulated-gate (MOS or MIS) GaAs FET devices could improve this situation, but the work on such devices is at a very preliminary, discrete FET state.[6,7] Another approach for achieving high-density, low-power GaAs FET IC's involves the use of high speed Schottky diodes for most logic functions, with low power depletion-mode MESFETs used for inversion and gain.[10] This Schottky diode-FET logic (SDFL) approach achieves speeds ($\tau_d \sim 100ps$) close to those of BFL at much lower ($P_D \sim 200\mu W$ to 2 mW/gate) power levels, which makes the achievement of much higher complexity chips possible. SDFL does, however, require a more sohpisticated fabrication approach in order to optimize both diodes and FETs.

IC PERFORMANCE ANALYSIS: COMPARISON OF GaAs AND SILICON

While the performance results achieved for GaAs IC's have been outstanding, there has been some disagreement about these results, with some people in the IC community ascribing them principally to the 1 μm geometries and semi-insulating substrates used in GaAs IC work, rather than to superior GaAs electronic properties and FET characteristics. This "mobility versus saturation velocity" argument is based on a difference in view of what are the appropriate approximations to use in the equations describing FET operation. In an FET, the gate voltage above pinchoff, $V_{gs} - V_p$, controls both the charge in the FET conduction channel, Q_c, and the average electric field, $\mathcal{E}_c$, controlling the motion of that charge. In the "mobility" view, exemplified by the Shockley model of the FET, the carrier drift velocity is assumed proportional to field, $v_d = \mu_n \mathcal{E}_c$, so that both Q_c and v_d are

*This work was supported, in part, by the Defense Advanced Researsh Projects Agency of the Dept. of Defense and was monitored by the Air Force Office of Scientific Research under Contract No. F49620-77-C-0087.

proportional to $V_{gs} - V_p$, giving a square-law saturated drain current, I_{DS}, characteristics;

$$I_{DS} = K(V_{gs}-V_p)^2 \qquad (1)$$

The constant K depends on the electron mobility in the channel, μ_n, the dielectric constant of the depleted semiconductor (MESFET or JFET) or insulator (MOSFET) separating the gate and channel, ϵ, the gate to channel separation, a, the gate length, L_g, and channel width, W as

$$K = \frac{\epsilon \mu_n W}{2 a L_g} \qquad (2)$$

Hence, in this model, the transconductance is given by

$$g_m = \frac{\epsilon \mu_n W}{a} (V_{gs} - V_p) \text{ [Shockley]} \qquad (3)$$

In the other extreme of viewpoint, if the control field in the channel, $\mathcal{E}_c \simeq (V_{gs} - V_p)/L_g$, is high enough at bias voltages of interest so that the electron velocity reaches saturation, i. e., $v_d = v_s$, then only Q_c will vary with $V_{gs} - V_p$, and the transconductance will be given by

$$g_m = \frac{\epsilon v_s W}{a} \quad \text{[Velocity Saturated]} \qquad (4)$$

(presumably valid for $\mu_n(V_{gs}-V_p)/L_g > v_s$). Inasmuch as the electron mobility in GaAs (μ_n=4000 cm^2/Vs at $N_d = 2 \times 10^{17}$ cm^{-3}) is nearly an order of magnitude higher than typical silicon NMOS channel mobilities at reasonably high charge densities, while the bulk electron saturation velocities for GaAs and silicon are similar ($v_s \simeq 10^7$ cm/s), Eq. 3 and 4 lead to vastly different estimates of the value to be gained by using GaAs rather than silicon in FETs.

The most definitive way of resolving this issue is to compare actual experimental data on short-channel GaAs and silicon FETs. Plotted in Fig. 2 are the I_{DS} versus $V_{gs} - V_p$ characteristics for L_g = 1μm MESFETs of GaAs and silicon, both normalized to W = 10μm channel widths. The GaAs MESFET data is for planar, double-implanted IC-type devices[1] as shown in Fig. 5, while the silicon data is for L_g = 1μm microwave MESFETs[11] of the type described in Ref. 12. The I_{DS} versus $V_{gs} - V_p$ characteristics are more or less parabolic (Eq. 1), linearizing somewhat at higher $V_{gs} - V_p$ values. The important thing to note is that for any given $V_{gs} - V_p$ bias, the saturated drain current and transconductance values for the GaAs MESFET are at least 6 times larger than the values for the silicon MESFET. These superior transconductance characteristics are also reflected in greatly superior microwave properties (gain, noise figure, etc.) for GaAs MESFETs. Note that while for accuracy of comparison a silicon MESFET is shown in Fig. 2, nearly identical characteristics to these are obtained with L_g = 1 μm silicon NMOS devices.[13]

Granted that real GaAs MESFETs give much better performance characteristics, particularly at low biases, than silicon FETs, the key question is what influence will this have on the on the speed and switching energies of logic circuits made with these devices? While there are many details and variants in logic circuits, a very general analysis can serve to establish overall trends and limitations of real circuits. If we consider an approximately square law switching FET with current source active load switching between hard limits at threshold, $V_{gs} = V_p$, and $V_{gs} = V_p + V_m$, where V_m is the logic voltage swing, and assume an optimized load current of $I_{dm}/2$, where I_{dm} is the peak FET drain current (I_{DS} at $V_{gs} = V_p + V_m$), then the logic propagation delay with a load capacitance C_L can be shown to be

$$\tau_d = \frac{4 C_L V_m}{3 I_{dm}} \quad \text{[Propagation Delay]} \qquad (5)$$

If we take a supply voltage of $V_{DD} \sim 1.7V_m$, the worst-case dynamic switching energy will be

$$P_D\tau_d = \frac{9}{8} C_L V_m^2 \quad \text{[Speed Power Product]} \qquad (6)$$

(about twice the 1/2 $C_L V_m^2$ stored energy in the load capacitance). Eq. 6 gives a direct relationship between the logic swing, V_m, and the $P_D\tau_d$ product for any given load capacitance, C_L, independent of FET type. The I_{DS} versus $V_{gs} - V_p$ FET characteristics (which is the same as I_{dm} versus V_m in Eq. 5) do determine the propagation delay for any given V_m, however. Taking the silicon and GaAs MESFET characteristics of Fig. 2, and assuming a C_L = 30ff load capacitance (reasonable for small circuits with insulating substrates such as GaAs or silicon on sapphire), we obtain the switching speed and dynamic switching energy relationships shown in Fig. 3. We note in Fig. 3 that for any given logic voltage swing (or $P_D\tau_d$ product) the GaAs MESFET IC will be over 6 times faster than the silicon MESFET circuit. On the other hand, if we demand equal propagation delays from both circuits, the GaAs device can achieve the speed with much smaller logic swings and hence enormously lower speed-power products than the silicon IC. This is, of course, extremely important for high speed VLSI applications.

GaAs IC RESEARCH: PRESENT STATUS

Fig. 4 shows a propagation delay versus power dissipation map for various GaAs IC approaches, along with approximate areas for other logic technologies. Some of the general features of these results can be understood in terms of the foregoing simple analysis, considering the logic swings, V_m, involved in the different GaAs FET logic approaches (as noted in the chart in Fig. 1). For example, as predicted from Fig. 3, the low logic swing, enhancement-mode circuits give excellent $P_D\tau_d$ products, but at significantly slower speeds than the depletion mode GaAs MESFET circuits. In general, all the GaAs IC approaches give much lower powers at any given speed than a silicon IC technology with comparable lithographic dimensions. Note that it is important to compare switching speeds of different technologies at the same lithographic dimensions (gate lengths). For example, while L_g = 1μm GaAs ICs fabricated

with optical lithography give $\tau_d \sim 75$ps speeds in SDFL or BFL circuits, E-beam fabricated $L_g = 0.5\mu m$ simple BFL inverter chains have, as would be expected, attained $\tau_d = 34$ps propagation delays[15] (at $P_D = 41$ mW power levels).

The performance attained with these GaAs integrated circuits have been excellent. However, the most serious concerns about the future of GaAs, particularly for LSI and VLSI applications, are focused on the questions of fabricability and yield. On the basis of silicon IC experience it seems unlikely that LSI circuit complexities could be achieved with mesa GaAs IC fabrication approaches. In addition, the single layer (epi or uniform implant) available with these approaches also results in some restrictions in circuit approach. More recently, a fully planar GaAs IC process making use of multiple localized implantations directly into a semi-insulating GaAs substrate has been developed[16,1] which avoids these problems. Because the multiple implantation steps make it possible to optimize more than one type of active device with this process, it has been extensively used to fabricate circuits of the Schottky diode-FET logic (SDFL) type.[1,10]

The attainment of LSI or VLSI circuit complexities in high speed logic requires low gate dissipations and hence ultra low $P_D\tau_d$ products. As indicated in Fig. 3, this implies relatively low logic swings with relatively low pinchoff voltage MESFETs, if depletion-mode logic is used. The FET pinchoff voltage, of course, must be controlled to a small fraction of the logic swing, the achievement of which has proven quite difficult in GaAs MESFETs, due to the extremely thin (~ 1000Å) active layers involved. Also, the MESFET drain currents must be reasonably well matched for optimum circuit function. Fig. 6 shows a statistical correlation plot of I_{DSS} versus V_p for 72 (of 72 fabricated) $W = 50\mu m$, $L_g = 1\mu m$ planar, double-implanted low power MESFETs from one of our GaAs IC wafers. The $\sigma_{V_p} = 70$mV standard deviation in V_p is excellent and the $\sigma_{I_{dss}} = 350\mu A$ standard deviation in I_{dss} is just a reflection of σ_{V_p} and the -5mA/V best linear fit to the data (which value also equals the FET transconductance). The very low ($\sim 70\mu A$) standard deviation of I_{DSS} relative to this linear fit attests very well to the uniformity of process parameters (gate length, alignments, ohmic contact resistances, etc.). Considering that these are $L_g = 1\mu m$ circuits fabricated with projection optical lithography, this is quite remarkable. Note that if we consider the FET channel to have a constant, $N_D = 2 \times 10^{17}cm^{-3}$, donor doping density over a thickness a_o, for this pinchoff voltage, a_o would be about 1100Å. The observed $\sigma_{V_p} = 70$ mV standard deviation in pinchoff would be accounted for by a $\sigma_{a_o} = 22.5$Å standard deviation in this layer thickness. Keeping in mind that this 22.5Å variation is only 4 GaAs lattice constants, the difficulty of achieving this level of pinchoff control with epitaxy becomes obvious, and the power of ion implantation as a fabrication tool is amply demonstrated.

These low power ($V_pI_{DSS} < 500\mu W$ for $W = 10\mu m$), high transconductance, very uniform planar GaAs MESFETs are ideal for low power SDFL logic circuits. Fig. 7 shows the circuit diagram for a simple SDFL (positive) NOR gate. The key elements in the circuit, other than the D-MESFET switching FET and active loads, are the tiny ($\sim 1\mu m \times 2\ \mu m$), low capacitance ($C_j \sim 2ff$), high conductance ($R_s$ as low as 300 Ω) Schottky barrier switching diodes, with which most of the logic is performed. The principal advantages for this circuit approach are its extreme simplicity (for high yields), low gate areas (as low as $600\mu m^2$/gate[17]) and low power requirements ($P_D \sim 200\mu W$ to 2mW/gate) for LSI or VLSI compatibility, combined with the high switching speeds ($\tau_d \sim 75$ to 150ps) of depletion mode GaAs MESFET logic. In addition, SDFL ring oscillators have been operated at temperatures up to 200°C with little change in propagation delay.[18] The dynamic switching energies attained with these SDFL circuits, $P_D\tau_d$ at low as 27 fJ (at $\tau_d = 156$ps) are close to the lowest values achieved in enhancement-mode GaAs logic circuits, but at considerably higher speeds.

Fig. 8 shows an SEM picture of a portion of a D-flip flop containing two SDFL NOR gates of the type shown in Fig. 7 and associated interconnects. The very clean, uniform lithography on the $L_g = 1\mu m$ MESFET gates and 1 μm diode metalizations is an excellent indication that state-of-the-art projection optical lithography is indeed capable of handling 1 μm feature size LSI and VLSI circuits. Fig. 9 shows a chain of 3 of these SDFL D-flip flops in a ÷8 ripple counter configuration. Other MSI circuits fabricated with this planar GaAs IC process and successfully tested include a more complex 3 stage synchronous binary counter and a complete 8:1 data multiplexer which used the synchronous counter as an address generator; this part has a 64 gate complexity. These SDFL MSI circuits are significantly more complex than the ~ 20 gate MSI parts demonstrated with BFL[2,9] or the ~ 8 gate SSI ÷ 2 circuit fabricated with enhancement-mode MESFET logic.[4] The principal factor limiting the achievement of higher chip complexities with the BFL depletion-mode MESFET circuits is the high gate dissipations, while the enhancement-mode MESFET work would appear to be hampered by the difficulty of achieving the required FET threshold uniformities with acceptable yields.

PROJECTIONS FOR THE FUTURE

Perhaps the most important point to be conveyed here is that GaAs integrated circuits are for real; they offer real speed and power performance advantages over silcon integrated circuits and it seems reasonable to expect that before long they will be playing key roles in electronic systems. While important applications