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大学电子信息科学与技术英汉实验丛书

数字电路实验

王怀登　陈孝桢　编著

南京大学出版社

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编 委 会

序

为了培养高质量的人才，在高等学校的教学计划中，应该充分重视实验课的设置，并把课程的各个环节抓紧、抓好。尤其在本科生阶段，更要让学生接受全面的训练，从常见仪器的使用、基本量的测量，到按照一定的要求搭建系统以满足特定的性能指标，到有意地探寻和隔离非主要因素、探寻和突出主要因素，并观察其对于最终结果的影响。这样，由易而难、由简单而复杂，环环相扣、步步升高，教学工作才能扎实有效。

南京大学电子科学与工程学院李元教授长期从事电子技术教学工作，对于实验教学一向十分重视。他转往南京大学金陵学院后，一度执掌全院教务处和信息科学与工程学院的领导岗位。在他的带领下，陈孝桢教授、吴宗森教授、王均义教授、沈一骑高工、何菁博士等一批在大学电子信息科学与技术领域内有重要影响的专家学者齐心协力，先后开设了模拟电路实验、数字电路实验、电工学综合实验、通信原理实验、嵌入式系统实验、大学物理实验等课程，并编写了相应的教材，集结为丛书。经过多年的使用和实践，证明这些课程和教材在基础的层面上恰如其分地反映了学科发展的趋势，符合当前学生的实际，对于培养学生的独立工作能力发挥了很好的作用，也得到了国内同行的高度认同。

这些课程和教材也吸引了国外同行的注意，有英国 ESSEX 大学、法国勒芒大学、加拿大罗里尔大学、日本北海道情报大学等学校主动要求交流。可惜，由于教材原来都用中文写成，语言的障碍使有关部门无法把这些教材送往国外，或者送出后没有起到其应有的作用。与此同时，随着学校国际化程度的日益提高，在学生这一层面上的涉外活动也不断增多，要求学校在关心学生能否通过四级或六级英语考试的同时，注意加强对他们专业英语能力的培养。

这样，李元等教授就萌发了一个想法，将原有的实验教材进行重新整理、出新，并进行初译，然后交由吴宗森教授、加拿大罗里尔大学 Sturtevant 教授进行英语文字上的加工与译审，使之成为英汉实验丛书，正式出版以飨国内外广大读者。

我很高兴地得知，经过有关教授一年多的努力，这套英汉实验丛书即将完成，并陆续付印。希望这套丛书的出版，对于培养我国电子信息科学与技术领域的专门人才、对于促进国际交流都能有所裨益。

南京大学教授
中国科学院院士
2013. 12

PREFACE
前 言

The electronic and informational age is upon us. With the rapid development of electronic science and technology, the digital circuit designed by EDA software has become a popular trend. Consequently, the digital circuit experiments in colleges and universities have to adapt and follow the changing. But in many colleges and universities, with different teams of teachers with different knowledge structure and different teaching idea, the traditional digital circuit experiments based on small and medium digital integrated chips (SSI and MSI) and CPLD/FPGA experiments are separated into two completely independent parts. In essence, the traditional digital circuit design and CPLD/FPGA design are toward for the same task, but with different approaches.

According to the above idea, we wrote the new textbook of "Digital Circuit Experiment" in which the traditional digital circuit experiments and CPLD/FPGA design experiments are combined as one unit. In the learning process, through timely contrasting and comparing, students will understand the advance of the modern digital system design deeply.

Since the total course hours are limited, the most digital circuit experiments in the textbook are chosen simpler ones, similarly, the corresponding experiments of CPLD/FPGA design are also entry-level. The further programming and design could be studied in further subsequent courses when needed.

Development software is an essential tool of CPLD/FPGA design. Because the CPLD experimental platform adopts CPLD of Xilinx Company, we choose Xilinx ISE 12.3 as the corresponding software. When introducing the software based on the foundation, we present the basic development process of the CPLD/FPGA design in a clear and concise explanation. We omit the knowledge such as the complex timing simulation, the IP core using, and the SoPC establishment which may be encountered in the high-end FPGA design. Students could further learn them in the subsequent special course.

Verilog HDL is one of the main hardware description languages and is widely used in CPLD/FPGA design and integrated circuit design currently. Since it is derived from C and there are a lot of special books discussing the language and its grammar, it is relatively easy to learn and use. In the textbook of *Fundamentals of Electronic Technique (Digital)* edited by Kang Hua Guang, there is explanation for Verilog HDL

language and program in corresponding of the related hardware content in each chapter. Therefore, there is no longer on the tutorial of Verilog HDL language in this book. Students could refer to *Fundamentals of Electronic Technique (Digital)* edited by Kang Hua Guang and other books in the experiment.

The textbook is divided as two parts. The first part is the digital circuit experiments based on SSI and MSI, which are implemented on the bread board. The second part is the CPLD experiments, which are implemented on the CPLD experimental platform. The experimental contents are corresponding to each another.

There are following experiments in the first part:

In Lab 1, it is required to implement NAND gate in EWB and to understand the external electrical properties and characteristics of integrated circuit associated with its internal circuit through software simulation.

In Lab 2, it is required to construct a corresponding circuit for measuring the corresponding external electrical properties and characteristics of integrated circuit 74LS00.

In Lab 3, it is required to form a half adder, three-state gates and comparator and to understand the implementation process and their characteristics of combinational logic circuit.

In Lab 4, it is required to construct a counting decoding display circuit for displaying the count results on 7-segment display. By experiencing the experiment, students are able to understand the working process of the sequential logic circuit under the action of the clock, and also comprehend the difference between synchronous and asynchronous in sequential logic circuit through observing counting process. In the meanwhile, they are capable of knowing the different decoding methods and using occasions between common-cathode and common-anode display.

In Lab 5, it is required to be familiar with the hybrid device by means of several different circuits formed with timer 555 and to know their working principles and applications of two different trigging modes of the monostable multivibrator. Through the experiment, students should know why the timer 555 is so widely used.

Finally, Lab 6 (Design a Circuit of "Who Answered First"), Lab 7 (Design an Indicating Circuit for LED) and Lab 8 (Design and Assemble a Circuit Measured for Rectangular Wave Duty Cycle) are the comprehensive experiments which are designed to enhance and improve the design, test and debugging knowledge and skills for complex digital logic circuit.

Now let us turn to the second part. Lab 14, i. e. "Implement a Finite State Machine", is added into the part. The purpose is to explain the basic design method of state machine by means of a classical 110 sequence detection circuit. Because the CPLD experimental platform chosen in our laboratory does not have the required circuit

interface, three labs (Lab 1, Lab 2 and Lab 8) have no corresponding relationship in the two parts. The rest ones (Lab 3, 4, 5, 6 and 7) have corresponding ones. Each experiment make students know what the basic routines are. As they progress through the experiments one by one, students can find out that the basic routines in the texts are reduced and simplified, by contrast, they are inspired to implement the experiments by their own ideas. And finally students are able to implement the relative comprehensive logic circuits by themselves freely.

Because the experimental contents are more, in implementation of the experiment course, the contents could be omitted according to the total experimental hours. The circuits in the first part could be implemented on the bread board, and the circuit in the second part could be implemented on the CPLD experimental platform. The labs can be completed in order of the textbook, which means that students begin to do the labs in the first part and then the second part. And they also could be completed in the experimental contents, that is, one same experimental content in the first part and then in corresponding in the second part. The second arrangement of experimental course mentioned above may be gain better teaching effect.

Attached this textbook, there is an appendix which provides data sheets of the four chips used in the experiments. The data sheets of other chips used in the experiments could be found in http://www.21ic.com/. Learning how to read data sheet of the chip is a very important aspect. Reading the data sheet in pre-experiment carefully to learn and understand basic knowledge of function, performance, typical application and package type of the chip used in the experiment will be helpful to use the chip correctly and play its performance fully in the experiment, and also lay good foundation for future design and scientific research work.

Because this textbook is the first edition, somewhat in the book needs to be discussed or to be improved, and even some errors are existed accidentally. We welcome your comments, questions and suggestions.

Acknowledgements

Over the years many members of our college have given generously of their time to us for writing, editing and publishing this textbook. We owe special thanks to Prof. Yuan Li for his encourage and sharing his idea with us, and to Prof. Zongsen Wu and Terry Sturtevant for their proofreading.

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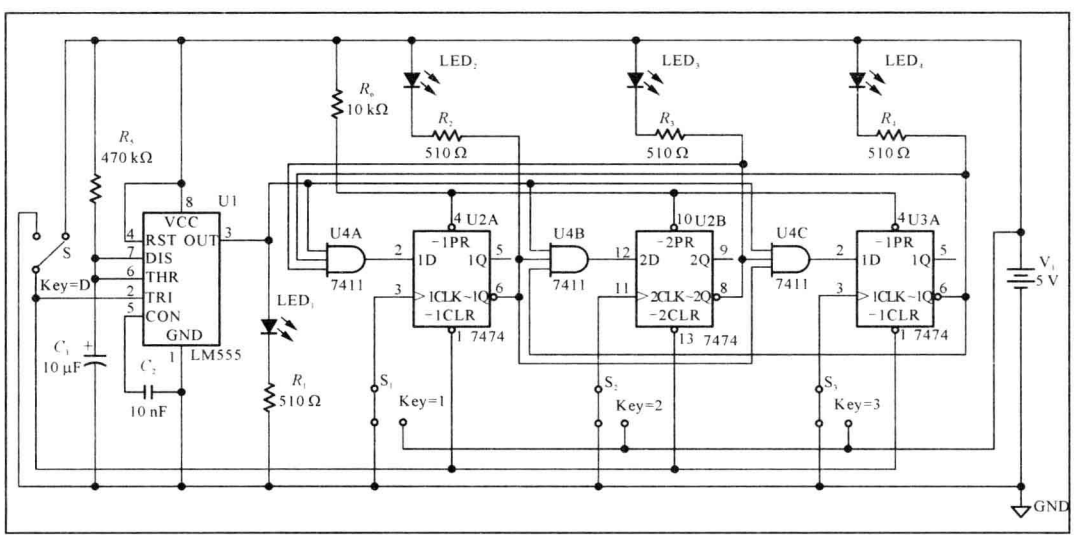
Part 2 Digital Circuit Implemented by CPLD

Part 1

Digital Circuit Implemented by Small and Medium Scale Digital Integrated Chips



Lab 1 Measure Electrical Characteristics of Integrated TTL NAND Gates (Simulation)
实验一 集成与非门电路电气特性测量(仿真)

Purpose

❶ Know that the electrical characteristics of an integrated circuit is determined by its internal circuit based on the simulation of circuits inside the TTL NAND gate.

❷ Know the electrical characteristics of the integrated TTL NAND gates by the measurements.

❸ Learn EWB circuit simulation.

Pre-lab

❶ Know how to do the circuit simulation by EWB.

❷ Know the internal circuit and electrical characteristics of the TTL NAND gate.

Apparatus

Computer and software EWB5.0.

Procedure

1. EWB simulation of TTL NAND gate

An internal circuit of a TTL NAND gate drawn with EWB is shown in Figure 1-1. The topology of the circuit is the same as that of the internal circuit of 74LS00. The resistances of the resistors in the circuit are also as same as those in the internal circuit of 74LS00. In 74LS00, some bipolar transistors are Schottky clamp bipolar transistors. Their input transistors are double emitter bipolar transistors. But there are no such elements in EWB, so in Figure 1-1, we use a set of diode 10BQ040 and bipolar transistor ZTX694B as alternative by using a Schottky clamp bipolar transistor, and diode D1X, D1Y, D2X, D2Y as alternative by using a multi-emitter bipolar transistor.

In EWB, the default parameters of diode 10BQ040 are as follows:

. MODEL 10BQ040 d IS = 2. 13126e − 05 RS = 0. 123203 N = 1. 53952 EG = 0. 600841 XTI=3. 78803 BV=40 IBV=0. 0001 CJO=1. 53747e−10 VJ=1. 5 M= 0. 476132 FC=0. 5 TT=0 KF=0 AF=1

And the default parameters of bipolar transistor ZTX694B are as follows:

. MODEL FZT694B NPN IS=1. 59E−12 NF=1. 001 BF=1009 IKF=0. 26 VAF= 45 ISE=. 253E−12 NE=1. 445 NR=1 BR=40 IKR=1 VAR=30 ISC=0. 326E− 12 NC=1. 075 RB=0. 2 RE=0. 065 RC=0. 075 CJC=35. 5E−12 MJC=. 465 VJC =. 515 CJE=258E−12 TF =. 763E−9 TR =130E−9

In order to simulate the results matched to 74LS00, we modify the parameters for the diode 10BQ040 and the bipolar transistor ZTX694B shown as Table 1 - 1. So that, the circuit shown in Figure 1 - 1 is only a simulation of the NAND gate, its electrical characteristics is not the same as 74LS00. In the simulation, if the parameters of elements in the circuit are changed, the electrical characteristics of the NAND gate would be changed.

Table 1 - 1 Modifications of parameters of diode 10BQ040 and the bipolar transistor ZTX694B

ZTX694B	IS	CC	CE
$Q_1 \sim Q_3$, Q_5	1. 59e−12	3. 55e−13	2. 58e−13
Q_4	6e−12	3. 55e−13	2. 58e−13

10BQ040	IS
the other diodes	1e−9
D1X, D2X, D1Y, D2Y	4e−7

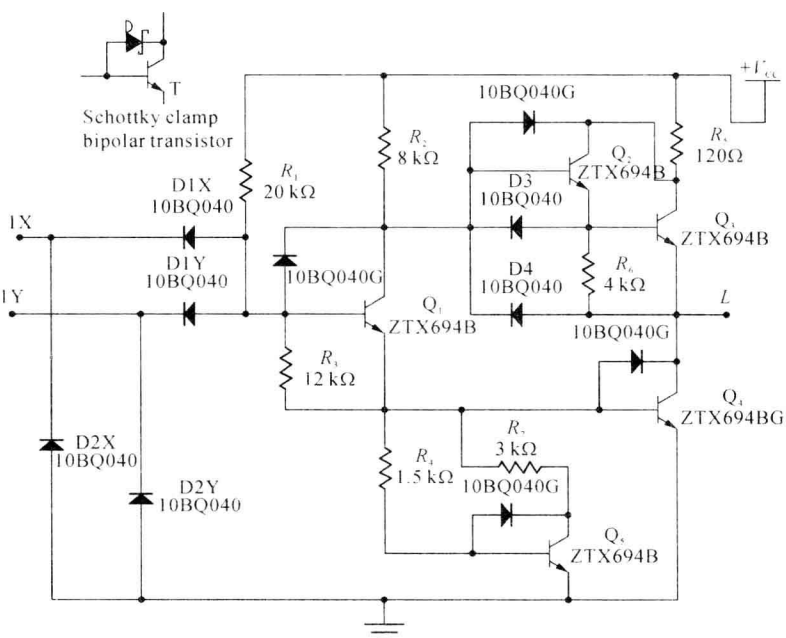


Figure 1 - 1 A simulated circuit of integral TIL NAND gate

In order to be convenient for simulation, we create a TTL subcircuit. Use a square frame to select a circuit shown in Figure 1 - 1, click on the symbol of "Create subcircuit",  , in "Tool Keys", a dialog box of "Subcircuit" appears on the "Circuit Window" shown as Figure 1 - 2. Write a name of the subcircuit in the "Name" field, such as "TTL", select "Replace in Circuit", the circuit is then placed in the subcircuit field. Then, drag the input nodes to the left board of the frame of the subcircuit, drag the output node to the right board, drag the power supply node to top board, and drag the GND node to the bottom board. The "Circuit Window" of EWB appears shown as Figure 1 - 3.

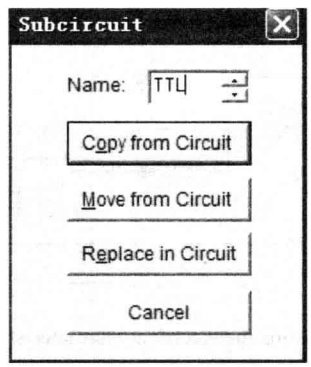


Figure 1 - 2 Create a subcircuit

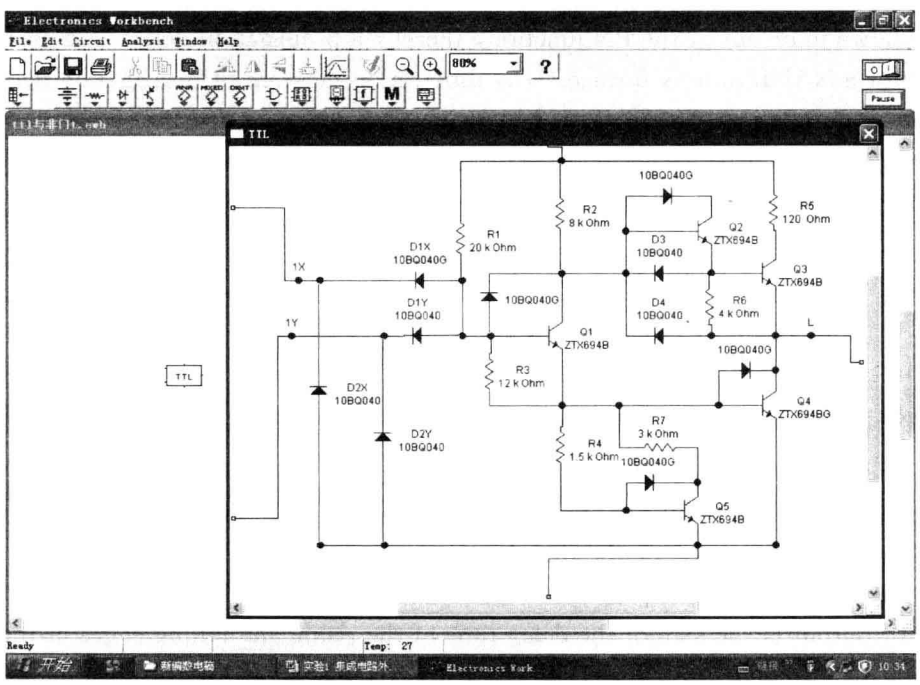


Figure 1 - 3 The terminals of the subcircuit

2. Measure the electrical characteristics of TTL NAND gate

(1) As shown in Figure 1 - 4, measure I_{CCH}, I_{IL}, V_{OH}.

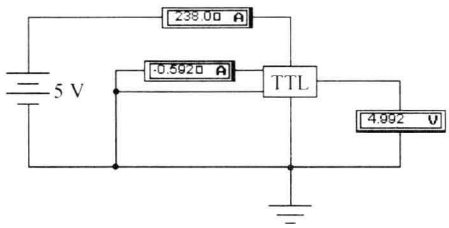


Figure 1 - 4 Measure the electrical characteristic with high output

(2) As shown in Figure 1 - 5, measure I_{CCL}, I_{IH}, V_{OL}.

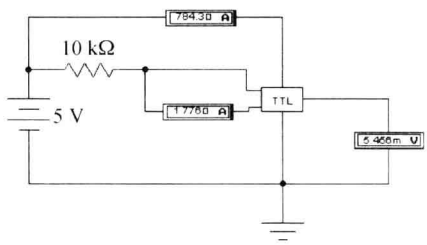


Figure 1 - 5 Measure the electrical characteristic with low output

(3) Since the PN junction capacitance is existed, when the state of the NAND gate changes, the charge wherein the PN junction along changes. It takes time that the charge flows in or out of the PN junction, thereby a propagation delay time of input to output for a NAND gate is formed. The illustration diagram of propagation delay time of input to output for a NAND gate is shown in Figure 1 - 6. And the circuit diagram of measuring the propagation delay time of input to output for a NAND gate by an annular oscillator is shown in Figure 1 - 7.

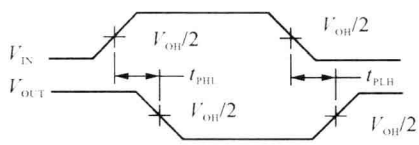


Figure 1 - 6 The illustration diagram of propagation delay time of input to output for a NAND gate

The circuit of an annular oscillator is formed with seven NAND gates. The output waveforms of each NAND gate are shown in the screen of a logic analyzer as Figure 1 - 7. As shown in Figure 1 - 7, the time between the rising edge of TTL1 and the falling edge of TTL2 is the falling propagation delay time of TTL2. The period of the annular oscillator output is the sum of the delay time of the rising and falling edges of the seven NAND gates. In generally, the rising edge of a NAND gate is not the same as its falling edge. Same thing happened to different NAND gates, their rising edges and falling ed-

ges are mostly not same. So, the measured delay time is only an average delay time of the rising edges and falling edges, $t_d = t/2N$ (N is the number of NAND gates), where t is the period of output waveform of the annular oscillator.

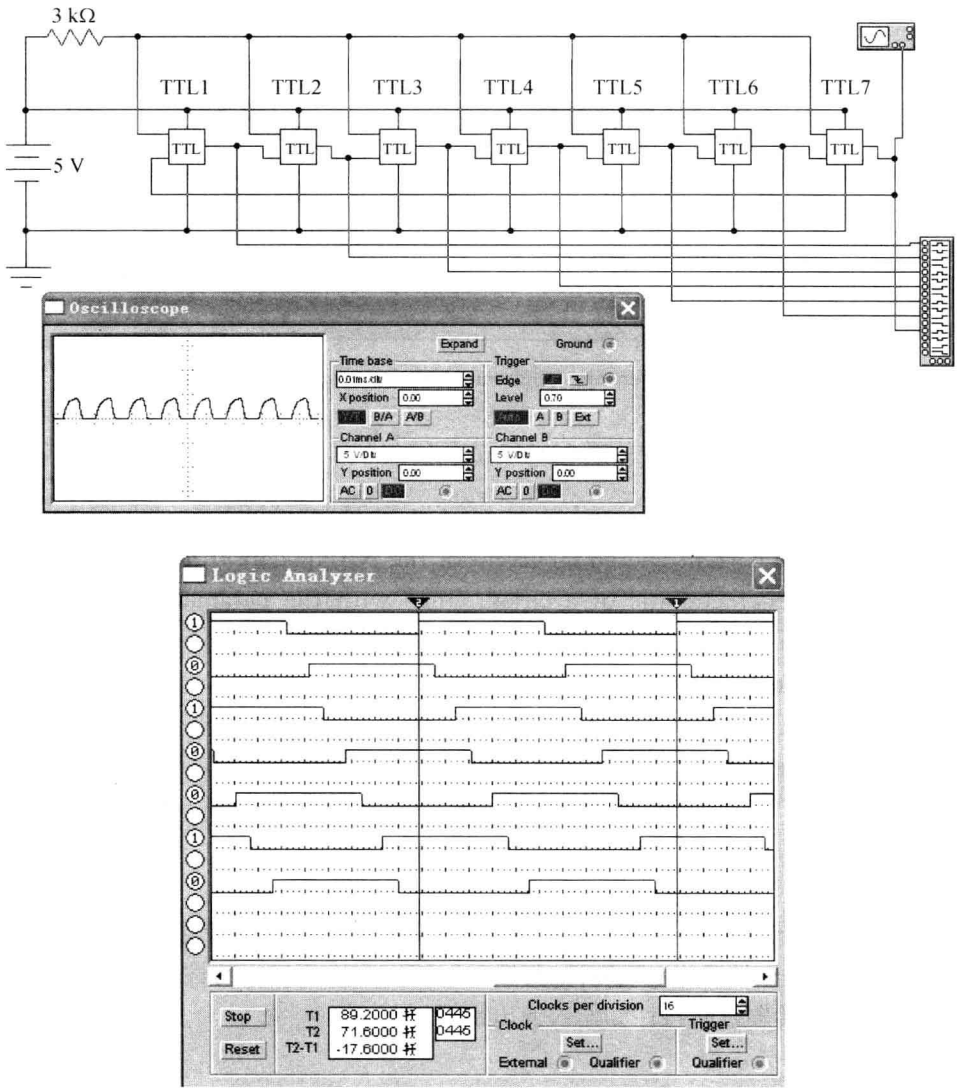


Figure 1 - 7 An annular oscillator for measuring propagation delay time of input to output for the NAND gate

(4) As shown in Figure 1 - 8, measure the input-output characteristic of the NAND gate.