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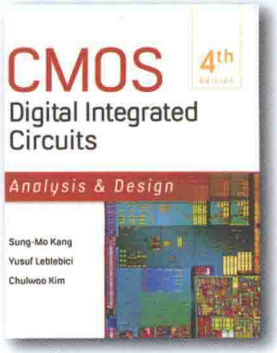
CMOS数字集成电路

——分析与设计(第四版)

CMOS Digit cuits Analysis and Design, Fourth Edition

[美] Sung-Mo Kang
[美] Yusuf Leblebici 著
[韩] Chulwoo Kim



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内容简介

全书详细讲述了CMOS数字集成电路的相关内容，为反映纳米级别CMOS技术的广泛应用和技术的发展，全书在前版的基础上对晶体管模型公式和器件参数进行了修正，几乎全部章节都进行了重写，提供了反映现代技术发展水平和电路设计的最新资料。全书共15章。第1章至第8章详细讨论MOS晶体管的相关特性和工作原理、基本反相器电路设计、组合逻辑电路及时序逻辑电路的结构与工作原理；第9章至第13章主要介绍应用于先进VLSI芯片设计的动态逻辑电路、先进的半导体存储电路、低功耗CMOS逻辑电路、数字运算和转换电路、芯片的I/O设计；第14章和第15章分别讨论电路的产品化设计和可测试性设计这两个重要问题。

本书是现代数字集成电路设计的理想教材和参考书。可供与集成电路设计领域有关的各电类专业的本科生和研究生使用，也可供从事集成电路设计、数字系统设计和VLSI设计等领域的工程师参考。

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ABOUT THE AUTHORS

Sung-Mo "Steve" Kang received his PhD in electrical engineering from the University of California, Berkeley. He has worked on the development of full-custom CMOS VLSI chips, including the world's first 32-bit full CMOS microprocessor and peripheral chips at AT&T Bell Laboratories in Murray Hill, New Jersey. He has taught digital integrated circuits at the University of Illinois at Urbana-Champaign; the University of California, Santa Cruz; the University of California, Merced; and the Korea Advanced Institute of Science and Technology (KAIST) in Daejeon, Korea. He has also given invited lectures and tutorials on CMOS digital circuits, reliability, and computer-aided design of VLSI circuits and systems at major conferences and universities globally.

Dr. Kang is a fellow of IEEE, ACM, and AAAS and has received many awards, including the IEEE Millennium Medal, IEEE Graduate Teaching Technical Field Award, IEEE CAS Society M. E. Van Valkenburg Award, IEEE CAS Society Technical Excellence Award, SRC Technical Excellence Award, and Chang-Lin Tien Education Leadership Award. He has served as Department Head of the University of Illinois at Urbana-Champaign; Dean of Engineering at the University of California, Santa Cruz; Chancellor of the University of California, Merced; and President of KAIST, Daejeon, Korea.

Yusuf Leblebici received a PhD in electrical and computer engineering from the University of Illinois at Urbana-Champaign. He has been a visiting assistant professor of electrical and computer engineering at the University of Illinois at Urbana-Champaign, associate professor of electrical and electronics engineering at Istanbul Technical University, and associate professor of electrical and computer engineering at Worcester Polytechnic Institute. He also served as the microelectronics program coordinator at Sabanci University. Currently, he is a full (chair) professor at the Swiss Federal Institute of Technology in Lausanne, Switzerland, and director of the Microelectronic Systems Laboratory. His research interests include design of high-performance CMOS digital and mixed-signal integrated circuits, computer-aided design of VLSI systems, intelligent sensor interfaces, modeling and simulation of semiconductor devices, and VLSI reliability analysis. He is a fellow of IEEE and recipient of the NATO Science Fellowship Award, the Young Scientist Award of the Turkish Scientific and Technological Research Council, and the Joseph Samuel Satin Distinguished Fellow Award of the Worcester Polytechnic Institute. He was elected as Distinguished Lecturer of the IEEE Circuits and Systems Society for 2010–2011.

Chulwoo Kim received BS and MS degrees in electronics engineering from Korea University, and a PhD in electrical and computer engineering from the University of Illinois at Urbana-Champaign. In 1999, he worked as a summer intern at

Design Technology at Intel Corporation, Santa Clara, California. In May 2001, he joined IBM Microelectronics Division in Austin, Texas, where he was involved in cell processor design. Since September 2002, he has been with the Department of Electronics and Computer Engineering at Korea University, where he is currently a professor. He was a visiting professor at the University of California, Los Angeles and at the University of California, Santa Cruz. His current research interests are in the areas of wireline transceiver, memory, power management, and data converters.

Dr. Kim received the Samsung HumanTech Thesis Contest Bronze Award, the ISLPED Low-Power Design Contest Award, the DAC Student Design Contest Award, the SRC Inventor Recognition Award, the Young Scientist Award from the Ministry of Science and Technology of Korea, the Seoktop Award for excellence in teaching, and the ASP-DAC Best Design Award. He is currently on the editorial board of *IEEE Transactions on VLSI Systems* and on the Technical Program Committee of the IEEE International Solid-State Circuits Conference.

作者简介

Sung-Mo (Steve) Kang（康松默） 于美国加州大学伯克利分校电机工程系取得博士学位，主要研究全定制 CMOS VLSI 芯片的发展。在美国新泽西州默里山 AT&T 贝尔实验室，他研究出了世界上第一个 32 位全 CMOS 微处理器及外围芯片。他曾在美国伊利诺伊大学厄巴纳-香槟分校、美国加州大学圣克鲁兹分校、美国加州大学默塞德分校以及韩国科学技术院（位于韩国大田）教授数字集成电路课程。他还在全球一些主要的会议和大学中，关于 CMOS 数字电路、可靠性，以及电脑辅助 VLSI 电路和系统的设计等问题，发表特约演讲及担任特邀讲师。

Kang 教授是 IEEE、ACM 以及 AAAS 会员。曾获诸多奖项，包括 IEEE Millennium 奖、IEEE 研究生教育技术领域奖、IEEE 电路与系统协会 M. E. Van Valkenburg 奖、 IEEE 电路与系统协会技术成就奖、SRC 卓越技术奖以及 Chang-Lin Tien 教育领导奖。他曾在美国伊利诺伊大学厄巴纳-香槟分校任系主任，美国加州大学圣克鲁兹分校任工程系系主任，美国加州大学默塞德分校担任名誉校长，现在在韩国科学技术院担任院长。

Yusuf Leblebici 于美国伊利诺伊大学厄巴纳-香槟分校电机和计算机工程系取得博士学位，是美国伊利诺伊大学厄巴纳-香槟分校的客座副教授，土耳其伊斯坦布尔科技大学电机和电子工程系的副教授，美国伍斯特理工学院电机和计算机工程系的副教授。曾担任土耳其萨班哲大学微电子项目的协调人。目前，他是瑞士联邦理工学院的全职（主）教授，并兼任微电子系统实验室主任。主要研究高性能 CMOS 数字及混合信号的集成电路设计，VLSI 系统的计算机辅助设计，智能传感器接口，半导体器件的模型及仿真，以及 VLSI 可靠性分析。他是 IEEE 会士，获北大西洋公约组织科学研究会奖，土耳其科学技术委员会年轻科学家奖，美国伍斯特理工学院 Joseph Samuel Satin 杰出人物奖。曾被选为 IEEE 电路与系统协会 2010-2011 年度杰出演讲人。

Chulwoo Kim 于韩国高丽大学电子工程系取得理科学士学位和硕士学位，于美国伊利诺伊大学厄巴纳-香槟分校电机和计算机工程系取得博士学位。1999 年，曾在美国加利福尼亚州圣克拉拉的因特尔公司设计工艺部门进行暑假实习；2001 年 5 月，加入位于得克萨斯州奥斯汀的 IBM 微电子部，研究单元处理器设计；2002 年 9 月，加入韩国高丽大

学电子和计算机工程系，现成为该系教授。曾任美国加州大学洛杉矶分校和美国加州大学圣克鲁兹分校的客座教授。目前研究有线线路收发器、存储器、功率管理以及转换器。

Kim 教授曾获三星人机工程论文比赛铜奖，ISLPED 低功率设计比赛奖，DAC 学生设计比赛奖，SRC 发明家奖，韩国科学技术部青年科学家奖，Seokto 优秀教师奖，ASP-DAC 最佳设计奖。现任 IEEE VLSI 系统交流会编委会委员及 IEEE 固体电路国际会议科技项目委员会成员。

PREFACE

Complementary metal oxide semiconductor (CMOS) digital integrated circuits are the enabling technology for the modern information age. Because of their intrinsic features in low-power consumption, large noise margins, and ease of design, CMOS integrated circuits have been widely used to develop random access memory (RAM) chips, microprocessor chips, digital signal processor (DSP) chips, and application-specific integrated circuit (ASIC) chips. The popular use of CMOS circuits continues to grow with the increasing demands for low-power, low-noise integrated electronic systems in the development of mobile computing platforms, wearable communication devices, smart phones, and multimedia systems.

Since the field of CMOS integrated circuits is broad, it is conventionally divided into digital CMOS circuits and analog CMOS circuits. This textbook is focused on the CMOS digital integrated circuits. However, it should be noted that the boundary between classical digital and analog CMOS design is becoming increasingly blurred, especially with the challenges presented by nanometer-scale fabrication technologies, very low operating voltages, and operating frequencies extending well into the multi-GHz range. Therefore, we attempt to present the analysis and design of digital CMOS integrated circuits from an "analog" point-of-view, i.e., taking into account the analog, non-discrete nature of the devices and circuits that are used to implement digital functions.

The origins of this textbook date back to the early 1990s, when the first two authors were intensively involved in undergraduate- and graduate-level teaching of digital IC fundamentals. At the University of Illinois at Urbana-Champaign, where both of us were teaching at the time, we tried some of the available textbooks on digital MOS integrated circuits for our senior-level technical elective course, ECE382—Large Scale Integrated Circuit Design. Students and instructors alike realized, however, that there was a need for a new book with more comprehensive treatment of CMOS digital circuits. Thus, our textbook project was initiated several years ago by assembling our own lecture notes. Since 1993, we have used evolving versions of this material at the University of Illinois at Urbana-Champaign, at Istanbul Technical University, at Worcester Polytechnic Institute, and at the Swiss Federal Institute of Technology in Lausanne. We are both encouraged by comments from our students, colleagues, and reviewers. The first edition of *CMOS Digital Integrated Circuits: Analysis and Design* was published in late 1995.

Soon after publishing the first edition, we saw the need for updating it to reflect the many constructive comments we were receiving from instructors and students who used the textbook. We intended to include and update important topics such as low-power circuit design and interconnects in high-speed circuit design, as well as the deep submicron circuit design issues, and to provide more rigorous treatment of new developments in memory circuits. We also felt that in a rapidly developing field such as CMOS

digital circuits, the quality of a textbook can only be preserved by timely updates reflecting the state of the art. This realization has led us to embark on the successive revisions of our work, with the second edition appearing in 1998 and the third edition in 2002, to reflect the advances in technology and in circuit design practices.

During the 11 years that have passed since the publication of the third edition in 2002, the domain of CMOS digital integrated circuits has continued to grow and develop at an ever-increasing pace. The advent of nanometer-scale technologies and the widespread use of system-on-chip architectures combining a large number of functional blocks on chip have ushered in dramatic changes in the way digital CMOS integrated circuit design has to be treated. Thus, we came to the conclusion that incremental revisions would no longer do justice for the next edition of this textbook, and that we needed a comprehensive rewriting of virtually all chapters. The author team was expanded by the valuable addition of Professor Chulwoo Kim of Korea University, and an extensive revision was embarked upon. The fourth edition is the outcome of this intensive effort.

CMOS Digital Integrated Circuits: Analysis and Design is intended primarily as a comprehensive textbook at the senior level and first-year graduate level, as well as a reference for practicing engineers in the areas of integrated circuit design, digital design, and VLSI. Recognizing that the area of digital integrated circuit design is evolving at an increasingly faster pace, we have made our best effort to present up-to-date materials on all subjects covered. This textbook contains 15 chapters; we recognize that it would not be possible to cover rigorously all of this material in one semester. Thus, we would propose the following based on our teaching experience: At the undergraduate level, coverage of the first 10 chapters would constitute sufficient material for a one-semester course on CMOS digital integrated circuits.

Time permitting, some selected topics in Chapter 11, "Low-Power CMOS Logic Circuits," Chapter 12, "Arithmetic Building Blocks," and Chapter 13, "Clock and I/O Circuits" could also be covered. Alternatively, this book could be used for a two-semester course, allowing a more detailed treatment of advanced issues, which are presented in the later chapters. At the graduate level, selected topics from the first 10 chapters plus the last 5 chapters can be covered in one semester.

The first 8 chapters of this textbook are devoted to a detailed treatment of the MOS transistor with all its relevant aspects; to the static and dynamic operation principles, analysis, and design of basic inverter circuits; and to the structure and operation of combinational and sequential logic gates. Note that the introduction chapter has been significantly expanded to include a detailed presentation of VLSI design methodologies. Since the digital integrated circuit design techniques discussed in the first half of this textbook are directly relevant for digital VLSI and ASIC design, we felt that the context should be presented at the beginning of the book. The issues of on-chip interconnect modeling and interconnect delay calculation are covered extensively in Chapter 6, which provides a complete view of switching characteristics in digital integrated circuits. A separate chapter (Chapter 9) has been reserved for the treatment of dynamic logic circuits, which are used in state-of-the-art VLSI chips. Chapter 10 has been completely revised in both content and presentation; it offers an in-depth presentation of many state-of-the-art semiconductor memory circuits.

Recognizing the increasing importance of low-power circuit design, we dedicate one chapter (Chapter 11) to low-power CMOS logic circuits, which provides a comprehensive coverage of methodologies and design practices that are used to reduce the power dissipation of large-scale digital integrated circuits. Key arithmetic building blocks are presented in Chapter 12, with an emphasis on high-performance multibit adders and multipliers.

Next, Chapter 13 provides a clear insight into the important subjects of clocking and chip I/O design. Critical issues such as ESD protection, clock distribution, clock buffering, and latch-up phenomena are discussed in detail. Finally, the more advanced but important topics of design for manufacturability and design for testability are covered in Chapters 14 and 15, respectively.

We have long debated the coverage of nMOS circuits in this textbook. We have concluded that some coverage should be provided for pedagogical reasons. Thus, to emphasize the load concept, which is still widely used in many areas in digital circuit design, we present basic resistive-load and pseudo-nMOS inverter circuits along with their CMOS counterparts in Chapter 5, while we present pseudo-nMOS logic gates (NAND/NOR) in Chapter 7.

The Online Learning Center for this edition (www.mhhe.com/kang) also contains:

- An Instructors Manual
- Lecture Slides (PowerPoint and PDF)
- Cadence™ Design Tutorial
- Color Plates.

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Although an immense amount of effort and attention to detail were expended to prepare the camera-ready manuscript, this textbook may still have some flaws and

mistakes due to erring human nature. We welcome and greatly appreciate suggestions and corrections from readers for the improvement of technical content as well as the presentation style.

ACKNOWLEDGMENTS TO THE FIRST EDITION

Our colleagues have provided many constructive comments and encouragement for the completion of the first edition. Professor Timothy N. Trick, former head of the department of electrical and computer engineering at the University of Illinois at Urbana-Champaign, has strongly supported our efforts from the very beginning. The appointment of Sung-Mo Kang as an associate in the Center for Advanced Study at the University of Illinois at Urbana-Champaign helped to start the process. Yusuf Leblebici acknowledges the full support and encouragement from the department of electrical and electronics engineering at Istanbul Technical University, where he introduced a new digital integrated circuits course based on the early version of this book and received very valuable feedback from his students.

Yusuf Leblebici also thanks the ETA advanced Electronics Technologies Research and Development Foundation at Istanbul Technical University for their generous support. Professor Elyse Rosenbaum and Professor Resve Saleh used the early versions of the manuscript as the textbook for ECE382 at Illinois and provided many helpful comments and corrections, which have been fully incorporated with deep appreciation. Professor Elizabeth Brauer, currently at Northern Arizona University, has also done the same at the University of Kentucky.

The authors would like to express sincere gratitude to Professor Janak Patel of the University of Illinois at Urbana-Champaign for generously mentoring the authors in writing Chapter 15, "Design for Testability." Professor Patel has provided many constructive comments, and many of his expert views on the subject are reflected in this chapter. Professor Prith Banerjee of Northwestern University and Professor Farid Najm of the University of Illinois at Urbana-Champaign also provided many good comments. We would also like to thank Dr. Abhijit Dharchoudhury for his invaluable contribution to Chapter 14, "Design for Manufacturability."

Professor Duran Leblebici of Istanbul Technical University, who is the father of the second author, reviewed the entire manuscript in its early development phase, and provided very extensive and constructive comments, many of which are reflected in the final version. Both authors gratefully acknowledge his support during all stages of this venture. We also thank Professor Cem Göknar of Istanbul Technical University, who offered very detailed and valuable comments on "Design for Testability," and Professor Uğur Çilingiroğlu of the same university, who offered many excellent suggestions for improving the manuscript, especially the chapter on semiconductor memories.

Many of the authors' former and current students at the University of Illinois at Urbana-Champaign also helped in the preparation of figures and verification of circuits using SPICE simulations. In particular, Dr. James Morikuni, Dr. Weishi Sun, Dr. Pablo Mena, Dr. Jaewon Kim, Mr. Steve Ho, and Mr. Sueng-Yong Park deserve recognition. Ms. Lilian Beck and the staff members of the Publications Office in the department of

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前　言

互补金属氧化物半导体（CMOS）数字集成电路是当今信息时代一种领先技术。由于具有低功耗、大噪声容限以及易于设计等固有的特点，CMOS 集成电路在开发研制随机存储器（RAM）、微处理器、数字信号处理（DSP）和专用集成电路（ASIC）芯片方面得到了广泛的应用。随着在移动计算平台、可穿戴设备、智能手机和多媒体系统等芯片开发方面对于低功耗、低噪声电子系统日益增长的需求，CMOS 电路的广泛应用将持续增长。

CMOS 集成电路涉及的领域非常广泛，通常分为数字 CMOS 电路和模拟 CMOS 电路两类。本书将集中讨论 CMOS 数字集成电路。然而需要指出的是：随着纳米制作工艺、极低的工作电压和 GHz 级工作频率带来的挑战，经典的数字 CMOS 电路设计与模拟 CMOS 电路设计的界限已渐趋模糊。因此，作者将试图从“模拟”的角度来分析和设计数字 CMOS 电路，例如用器件和电路的模拟及连续特性来实现数字化功能。

作者在 20 世纪 90 年代初期即计划撰写本书，当时两位主要作者正在从事本科及研究生的数字集成电路基础教学。在美国伊利诺伊大学厄巴纳-香槟分校任教期间，在高年级工程技术选修课（即 ECE382——大规模集成电路设计）教学中作者曾尝试选用已有的教材，然而老师和同学们一致反映需要一本深入讨论 CMOS 逻辑电路的全新教材，因此作者通过整理多年的课堂讲义开始编撰本书。从 1993 年起，作者在美国伊利诺伊大学厄巴纳-香槟分校、土耳其伊斯坦布尔科技大学、美国伍斯特理工学院、瑞士联邦工学院使用了这些新版的讲义。从广大同学、同行及审阅者的好评中，我们得到了极大的肯定和鼓舞。于 1995 年底出版了《CMOS 数字集成电路——分析与设计》的第一版。

在第一版出版后不久，使用本书的众多师生提出了许多建设性的意见，作者迫切感到本书有待修订。作者对低功耗电路的设计、高速电路设计中的互连线问题、深亚微米电路设计等问题进行了修改和补充，并针对存储电路的新发展提供了众多更为精确有效的处理方法。在 CMOS 数字电路这个发展异常迅速的领域中，一本教科书只有通过不断修订，及时反映当今的技术发展水平，才能保证具有高的学术水平。基于这种认识，作者对本书不断地进行修订，先后于 1998 年、2002 年出版了第二版和第三版，以反映技术水平和电路设计实践的最新发展。

从 2002 年本书第三版发行到现今的 11 年里，CMOS 数字集成电路领域一直以越来越快的速度发展。纳米科技的出现以及集成大量功能模块的片上系统的广泛应用给 CMOS 数字集成电路的设计方式带来了巨大且亟需应对的改变。因此我们认为仅对内容进行增加修订已经不能满足本教材下一版本的要求了，而是需要对几乎所有章节进行全面重写。我们的作者团队加入了一位重要成员，来自韩国高丽大学的 Chulwoo Kim 教授。我们一起

对本教材进行了大量修订。本书的第四版终于在付出艰辛努力后诞生了。

本书可作为高年级本科生和一年级研究生的教材，也可供从事集成电路设计、数字设计、VLSI 等领域的工程师参考。数字集成电路设计正在持续高速地发展，作者也竭尽全力对本书所涵盖的内容提供最新的资料。

本书共分 15 章，依据作者的教学经验，在一学期内教授本书所有内容略显局促，因此推荐按照如下计划授课：在面向本科生的教学中，用一学期的时间来讲授第 1 章至第 10 章有关 CMOS 数字集成电路的内容。如时间允许，还可有选择地讲授第 11 章“低功耗 CMOS 逻辑电路”、第 12 章“算术组合模块”和第 13 章“时钟电路与输入输出电路”的内容。本书也可安排为两学期讲授，可以对后面章节中的新问题进行详细的探讨。在面向研究生的教学中，本书的全部章节可安排在一个学期内讲授。

本书的第 1 章至第 18 章详细讨论 MOS 晶体管及其相关特性、静态和动态工作原理与分析以及基本反相器电路的设计、组合逻辑电路及时序逻辑电路的结构与工作原理。第四版第 1 章的内容有大量扩充，将详细介绍一些 VLSI 的设计方法。由于本书的前半部分主要讨论的是与数字 VLSI 及 ASIC 设计相关的一些数字 IC 设计方法，作者认为有必要在本书的开头加以说明。第 6 章深入讨论芯片上的互连线模型及互连线上的延迟时间计算，并将完整介绍数字集成电路的开关特性。第 9 章单独介绍应用于达到领先水平的 VLSI 芯片上的动态逻辑电路。第 10 章在内容和表达形式方面都做了全面的修改，深入地介绍许多达到当今领先水平的半导体存储电路。由于低功耗电路设计的重要性日益增加，作者在第 11 章将致力于低功耗 CMOS 逻辑电路的讨论，全面覆盖了低功耗大规模数字集成电路的设计方法和实例。第 12 章介绍关键算数运算模块，并重点介绍高性能多位加法器和乘法器。第 13 章将对时钟电路和芯片的 I/O 设计做详细介绍。对如 ESD 保护电路、时钟分配、时钟缓冲及闩锁效应等一系列不可忽视的问题也给出了详细的讨论。最后，第 14 章和第 15 章分别讨论电路的可制造性设计和可测试性设计这两个重要问题。

作者曾就本书中的 nMOS 电路进行了长篇幅的讨论。从教学的角度来看，对 nMOS 电路进行一些介绍是有益的。为了强调广泛应用于数字电路设计的负载的概念，第 5 章介绍了基本的电阻型负载和伪 nMOS 反相器电路以及与其对应的 CMOS 电路，并在第 7 章介绍伪 nMOS 逻辑门（与非 / 或非）。

本书的教师资源包括习题解答和 PPT，学生资源包括 Cadence 设计教程和本书彩图。[①]

① 教师资源申请邮箱：te_service@phei.com.cn。学生资源可在 www.mhhe.com/kang 或华信教育资源网（www.hxedu.com.cn）下载。