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Advanced Field-Solver Techniques for RC Extraction of Integrated Circuits

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内 容 简 介

电阻、电容(RC)提取是设计纳米制造工艺集成电路的重要步骤，通过它对集成电路中的互连线或衬底耦合效应进行电学建模，为进一步的电路性能验证、制造良率分析提供基础。用于RC提取的场求解器方法直接对电场进行求解，因此具有最高的准确度。为了满足集成电路设计中准确建模与仿真的要求，场求解器RC提取方法正变得越来越重要。本书对刻画超大规模集成电路互连线和混合信号集成电路衬底耦合效应的关键场求解器提取方法进行了全面、系统的介绍。通过来自实际电路设计的例子，对各种场求解器算法进行了详细阐述，并说明它们各自的优点和缺点。

本书适合于电子工程和计算机工程相关专业的研究生和学者阅读，也可为工作在集成电路设计、设计自动化领域的技术人员提供参考

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Wenjian Yu • Xiren Wang

Advanced Field-Solver Techniques for RC Extraction of Integrated Circuits

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Foreword

This book is about three-dimensional RC extraction techniques for microelectronic designs. The authors are from the Parasitic Parameter Extraction Group, Department of Computer Science and Technology, Tsinghua University, which has made many significant contributions to the field since 1991. Some of their approaches, e.g., direct boundary element method (BEM) for C extraction (2001–2006) and hierarchical block BEM (2004), have been incorporated in industrial tools.

Resistance and capacitance (RC) extraction is an essential step to model the interconnect wires and substrate coupling in integrated circuits. The parasitic plays a significant role in the system performance. Advances of fabrication processes and new materials with various dielectric permittivities call for accurate and efficient extraction tools to handle complex geometries. Although RC extraction has been a research topic in the electronic design automation community for about 25 years, larger designs and faster project turnaround have kept pushing the demand for better extraction tools.

The authors cover the state-of-the-art techniques of RC field solvers, mainly the boundary element method (direct or indirect) with accelerating techniques and the fast floating random walk methods. These subjects are relatively new and of large impact theoretically and practically. The content also reflects the research activities of the authors in the last 10 years.

This book presents a systematic introduction to and treatment of the key concepts of the extraction. To the best of my knowledge, it is the first time for a monograph dedicated to the advanced RC extraction techniques. Various field-solver techniques are explained in details, with examples to illustrate the advantages and disadvantages of each algorithm. Readers are encouraged to consider the computational complexity, physical theory, numerical stability, robustness of the algorithm for general cases, and applicability for software development and maintenance. The presentation brings insights of suitable solvers for specific extraction problems.

San Diego, CA, USA

Chung-Kuan Cheng

Preface

The main goal of writing this book was to present a methodological and algorithmic perspective on the field-solver-based parasitic extraction of integrated circuits (ICs). Specifically, we present advanced techniques based on three-dimensional (3-D) boundary element method and floating random walk method for the problems of resistance and capacitance (RC) calculation. With the feature size scaling down and mixed-signal interference in modern ICs, the research of parasitic extraction has gained much concern in recent years and promoted the utilization of field-solver methods for tackling the challenge of accuracy.

Now, the field solver which directly solves the electrostatic equations is becoming more and more important for the RC extraction of ICs. It is a necessary supplement, or even a replacer, of the existing parasitic extraction methodology. On accurately capturing the complex interconnect geometry and the substrate coupling in mixed-signal IC, the field-solver method has distinct advantages. The major obstacle for its application is the excessive computational expense. The complexity of interconnect structure and even tighter performance margin for designing nanometer-technology ICs have urged the extensive usage of field solvers. The random process variations also add significance to this request. All these have pushed the related research for 20 years. Various accelerating approaches have been proposed to reduce the computational expense while preserving accuracy. Until recently, the achievements of these works have been applied successfully in industrial tools. They are daily used for settling the sign-off timing and verification issues in various IC designs. These achievements in field-solver-based RC extraction are the object of this book. We hope we have succeeded in providing a unique and comprehensive treatment on them.

The works presented in this book are mostly from research projects undertaken by the Parasitic Extraction Group, Tsinghua University, China. Chapter 3 and Chaps. 5, 6, and 7 are contributed by Xiren Wang, mostly from his Ph.D. work at the Parasitic Extraction Group. The remaining chapters are written by Wenjian Yu, based on his research work. Many of those original publications can be found at http://learn.tsinghua.edu.cn:8080/2003990088/index.htm.

We want to emphasize that the book is by no means intended to be comprehensive. The absence of coverage of related works should by no means diminish their value and contribution. Many academic groups and experts from industry have made significant contributions in the field, and the reader is encouraged to investigate their works. Key contributors to progress in RC field-solver techniques include: Jacob White (MIT), Weiping Shi (TAMU), Lawrence T. Pileggi (CMU), Ali Niknejad (UC Berkeley), Dan Jiao (Purdue Univ.), Vikram Jandhyala (Univ. Washington), Luca Daniel (MIT), Yannick L. Le Coz (RPI), Sheldon X.-D. Tan (UC Riverside), Lei He (UCLA), Ranjit Ghapurey (UT Austin), Charlie Chung-Ping Chen (National Taiwan Univ.), Wayne Dai (UCSC), Nick van der Meijs (TU Delft), Luis Miguel Silveira (Technical University of Lisbon), Ibrahim Elfadel (Masdar Institute of Science and Technology), Nasser Masoumi (Univ. Waterloo), Madhav P. Desai (Indian Institute of Technology, Bombay), Angelo Brambilla (Politecnico di Milano), Alkiviades A. Hatzopoulos (Aristotle Univ. Thessaloniki), Ruben Specogna (Univ. Udine), Xuan Zeng (Fudan Univ.), Zeyi Wang (Tsinghua Univ.), Wei Hong (Southeast Univ.), Junfa Mao (Shanghai Jiaotong Univ.), Martin Bachtold (Swiss Federal Institute of Technology), Sharad Kapur (Integrand Software Inc.), Joel R. Phillips (Cadence Inc.), Xiaoning Qi (Intel), and Zhuoxiang Ren (Mentor Graphics Inc.).

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It is a pleasure to record our gratitude to many colleagues and students who have contributed to this book. First of all, the authors would like to thank Prof. Zeyi Wang of Tsinghua University. He was the Ph.D. thesis advisor of both authors and had been the leader of the Parasitic Extraction Group until 2006. The quasi-multiple medium approach for accelerating the boundary element method (BEM) originates from his idea, and several works on fast BEM approaches were also under his guidance. Many students in this group have excellent contributions to the works in this book, including Deyan Liu, Mengsheng Zhang, Lei Zhang, Wangyang Zhang, Chao Hu, Qingqing Zhang, Hao Zhuang, Zhi Liu, Gang Hu, and Chao Zhang. Special thanks are also given to Prof. Xianlong Hong of Tsinghua University for his great support during these years and Dr. Jiangchun Gu and Dr. Jinsong Hou graduated from the group, who had provided a solid basis for our research works.

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Xiren Wang is appreciative to the members in the Parasitic Extraction Group of Tsinghua University, where he had stayed for 5 years and got the Ph.D. degree. He is also grateful to Prof. Vikram Jandhyala at the University of Washington, who had been his postdoc advisor. Discussion with Dr. Dipanjan Gope at the University of Washington, and now Indian Institute of Science, was largely beneficial and really appreciated.

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Last but not least, Wenjian Yu and Xiren Wang would like to thank their families, respectively, for understanding and support during the many hours it took to compose this book.

Contents

Chapter 1
Introduction

1.1 The Need for Parasitic Extraction

In very large-scale integration (VLSI) circuits, electromagnetic coupling among interconnect wires is becoming increasingly important. With the introduction of deep sub-micronmeter (DSM) or nanometer semiconductor technologies, the on-chip interconnect wire could no longer be considered as equipotential link. The parasitic effects introduced by the wires display a scaling behavior that differs from that of active devices such as transistors, and these effects tend to gain importance as device dimensions are reduced and circuit speed is increased. In fact, they have dominated some of the relevant metrics of digital integrated circuits, such as speed and reliability. A typical recursive design flowchart of digital integrated circuit (IC) is shown in Fig. 1.1, where a post-layout step termed *parasitic extraction* precedes *gate-level simulation*. Each step in the design flow corresponds to numerous computer-aided design (CAD) tools, which guarantee the feasibility of designing modern VLSI circuits. The task of parasitic extraction is to model the electromagnetic effect of the wires with parasitic components of capacitance (C), resistance (R), and inductance (L), so that the gate-level simulation, including timing analysis, can be performed.

In microwave or analog integrated circuits, the electromagnetic coupling among conductors also greatly influences circuit performance. This coupling effect is sometimes utilized to construct compact circuit components. But under most circumstances, it is regarded as a parasitic effect that must be modeled accurately for the verification of circuit's validity and performance. With the increase of working frequency and advancement of the silicon technologies, the discrepancy between the analog IC and the VLSI digital IC becomes reduced. Therefore, the electromagnetic modeling and accurate extraction of the interconnect parasitics have become a widely concerned research topic. Among the three parasitic parameters, capacitance has attracted the most attention because it greatly influences time delay, power consumption, and signal integrity [3, 32]. Because of the equivalence of electrostatic field and steady-state current field, the method for extracting capacitances can

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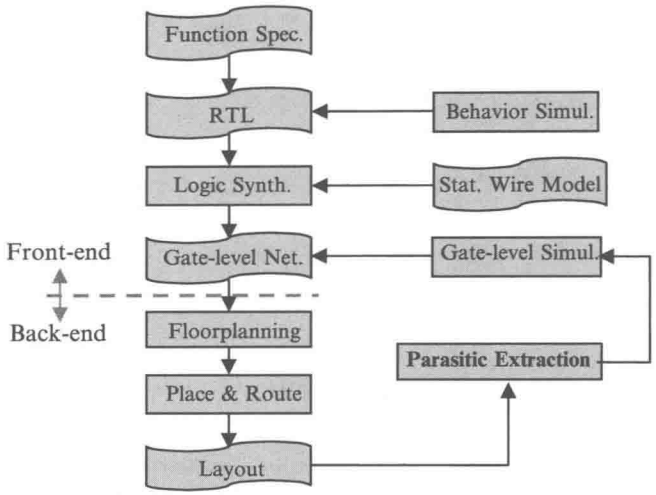

Fig. 1.1 A typical recursive design flow of digital IC (Reprinted with permission from Yu and Wang [180] © 2005 John Wiley & Sons)

be applied to extract the resistances. In most cases, the resistance extraction of interconnect wire is much easier. If the signal frequency is not very high, the inductive effect is not prominent. For example, the parasitic inductance is often ignored in the design of digital IC.

Except for the parasitic effect on interconnect wire, the modeling of substrate coupling in mixed-signal IC also attracts a lot of attention. With the increase of integration, the digital components and analog components in a circuit are often built on a common silicon substrate. This gives rise to the problem called *substrate noise coupling*. The digital components may inject current noise into the substrate, which travels throughout the substrate and severely impacts the sensitive analog components. The substrate coupling affects some circuit metrics, like the quality factor of spiral inductor in microwave circuit. If the signal frequency is not very high, the substrate coupling can be modeled with a resistance network among contacts. With the increase of frequency, more comprehensive model with both capacitance and resistance effects should be adopted. The calculation of the substrate coupling parameters is also regarded as a parasitic extraction problem. Efficient modeling and extraction of substrate coupling are necessary, or even critical, for the design of mixed-signal IC.

1.2 The Methods for RC Extraction and Field Solver

An accurate and general method for calculating the capacitance parameters needs simulating the electrostatic field among conductors, because capacitance is the coefficient relating the electric potential (voltage) and the electric charge. This method

is often referred to as *field solver*. For the problems of resistance extraction and inductance extraction (or impedance extraction), there are different field solvers which simulate corresponding steady current field and electromagnetic field. However, efficient field solver for capacitance calculation is difficult, if feasible, due to the large quantity of and complicated interconnect wires we are facing in ICs. That means huge expense on memory and computing time.

To obtain a good trade-off between accuracy and efficiency, modern capacitance extraction tools utilize special techniques for the capacitance extraction in IC design, which is usually divided into two major steps [79]:

1. Technology precharacterization. Given a description of the process cross sections, tens of thousands of test structures are enumerated and simulated with two-dimensional (2-D) and/or three-dimensional (3-D) field solvers. The resulting data are collected either to fit some empirical formulas or to build lookup tables (either type is called a "pattern library") [3, 32, 33, 55]. This first step should be performed only once per process technology. The challenge in this step includes the handling of increasingly complex technology features, such as low-k dielectric, air bubble, nonvertical conductor cross sections, conformal dielectric, and shallow trench isolations.
2. Capacitance extraction with pattern-matching approach. While performing full-chip or full-path (specified critical signal path) extraction, the whole structure is chopped into small- or medium-sized pieces firstly. Each piece is regarded as a pattern structure with geometric parameters. Then, the geometric parameters are matched to some entries in the precharacterized pattern library. Finally, the capacitance values of the piece can be obtained through table lookup or analytical formulas. With more kinds of patterns and more geometric parameters per pattern, the computational expense of technology precharacterization and the complexity of the pattern-matching procedure will largely increase. On the other hand, if there are few patterns and each is described by very few parameters, it becomes difficult to be accurate. So, the definition of geometric patterns is crucial and relates both steps in modern parasitic extraction tool. Some techniques can be used to reduce the complexity of geometric patterns by considering the shielding effect in electrostatic field. For example, it is often assumed that the conductors two layers away from the main conductor of interest can be described as a big plane [33, 55].

There are two major sources of error in the pattern-matching approach. The first one is called the *pattern mismatch*, where extracted geometry parameters do not have an exact match in the pattern library. The other one is due to the layout decomposition, which is analyzed in Dengi and Rohrer [37] and can be revamped by the approach proposed by Shi and Yu [134]. However, with the increase of geometric and material complexity in the advanced process technology, the error of pattern-matching-based capacitance extraction will be even larger.

For the resistance of interconnect wire, the simple method of "square-counting" is fast and accurate in most time. However, to model some complex 3-D structure, the field-solver method should be used to simulate the steady current field in the