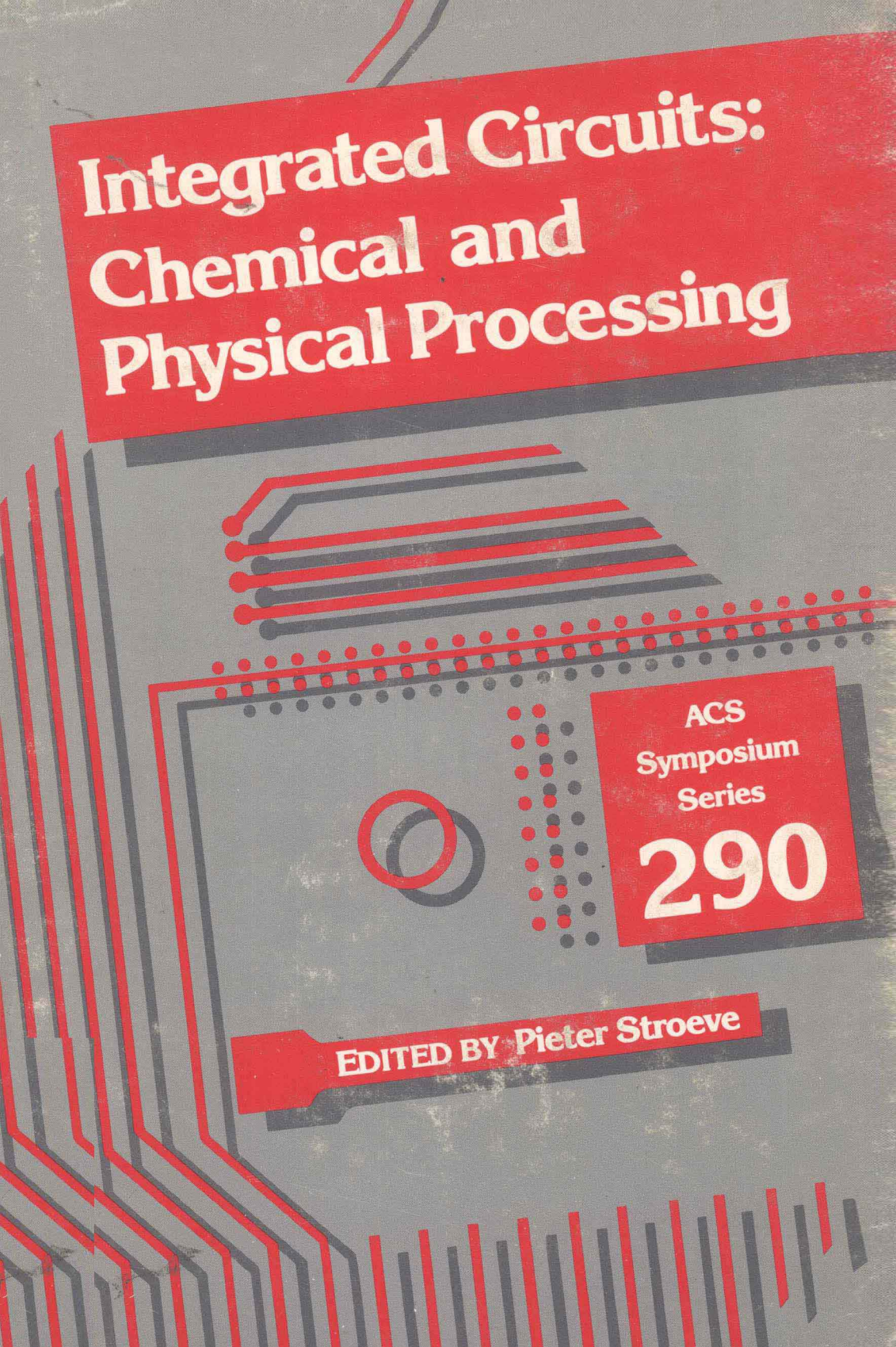
Integrated Circuits: Chemical and Physical Processing



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FOREWORD

The ACS SYMPOSIUM SERIES was founded in 1974 to provide a medium for publishing symposia quickly in book form. The format of the Series parallels that of the continuing ADVANCES IN CHEMISTRY SERIES except that, in order to save time, the papers are not typeset but are reproduced as they are submitted by the authors in camera-ready form. Papers are reviewed under the supervision of the Editors with the assistance of the Series Advisory Board and are selected to maintain the integrity of the symposia; however, verbatim reproductions of previously published papers are not accepted. Both reviews and reports of research are acceptable, because symposia may embrace both types of presentation.

PREFACE

THE MANUFACTURE OF INTEGRATED CIRCUITS has become a sophisticated technology involving complex physical and chemical operations, often under computer control, that are designed to build structures or modify properties of materials in very thin films. The complexity of any manufacturing process can be understood by studying the individual unit processes used to manufacture integrated circuits. The fundamental physical and chemical phenomena occurring in these unit processes are under intensive investigation by scientists and engineers. This fact is somewhat surprising because the unit processes are used extensively in processing. However, a further understanding of the basic processes may lead to better process control and consequently to better product yield and quality. The fundamental phenomena occurring in the unit processes include mass transfer, heat transfer, fluid mechanics, chemical reaction, phase transformations, and adsorption. To be able to predict how these processes influence the characteristics of the electrical components built on the wafer's surface, one also must have a good background in solid state physics, materials science, and electrical engineering. Therefore, research in the area of integrated circuits has become interdisciplinary, and researchers come from such distinct fields as chemical engineering and solid state physics.

The chapters in this volume present a cross section of some of the most important areas of study in the fabrication of integrated circuits. Many of the chapters are reviews, and the book gives an overview of many areas important in the manufacture of integrated circuits. Both experts and novices will find material in this text that will increase their knowledge of the phenomena occurring in the unit processes.

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April 15, 1985

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Unit Processes in the Manufacture of Integrated Circuits

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The fabrication of integrated circuits is very complex. The intricacy of a particular process can be understood by considering the individual unit processes used to make the product. Key unit processes are consistently used in the manufacture of integrated circuits. An improved understanding of the basic physical and chemical fundamentals of each process will help the manufacturing engineer in controlling the uniformity of the product or to design new processes.

The microelectronic revolution is the term utilized for the phenomena of manufacturing large numbers of electronic components on thin silicon chips and the utilization of these chips in sophisticated electronic devices. The push for miniaturization came in part because of economic needs to produce circuits at much lower cost and at lower power requirements, the development of small electronic devices, and the need to produce high speed electronic computers. The microelectronic revolution began with the invention of the transistor in the late 1940's and has grown to a multi-billion dollar industry today. The growth of the industry is truly amazing considering that the first integrated circuits were marketed in early 1960's. At that time, integrated circuits were "small-scale" in the sense that about 10 components would be present per single chip. In the mid to the end of the 1960's medium-scale integrated circuits were build containing up to 1024 components per circuit, or a 1K bit circuit. In the 1970's large-scale circuits were built and in the 1980's we now speak of very large scale integrated circuits (VLSI). Presently, circuits are built with 262,144 components per circuit or 262K, which is equal to 2^{18} components on a single chip. In the near future, 1M bit chips will be a standard product. This number is staggering

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considering that a chip is approximately 0.5 by 0.5 cm. Because of the larger number of components, the cost per component is a small fraction of a penny (<0.01¢), and the basic cost per chip continues to decrease even though the number of components per chip have increased.

The design of 262K and 1M bit chips is a very complicated process. Computer-aided design techniques are now used to perform many of the time-consuming tasks such as the relative placement of transistors, resistors and diodes, and the design of interconnections. Large computer programs and data bases are required to perform such design calculations. The computer-aided design techniques can be used to verify that the design conforms to the constraints imposed by the integrated circuit fabrication process.

The manufacture of integrated circuits involve a series of lithographic, deposition, and etching steps to fabricate patterned layers. This process is often called planar processing or planar technology.

The manufacture of thin film products does not only apply to the making of integrated circuits but also magnetic bubble memories, thin film recording heads, tapes and disks. The physical and chemical processes carried out involve heat and mass transfer, momentum transfer, surface phenomena, high temperature chemistry, radiation, etc. Although the material discussed in this book focuses on the manufacture and fundamentals of integrated circuits, many of the basics are applicable to the fabrication of other thin film devices.

Planar Technology

Wafer processing is often called planar processing or planar technology because small and thin planar structures are built on thin wafers (~ 500 μm thick) of ultra pure silicon or germanium or any other suitable semi-conductor material. The thin wafers are cut from a rod of pure material, which is a single crystal, and then polished. The structures built on the surface of the wafer are electrical components such as resistors, capacitors, diodes, junction transistors, MOSFET transistors, etc. Each wafer contains 200 to 500 chips, with each chip identical to the others.

In any wafer fabrication process, the surface region of the wafer undergoes a number of processing steps involving changes in chemical composition and physical state, as well as the controlled deposition of material on the wafer's surface. Typically, the thickness of the layers of material may be from 0.1 μm to 1 μm thick while the width and length of the characteristic features within the layers, which define the dimensions of each electrical component, are a few microns. For 1 Megabit RAMs the dimensions are now less than 1.7 μm. The control of the processing steps must be extremely precise in order to make a uniform product from chip to chip. A simple example of the manufacture of a component

is the capacitor. A capacitor can be made by locally oxidizing the semiconductor substrate, which is silicon here, to silicon dioxide. Whereas silicon is a semiconductor, silicon dioxide is an excellent insulator. If the thin layer of SiO_2 separates a conductor, such as a metal contact, from the semiconductor, then a capacitor is formed. Electrical contact to the semiconductor material can be made in a variety of ways, e.g., by etching an opening in the silicon dioxide and providing a metal contact there. Transistors are more complex in structure than capacitors and depend on the particular design of the transistor. Figure 1 shows a cross-section of a bipolar npn transistor which uses silicon dioxide as an isolator to separate it from other electrical components on the wafer's surface. There are, of course, a variety of ways to isolate electrical components so that the variety of different designs of components is numerous. As a consequence, the fabrication processes are also very different.

Unit Processes in Fabrication

In any wafer fabrication process, the surface region of the wafer undergoes a large number of lithographic, etching, deposition and other physical and chemical processes. The complexity of a process for a given type of chip is impressive. In the training of process engineers, it makes little sense to study the whole manufacturing process for each type of product, since any manufacturing process can be divided into a series of steps or unit processes. The basic principles of each unit process are for the most part independent of the material or the characteristics of the system in which the process is carried out. In the understanding of an integrated circuit manufacturing process, each unit process used to manufacture the product can be studied individually. In chemical engineering processes, the unit processes are often called "unit operations". Traditionally, in chemical engineering, the restriction to the definition of unit operations is that the changes induced in the material are mainly physical (1). In the manufacture of integrated circuits, many of the unit processes involve mainly chemical changes so perhaps the term unit processes is more appropriate here. The important types of unit processes common to the manufacture of integrated circuits are listed in Table I. Not included are the unit processes used to manufacture masks, or the unit processes used to produce some of the materials necessary in the manufacturing process, such as the important unit processes of filtration of air and water purification. The unit processes listed may be subdivided. For example, in the unit process, "implantation", either diffusion and ion implantation can be used. Under the term, "dry etching", we can find unit processes such as gas etching, plasma etching, and reactive ion milling. Further, some overlap of the categories listed in Table 1 does exist.

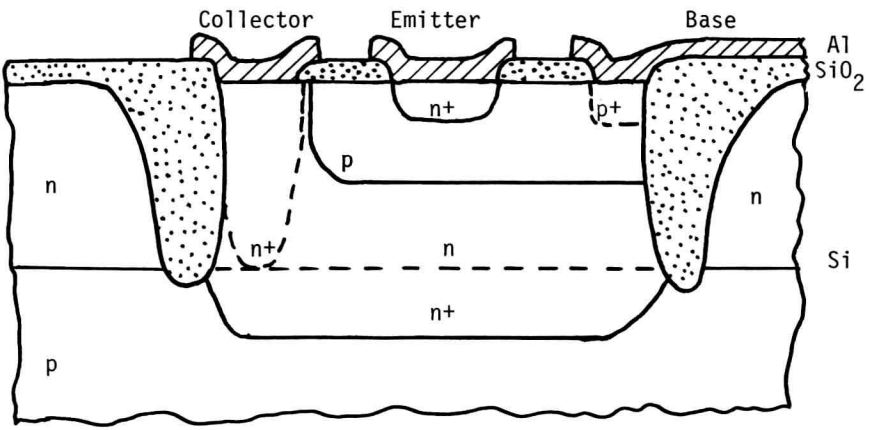

Figure 1. Example of a bipolar npn transistor. The figure shows a cross section of the silicon wafer. Symbols are: AL, aluminum; Si, silicon; SiO_2, silicon dioxide; and n and p, the doped regions of the silicon.

Table I. Categories of Unit Processes

1. Single Crystal Processess	2. Imaging Processes
a) Silica purification b) crystallization from melt c) melt doping d) zone refining e) slicing and polishing	a) coating b) baking c) exposure d) development
3. Etching and Cleaning Processes	4. Deposition and Growth Processes
a) wet etching b) dry etching	a) oxidation b) epitaxy c) implantation d) evaporation e) sputtering f) lift-off g) plasma deposition h) chemical vapor deposition
5. Assembly and Packaging	
a) testing b) scribing c) dicing d) lead attachment e) encapsulation	
6. Miscellaneous	
a) Laser-annealing	

It is instructive to consider an example of the manufacture of a typical component such as the MOS (metal-oxidide-semiconductor) transistor. Figure 2 gives a broad outline of how a p-channel MOS transistor is manufactured. Starting with a smooth and clean wafer of n-type silicon, the surface is first oxidized by exposing the wafer to oxygen gas and/or water vapor at high temperatures (~1200°C). Usually a layer of silicon dioxide approximately 1 μm thick is grown. Another process that can be used is chemical vapor deposition in which silicon dioxide is deposited from a reactive vapor phase. This latter process can be operated at a considerably lower temperature than that required for thermal oxidation and is often preferred. Silicon oxidation phenomena are well-understood (2,3) and reaction conditions can be easily designed to obtain the appropriate silicon dioxide thickness.

After the oxide layer has been grown, a thin layer of photoresist is applied to the wafer's surface. The photoresist is a radiation-sensitive polymeric solution. It contains a complex mixture of photo-sensitive molecules and solvents. The layer of photoresist must be very thin, of the order of two microns, and spin coating is a process that is used to obtain a uniform layer

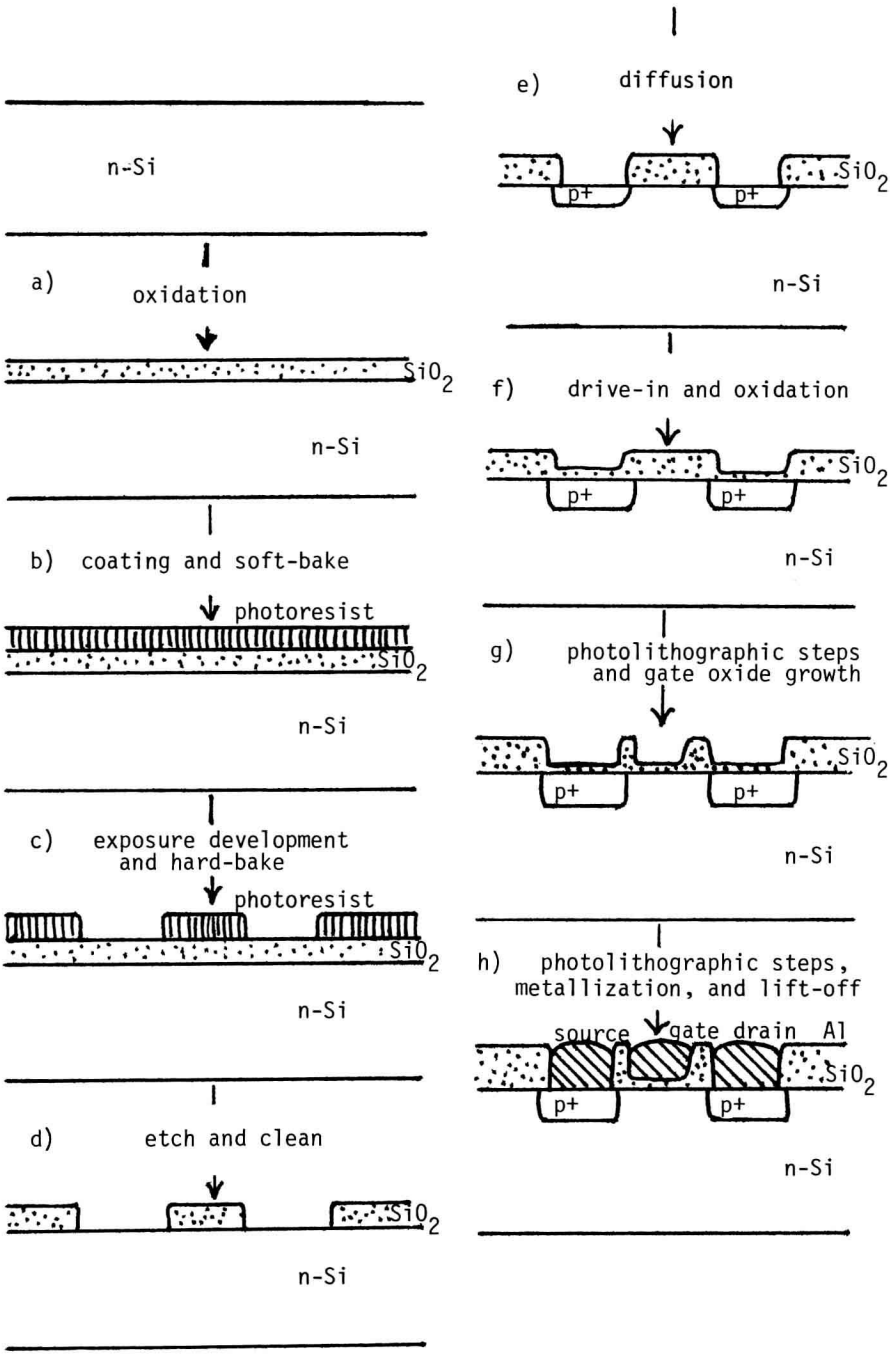

Figure 2. Schematic diagram of the fabrication of a p-channel MOS transistor.

of photoresist on the surface. In this coating process a controlled volume of photoresist is placed on the center of the wafer after which the wafer is spun at high speed (3000-8000 rpm) in order to spread and thin the liquid photoresist uniformly on the wafer. The fluid mechanics of the spin coating process is complex and is not fully understood because of several factors: the speed of the rotating wafer is ramped; the photoresist solution may be non-Newtonian; evaporation of solvent takes place simultaneously with the momentum transfer process. A review article on the problem has been given (4) and mathematical models have appeared in the literature (5).

After spin coating the wafer is baked to remove excess solvent from the photoresist. The baking conditions are mild (~ 90°C) and the process is, therefore, called soft-baking. The drying of the photoresist improves its photosensitivity to radiation, and increases adherence to the thin film layer. Next, the photoresist is selectively exposed using an image pattern transfer technique. For example, in proximity printing, a mask is placed very near to the photoresist and exposed with ultra violet light through the non-opaque areas. There are many other exposure techniques such as optical projection, electron beam writing, and x-ray exposure. After exposure, the development process depends on the type of photoresist (6). For negative photoresist, the exposed areas have undergone polymerization. Unexposed areas can be dissolved in the developer solution. Although some components are similar, positive resists are different from negative resists in the chemistry of the resist and developer, and the resist response to exposure. For positive photoresist, the exposed areas become soluble in the developer solution. After development, the pattern is cleaned by a spray rinse and then the wafer is hard-baked. The baking temperatures can be around 200°C causing the photoresist to harden and adhere firmly to the surface of the substrate. The lithographic steps of spin coating the photoresist, soft-baking, exposure, and development, are always necessary as the first step in transferring the circuit pattern from the mask to the wafer. Insufficient information on these processes is available in the open literature because the composition of photoresists are proprietary. Photoresist manufacturers usually supply guidelines to set processing conditions (7). After development, the silicon dioxide that is not covered by photoresist can now be etched away by either a wet etching or dry etching process. In wet etching, a reactive solution causes dissolution of the unprotected silicon dioxide layer. Wet etching involves a moving-boundary phenomenon, and in recent years new mathematical models for this type of problem have given a better insight into the physics of the process (8). In dry etching a plasma gas reacts with the silicon dioxide and the products are vaporized at vacuum conditions. Dry etching with plasmas is used extensively in processing, but considerable research is still in progress to understand the detailed chemistry and process parameters (9).

The etching process results in removal of the silicon dioxide in the selected areas defined, for example, by the clear or opaque areas in the mask outlining the circuit pattern, so that the silicon is exposed.

After removal of the photoresist by a cleaning or stripping process, the exposed areas of the silicon can be doped with phosboron or other dopants to change the semicondutor from n-type to p-type in the openings of silicon dioxide (for the example shown in Figure 2). High temperature diffusion or ion-implantation can be used as the unit processes to dope the surface areas. Diffusion of impurities into solids is well-understood (10). Ion implantation is rapidly becoming a mature unit process (11). The advantage of this process is that it is carried out at considerably lower temperatures than the diffusion process although some thermal annealing may be required. Further drive-in of the purity and oxidation of the silicon can be achieved by heating the wafer in the presence of oxygen gas and/or water vapor.

Additional photolithographic steps similar to those discussed earlier are necessary to reopen the silicon dioxide covering source and drain areas above the p-type regions and to create a very thin silicon-dioxide layer below the gate area. The next step involves deposition of a metal such as aluminum to form the contacts for the source, gate and drain. Finally, an interconnection pattern is defined to connect the transistor with other electrical components on the surface. The transistors are now finished and the wafers proceed to other processing operations.

Process Flow-Sheet

The process described in the previous section can be shown as a flow-sheet as depicted in Figure 3. The figure shows the sequential nature of each of the unit processes with the repetition of the photolithographic or imaging steps involving coating, baking, exposure and development. Flow-sheets for other devices would be quite similar to Figure 3 in that similar unit processes would be employed. The particular sequence of operations may differ. Further, in any manufacturing process there is usually a choice of several unit processes that can be used to produce a particular product. For example, etching can be carried out by a wet etching or dry etching process. As far as deposition and growth processes are concerned, the unit processes in epitaxy, plasma deposition and chemical vapor deposition are extensively used to deposit other layers such as silicon nitride and polysilicon.

The process flow-sheet does not show the unit processes in preparing the wafer, nor the final assembly and packaging processes. With higher and higher density chips, the assembly and packaging may prove to be a bottleneck. The choice of a particular unit process depends on a variety of factors including experience in using the process and economics.

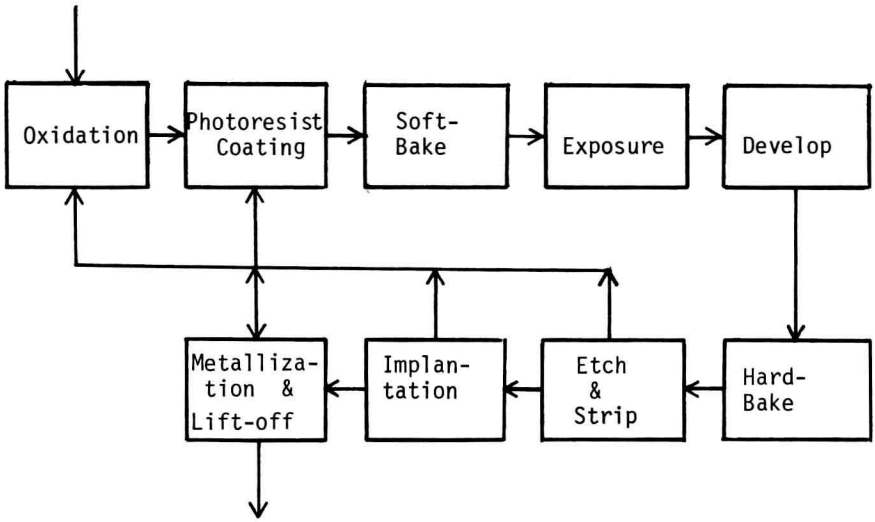

Figure 3. Process flow-sheet for the MOS transistor depicted in Figure 2. Direction of arrows allows for the repetition of several lithographic processes.