intel

MICROCONTROLLER HANDBOOK

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1986

About Our Cover:

The design on our front cover is an abstract portrayal of the control function of a microcontroller. The center sphere contains a symbolic microcontroller guiding multi-levels of remote controlled applications around the outside of the design. Microcontrollers are improving the quality and capabilities of the end product; Intel microcontrollers do more, so you can do more.

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Introduction to MCS®-96

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CHAPTER 1
INTRODUCTION TO MCS®-96

1.0 MCS-96 SECTION ORGANIZATION

The MCS-96 family of microcontrollers is composed of the 8096 series of components and the 8096BH series. The 8096BH parts are fully compatible with the 8096 parts while offering enhanced functionality and the option of on-chip EPROM.

The following five chapters describe the MCS-96 family. To provide a convenient means of reference for those already familiar with the products, each chapter is a free standing module which covers one aspect of design. For those not already familiar with the 8096, reading the chapters in the order they appear will present a logical and complete presentation of the MCS-96 family of products.

Chapter 1 presents an introduction to the MCS-96 product family.

An Architectural Overview, contained in Chapter 2, provides the operational description of each of the hardware units on the chip. Information in this chapter will be of interest to anyone technically involved with an 8096 design.

The Software Design section, Chapter 3, provides information which will primarily interest those people who will write programs to execute in the 8096.

The Hardware Design section, Chapter 4, provides the hardware engineer with all the information needed to connect external hardware to the 8096.

Chapters 3 and 4 are both written assuming the reader is familiar with the information contained in Chapter 2.

Data sheets for the MCS-96 parts are contained in Chapter 5. The first data sheet describes the 8096 series of parts. The second one describes the 8096BH series of parts. The final data sheet is for the Express series of parts, those that have been burned-in and/or tested for an extended temperature range.

1.1 CONTINUING MICROCONTROLLER EVOLUTION

Beginning with the introduction of the world standard 8048 (MCS®-48) Microcontroller in 1976, Intel has continued to drive the evolution of single chip microcontrollers. In 1980, Intel introduced the 8051 (MCS-51) offering

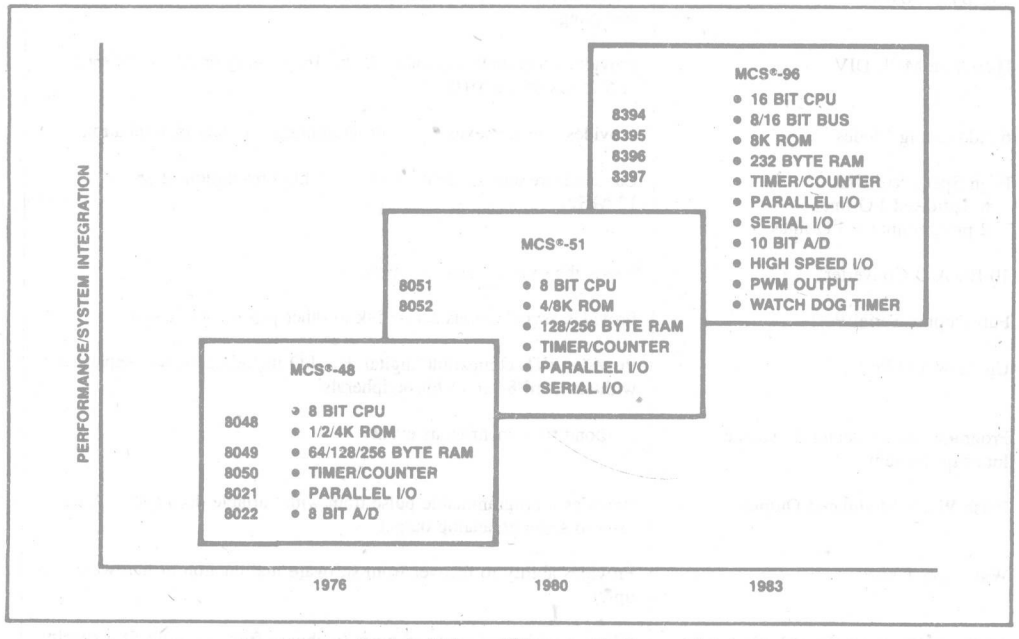

Figure 1-1. Evolution of Microcontrollers at Intel

performance levels significantly higher than the 8048. With the advent of the 8051, the microcontroller applications base took a marked vertical leap. These versatile chips are used in applications from keyboards and terminals to controlling automobile engines. The 8051 quickly gained the position of the second generation world standard microcontroller.

Now that the semiconductor process technologies are being pushed to new limits, it has become possible to integrate more than 100,000 transistors onto a single silicon chip. Microcontroller designers at Intel have taken today's process technology achievements and forged a new generation of single chip microcontrollers called the MCS-96. The 8096 (generic part number for MCS-96) offers the highest level of system integration ever achieved on a single chip microcontroller. It uses over 120,000 transistors to implement a high performance 16-bit CPU, 8K bytes of program memory, 232 bytes of data memory and both analog and digital types of I/O features. Figure 1-1 shows the evolution of single chip microcontroller at Intel.

1.2 INTRODUCTION TO THE MCS®-96

The 8096 consists of a powerful 16-bit CPU tightly coupled with program and data memory along with several I/O features all integrated onto a single piece of silicon. The CPU supports bit, byte, and word operations. 32-bit double words are also supported for a subset of the instruction set. With a 12 MHz input frequency, the 8096 can perform a 16-bit addition in 1.0 μs and 16 x 16 multiply or 32/16 divide in 6.25 μs.

The 8096BH allows the external bus width to be run-time configured to operate as a standard 16-bit multiplexed address/data bus or an 8088 minimum mode type bus.

Table 1-1 MCS®-96 Features and Benefits Summary

FEATURES	BENEFITS
16-Bit CPU	Efficient machine with higher throughput.
Dynamically Reconfigurable Bus	Select 8-bit or 16-bit bus width.
8K Bytes ROM	Large program space for more complex, larger programs.
232 Bytes RAM	Large on-board register file for data storage and fast context switching.
Hardware MUL/DIV	Provides good math capability 16 by 16 multiply or 32 by 16 divide in 6.25 μs @ 12 MHz.
6 Addressing Modes	Provides greater flexibility of programming and data manipulation.
High Speed I/O Unit 6 dedicated I/O lines 2 programmable I/O lines	Can measure and generate pulses with high resolution (2 μs @ 12 MHz).
10-Bit A/D Converter	Reads the external analog inputs.
Full Duplex Serial Port	Provides asynchronous serial link to other processors or systems.
Up to 40 I/O Ports	Provides TTL compatible digital data I/O including system expansion with standard 8- or 16-bit peripherals.
Programmable 8 vector/21 source Interrupt System	Respond to asynchronous events.
Pulse Width Modulated Output	Provides a programmable pulse train with variable duty cycle. Also used to generate analog output.
Watchdog Timer	Provides ability ro recover from software malfunction or hardware upset.
48-Pin (DIP) & 68-Pin (Plastic Leaded Chip Carrier, Pin Grid Array) Versions	Offers a variety of package types to choose from to better fit a specific application need for number of I/O lines and package size.

Four high-speed trigger inputs are provided to record the times at which external events occur with a resolution of 2 μs (at 12 MHz crystal frequency). Up to six high-speed pulse generator outputs are provided to trigger external events at preset times. The high speed output unit can simultaneously perform software timer functions. Up to four such 16-bit software timers can be in operation at once in addition to the two 16-bit hardware timers.

An optional on-chip A/D converter converts up to eight analog input channels into 10-bit digital values. Also provided on-chip, are a serial port, a watchdog timer, and a pulse-width modulated output signal. Table 1.1 shows the features and benefits summary for the MCS-96.

The 8096 with its 16-bit CPU and all the I/O features and interface resources on a single piece of silicon represents the highest level of system integration in the world of microcontrollers. It will open up new applications which had to use multiple chip solutions in the past.

Table 1-2 MCS®-96 Broad Base of Applications

INDUSTRIAL
Motor Control
Robotics
Discrete and Continuous Process Control
Numerical Control
Intelligent Transducers
INSTRUMENTATION
Medical Instrumentation
Liquid and Gas Chromatographs
Oscillioscopes
CONSUMER
Video Recorder
Laser Disk Drive
High-end Video Games
GUIDANCE & CONTROL
Missile Control
Torpedo Guidance Control
Intelligent Ammunition
Aerospace Guidance Systems
DATA PROCESSING
Plotters
Color and B&W Copiers
Winchester Disk Drive
Tape Drives
Impact and Non-Impact Printers
TELECOMMUNICATIONS
Modems
Intelligent Line Card Control
AUTOMOTIVE
Ignition Control
Transmission Control
Anti Skid Braking
Emission Control

1.3. MCS®-96 APPLICATIONS

The MCS-96 products are stand-alone high performance single chip microcontrollers designed for use in sophisticated real-time demanding applications such as industrial control, instrumentation and intelligent computer peripherals. The wide base of applications cut across all industry segments (see table 1.2). With the 16-bit CPU horsepower, high-speed math processing and high-speed I/O, the 8096 is ideal for complex motor control and axis control systems. Examples include three phase, large horsepower AC motors and robotics.

With its 10-bit A/D converter option, the device finds usage in data acquisition systems and closed-loop analog controllers. It permits considerable system integration by combining analog and digital I/O processing in the single chip.

This chip is ideally suited in the area of instrumentation products such as gas chromatographs, which combine analog processing with high speed number crunching. The same features make it a desirable component for aerospace applications like missile guidance and control.

1.4. MCS®-96 FAMILY DEVELOPMENT SUPPORT TOOLS

The product family is supported by a range of Intel software and hardware development tools. These tools shorten the product development cycle, thus bringing the product to the market sooner.

1.4.1. MCS®-96 Software Development Package

The 8096 software development package provides development system support specifically designed for the MCS-96 family of single chip microcontrollers. The package consists of a symbolic macro assembler ASM-96, Linker/Relocator RL-96 and the librarian LIB-96. Among the high level language, PLM-96 is offered along with a floating point math package. A real-time executive software package, the iDCX-96 is also available. Additional high level languages are being developed for the MCS-96 product family.

1.4.2. ASM-96 MACRO Assembler

The 8096 macro assembler translates the symbolic assembly language instructions into the machine executable object code. ASM-96 enables the programmer to write the program in a modular fashion. The modular programs divide a rather complex program into smaller functional units, that are easier to code, to debug, and to change. The separate modules can then be linked and located into one program module using the RL-96 utility. This utility

combines the selected input object modules into a single output object module. It also allocates memory to input segments and binds the relocatable addresses to absolute addresses. It then produces a print file that consists of a link summary, a symbol table listing and an intermediate cross-reference listing. LIB-96, another utility helps to create, modify, and examine library files. The ASM-96 runs on Intellec Series III or IV.

1.4.3. PL/M-96

The PL/M-96 compiler translates the PL/M-96 language into 8096 relocatable object modules. This allows improved programmer productivity and application reliability. This high level language has been efficiently designed to map into the machine architecture, so as not to trade off higher programmer productivity with inefficient code. Since the language and the compiler are optimized for the 8096 and its application environment, developing software with PL/M-96 is a 'low-risk' project.

1.4.4. iDCX-96

The iDCX-96 is an executive software package useful in multi-tasking environments. Up to 16 user tasks can be handled. The iDCX-96 is ideal for the customer who must quickly develop software for a multi-tasking, real-time environment.

1.4.5. Hardware Development Support: VLSICE-96

The VLSICE-96 is based on Intel's state-of-the-art bond-out technology. It permits full access to the internal bus and control timing cycles for true real-time emulation. The VLSICE-96 is controlled by either an Intellec series III/IV or an IBM PC/XT/AT or compatible over a serial link.

The VLSICE-96 provides total development support for MCS-96 microcontroller designs. It supports full speed real time emulation. A comprehensive break/trace capability allows for the specification of complex, multi-level events.

1.4.6. Hardware Development Support: SBE-96

The iSBE-96 is a hardware execution and debug tool for the MCS-96 products. It consists of a monitor/debugger resident in an 8096 system. This development system interfaces with the user's 8096 system via two ribbon cables, one for the 8096 I/O ports, and the other for the memory bus. The iSBE-96 is controlled by an Intellec Series III, IBM PC or compatible, or other computer system over a serial link. Power for the iSBE-96 can be supplied by plugging it into the MULTIBUS® card slot, or by an external power supply. The iSBE-96 is contained on one standard MULTIBUS board.

The iSBE-96 provides the most often used features for real-time hardware emulation. The user can display and modify memory, set up break points, execute with or without breakpoints and change the memory map. In addition, the user can single step through the system program.

1.4.7. MCS®-96 Workshop

The workshop provides the design engineer or system designer hands-on experience with the MCS-96 family of products. The course includes an explanation of the Intel 8096 architecture, system timing, input/output design. The lab sessions allow the attendees to gain in-depth knowledge of the MCS-96 product family and support tools.

1.4.8. Insite™ Library

The Intel Insite Library contains several application programs. A very useful program contained in the Insite is SIM-96, the software simulator for 8096. It allows software simulations of user's system. The simulator provides the ability to set breakpoints, examine and modify memory, disassemble the object code and single step through the code.

1.5. MCS®-96 FAMILY OF PRODUCTS

Although 8096 is the generic part number often used for the MCS-96 products throughout this manual, the product family consists of eight configurations with eight part numbers including the 8096. This wide variety of products is offered to best meet user's application requirements in terms of number of I/O's and package size. The options include on-board 8K bytes of mask programmed memory, 10-bit A/D converter, and 48 or 68 pin package type.

The 48-pin components are similar to the 68-pin versions except that the following pins are not available:

Port 0	4 of 8 analog/digital input pins
Port 1	8 general purpose I/O pins
Port 2	4 of 8 general/special function pins (the special functions are available through other pins)
Control	CLKOUT, INSTruction, NMI, TEST (BUSWIDTH on 8096BH)

Table 1-3 summarizes all the current products in the MCS®-96 product family.

Table 1-3 MCS®-96 Family of Products

OPTIONS		68-PIN	48-PIN
DIGITAL I/O	ROMLESS	8096	8094
	ROM	8396	8394
	EPROM	*8796	8794
ANALOG AND DIGITAL I/O	ROMLESS	8097	8095
	ROM	8397	8395
	EPROM	*8797	8795

The 48 pin version is available in a DIP (dual inline) package.

The 68 pin version comes in two packages, the Plastic Leaded Chip Carrier and the Pin Grid Array.

*The 68-pin version of the 879x is available in a Leaded Chip Carrier and a ceramic Pin Grid Array. The L.C.C. is socket foot print compatible with PLCC.

Architectural Overview 2

CHAPTER 2
ARCHITECTURAL OVERVIEW

2.0. INTRODUCTION

The 8096 can be separated into several sections for the purpose of describing its operation. There is a CPU, a programmable High Speed I/O Unit, an analog to digital converter, a serial port, and a Pulse Width Modulated (PWM) output for digital to analog conversion. In addition to these functional units, there are some sections which support overall operation of the chip such as the clock generator and the back-bias generator. The CPU and the programmable I/O make the 8096 very different from any other microcontroller, let us first examine the CPU.

2.1. CPU OPERATION

The major components of the CPU on the 8096 are the Register File and the RALU. Communication with the outside world is done through either the Special Function Registers (SFRs) or the Memory Controller. The RALU (Register/Arithmetic Logic Unit) does not use an accumulator, it operates directly on the 256-byte register space made up of the Register File and the SFRs. Efficient I/O operations are possible by directly controlling the I/O through the SFRs. The main benefits of this structure are the ability to quickly change context, the absence of accumulator bottleneck, and fast throughput and I/O times.

2.1.1. CPU Buses

A "Control Unit" and two buses connect the Register File and RALU. Figure 2-1 shows the CPU with its major bus connections. The two buses are the "A-Bus" which is 8-bits wide, and the "D-Bus" which is 16-bits wide. The D-Bus transfers data only between the RALU and the Register File or Special Function Registers (SFRs). The A-Bus is used as the address bus for the above transfers or as a multiplexed address/data bus connecting to the "Memory Controller". Any accesses of either the internal ROM or external memory are done through the Memory Controller.

Within the memory controller is a slave program counter (Slave PC) which keeps track of the PC in the CPU. By having most program fetches from memory referenced to

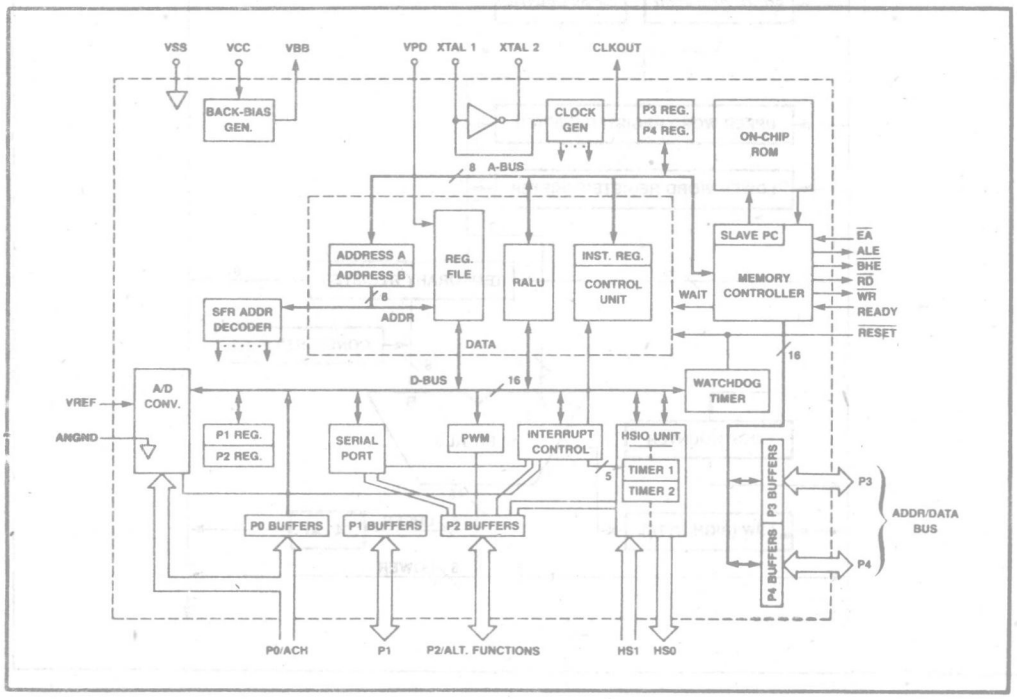

Figure 2-1. Block Diagram (For simplicity, lines connecting port registers to port buffers are not shown.)