

Nanoscale CMOS

*Innovative Materials,
Modeling and Characterization*

**Edited by
Francis Balestra**

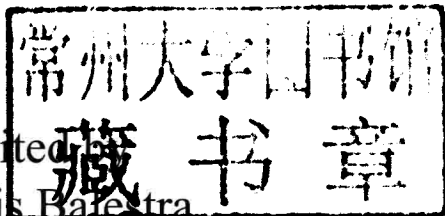
ISTE

 **WILEY**

Nanoscale CMOS

*Innovative Materials, Modeling
and Characterization*

Edited by
Francis Balestra



ISTE

 WILEY

First published 2010 in Great Britain and the United States by ISTE Ltd and John Wiley & Sons, Inc.

Apart from any fair dealing for the purposes of research or private study, or criticism or review, as permitted under the Copyright, Designs and Patents Act 1988, this publication may only be reproduced, stored or transmitted, in any form or by any means, with the prior permission in writing of the publishers, or in the case of reprographic reproduction in accordance with the terms and licenses issued by the CLA. Enquiries concerning reproduction outside these terms should be sent to the publishers at the undermentioned address:

ISTE Ltd
27-37 St George's Road
London SW19 4EU
UK

www.iste.co.uk

John Wiley & Sons, Inc.
111 River Street
Hoboken, NJ 07030
USA

www.wiley.com

© ISTE Ltd 2010

The rights of Francis Balestra to be identified as the author of this work have been asserted by him in accordance with the Copyright, Designs and Patents Act 1988.

Library of Congress Cataloging-in-Publication Data

Nanoscale CMOS: innovative materials, modeling, and characterization / edited by Francis Balestra.
p. cm.

Includes bibliographical references and index.

ISBN 978-1-84821-180-3

1. Metal oxide semiconductors, Complementary--Materials. I. Balestra, Francis.

TK7871.99.M441545 2010

621.39'732--dc22

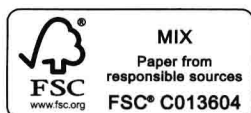
2010012627

British Library Cataloguing-in-Publication Data

A CIP record for this book is available from the British Library

ISBN: 978-1-84821-180-3

Printed and bound in Great Britain by CPI Antony Rowe, Chippenham and Eastbourne.



Nanoscale CMOS

Introduction

Microelectronics, based on CMOS (complementary metal oxide semiconductor) technology, is the essential hardware enabler for electronic product and service innovation in key growth markets, such as communications, calculating, consumer electronics, automotive, avionics, automated manufacturing, health and environment. The global semiconductor industry underpins 16% of the world's total economy and is growing every year. The worldwide market for electronic products is estimated at more than \$1,100 billion, and the related electronics services market at more than \$6,500 billion. These product and service markets are enabled by a \$280 billion market for semiconductor components and an associated \$80 billion market for semiconductor equipment and materials. The new era of nanoelectronics, which started at the beginning of the current millennium with the smallest patterns in state-of-the-art silicon-based devices below 100 nanometers, is enabling an exponential increase in system complexity and functionality.

Nanoelectronics enables the development of smart electronic systems by switching, storing, receiving and transmitting information. In respect to its societal relevance, the ubiquitous nanoelectronics is also closely linked to the notion of ambient intelligence, which is a vision of the future where people are surrounded by intelligent intuitive interfaces that are embedded in all kinds of objects and an environment that is capable of recognizing and responding to the presence of different individuals in a seamless way.

Since the invention of the transistor in 1947 at Bell Labs, followed by the first silicon transistor in 1954 and the concept of integrated circuits in 1958 in Texas Instruments, progress in the field of microelectronics has been tremendous, which has revolutionized the society. In these last 50 years, dramatic advances have been achieved in the packing density of transistors, resulting since the 1970s in a density of transistors on an integrated chip (IC) will doubles every two years (Moore's law). At the beginning of the 1970s, the first microprocessor had only about 2,000

transistors (10 μm gate length), the world's first two-billion transistor processor was reported in 2008 in 65 nm CMOS technology. The technology node will drop down to 9 nm in 2024. Meanwhile, development goes on apace with the 32 nm node coming on stream in late 2009. Today, the annual fabrication of MOSFET (metal oxide semiconductor field effect transistor) per person is about one billion.

The same trend is observed for memories. The DRAM (dynamic random access memory) capacity has been raised from 1 kb in 1970 to more than 2 Gb at present. Three billion transistor SRAM test chips have also been recently announced. For nonvolatile memories, a recent record of 64 Gb has been demonstrated. This increase in transistor count and memory capacity has led to increased processing power, measured now in thousands of MIPS (millions of instructions per second).

A dramatic increase in the transistor performance, measured as the ON to OFF ratio of drain current in DC mode, while lowering the supply voltage, has been obtained during recent decades. In AC mode, cut-off frequencies of several hundred GHz have been recently measured in bulk and SOI (silicon-on-insulator) CMOS technologies.

Moore's law also means decreasing cost per function, the transistor price has dropped at an average rate of about 1.5 per year (about 10^8 since the beginning of the semiconductor industry).

However, according to the International Technology Roadmap for Semiconductors [ITR 09] and ENIAC Strategic Research Agenda [SRA 07], there are big challenges to overcome in order to continue progress in the same direction. Si will remain the main semiconductor material for the foreseeable future, but the required performance improvements for the end of the roadmap for high performance, low and ultra-low power applications as well as memories will lead to a substantial enlargement of the number of new materials, technologies and device architectures.

SOI substrates are interesting candidates for the manufacturing of mainstream semiconductor products such as microprocessors, low-power devices or memories [CRI 09]. The classic CMOS architecture is approaching its scaling limits, "end-of-roadmap" alternative devices are also being investigated. Amongst the different types of SOI-based devices proposed, one clearly stands out for the end of the roadmap: the multigate field-effect transistor (multigate- or double-gate- or gate-all-around- or Fin-FET), enabling better electrostatic control of the channel(s), hence a more aggressive scalability and reduced leakage currents, higher driving currents and speed, reduced variability and enriched functionality. The

International Technology Roadmap for Semiconductors recognizes the importance of these devices.

In the sub-10 nm range, “beyond-CMOS” devices, based on nanowires, nanodots, carbon electronics or other nanodevices, could play an important role and could be integrated on CMOS platforms in order to pursue integration down to nanometer structures.

Therefore, new generations of nanoelectronic ICs present increasingly formidable multidisciplinary challenges at the most fundamental level (novel materials, new physical phenomena, ultimate technological processes, etc.). This long-term research is fundamental to prepare the path for future nanoelectronic technologies, as a 15 to 20 year time frame is usually necessary between the first validation of a new innovative idea and its full demonstration and acceptance into complex systems.

The three parts of this book have been written by scientists, from universities and research centers, strongly involved in teaching and research programs related to nanoelectronic devices; because of their expertise and international commitment, they are very well informed on the state-of-the-art of the physics and technologies and the evolution of nanoelectronic materials and components.

This book offers a comprehensive review of the state-of-the-art in innovative materials, advanced modeling and novel characterization methods for nanoscale CMOS dedicated to researchers, engineers and students. In the field of new materials, which has been a major drive to find new ways to enhance the performance of semiconductor technologies, this text covers three areas that will provide a dramatic impact on the approaches to future CMOS – global and local strained and alternative materials for high-speed channels on bulk substrate and insulator, very low access resistance and various high dielectric constant gate stacks for power scaling. It also focuses on the most reliable modeling and simulation methods of the electrical properties of ultimate MOSFETs, including ballistic transport, gate leakage, atomistic simulation and compact models for single- and multi-gate devices, nanowire and carbon-based FETs. Finally, the book presents an in-depth investigation of the main nanocharacterization techniques for an accurate determination of transport parameters, interface defects, channel strain as well as RF properties, including capacitance-conductance, improved split C-V, magnetoresistance, charge pumping, low frequency noise and Raman spectroscopy.

Part 1 reviews some of the progress being made in the key areas of new materials for nanoscale transistors that could be incorporated in future technology nodes. Chapter 2 focuses on general issues of high- k dielectrics and metal gates, and points out a range of different materials that will be able to circumvent fundamental

limitations in various applications. Chapter 3 reviews the current state-of-the-art for strained silicon and then discuss the route to higher strain and Ge channels, based on global strain tuning buffers. Interesting approaches for the realization of thin virtual substrates and strained silicon on oxide (SSOI) wafers and devices are described in Chapter 4. The conversion of the biaxial strain to uniaxial strain in order to develop nanowire FETs is also shown. The objective of Chapter 5 was to introduce recent developments in the field of Schottky barrier engineering and integration in nonconventional MOSFET architectures. Low temperature dopant segregation at the silicide-semiconductor interface is also analysed as a useful methodology to lower the barrier height. Practical implementation scenarios are described for *p*- and *n*-type devices and both static and high frequency performances of Schottky-barrier MOSFETs are also presented.

Part 2 outlines some of the progress being made in the key areas of simulation of nanoscale transistors including the simulation of drain and gate leakage currents, the role of alternative channel materials, the application of a full-quantum transport approach in the simulation of ultimate silicon nanodevices, the progress in the field of compact models for nano-CMOS and the advanced simulation approaches for beyond-CMOS devices. Chapter 7 illustrates how to calculate gate current in non conventional devices such as double gate SOI MOSFETs and addresses the problem of analyzing tunneling in 2D and 3D devices. An overview about trap-assisted tunneling is given. Finally, a comparison between different approaches for gate current computation applied to a template gate stack featuring high-*k* dielectric is reported. In Chapter 8, the general semi-classic modeling framework for drain current computation is introduced together with the methodology for the derivation of the moments of the Boltzmann transport equation. A systematic comparison of drain current simulations for long channel as well as nano scale MOSFETs obtained either with the Monte Carlo method or with the moment-based models is also addressed. In Chapter 9, the results of the theoretical evaluation of the performance of ultra-scaled nMOSFET with alternative channel material are presented. Both results from efficient and accurate semi-analytical models and by using state-of-the-art simulation tools are investigated. The simplicity of analytical models enable a better understanding of the relative importance of the various mechanisms which contribute to the overall device performance. Chapter 10 deals with the investigation of interface roughness and random discrete dopants, and related variability in nanoscale MOSFETs, which requires fully 3D quantum transport simulations. Then, we review and present several recent developments in compact modeling of nanoscale MOSFETs, in particular multigate devices. Electrostatic and transport modeling issues as well as the development of unified charge control models for different types of multigate MOSFETs are considered. Specific compact modeling issues for ultimate MOSFETs, including velocity saturation, channel length modulation, ballistic transport and quantum confinement, are also discussed. In Chapters 11 and 12, two different types of beyond-CMOS devices, based on carbon

nanotubes or graphene and gate-all-around transistors based on silicon or 3C silicon carbide nanowires, are analyzed using 3D device simulator able to solve the full band Schrödinger equation with open boundary conditions in the nonequilibrium Green's function (NEGF) framework coupled with the 3D Poisson equation.

In Part 3, the main nanocharacterization techniques for nanoscale devices are investigated. Chapter 14 shows the need to develop a reliable extraction method for transport parameters, which is playing a key role in device performance, and to correlate these electrical properties to materials and processing options. The aim of this chapter is to give an overview of how standard extraction methods have been progressively adapted to account for MOS transistors evolution, what their limits are, and which alternative methods may be used for highly scaled structures. In Chapter 15, we consider accurate methods for characterizing the density and energy distribution of interface states and trap density in the semiconductor/oxide system using measurements of capacitance or conductance of MOS structures, as well as charge pumping and low frequency noise. Chapter 16 shows the methods leading to a reliable evaluation of the channel strain for future nanoscale CMOS. In Chapter 17, we point out the importance of an accurate wideband characterization technique, well adapted to advanced MOS devices, in order to understand their static and dynamic behaviors, and thus to monitor and optimize the fabrication process steps for further reducing the impact of parasitic elements.

Francis BALESTRA

Acknowledgements

We would like to acknowledge David Leadley for coordinating Part 1, Enrico Sangiorgi for coordinating Part 2, and Denis Flandre for coordinating Part 3 of the book. All the Members of the Sinano Institute and the Partners of the Nanosil and Sinano Networks of Excellence are also gratefully acknowledged for their support.

Bibliography

- [CRI 09] CRISTOLOVEANU S. and BALESTRA F., "Introduction to SOI technology and transistors", in J. GAUTIER (Ed.), *Physics and Operation of Silicon Devices and Integrated Circuits*, ISTE-Wiley, London, UK, New York, USA, 2009.
- [ENI 07] <http://www.eniac.eu/web/downloads/SRA2007.pdf>
- [ITR 09] <http://www.itrs.net/Links/2009ITRS/Home2009.htm>

Table of Contents

Introduction	xv
F. BALESTRA	
PART 1. NOVEL MATERIALS FOR NANOSCALE CMOS	1
Chapter 1. Introduction to Part 1	3
D. LEADLEY, A. DOBBIE, V. SHAH and J. PARSONS	
1.1. Nanoscale CMOS requirements	3
1.2. The gate stack – high- κ dielectrics	5
1.3. Strained channels	7
1.3.1. Carrier mobility	7
1.3.2. Introducing strain	10
1.3.3. Global strain	10
1.3.4. Local strain	12
1.3.5. Strained layers on insulator	14
1.3.6. Alternative channel materials	15
1.4. Source-drain contacts	16
1.5. Bibliography	17
Chapter 2. Gate Stacks	23
O. ENGSTRÖM, I. Z. MITROVIC, S. HALL, P. K. HURLEY, K. CHERKAOUI, S. MONAGHAN, H. D. B. GOTTLOB and M. C. LEMME	
2.1. Gate-channel coupling in MOSFETs	23
2.2. Properties of dielectrics	24
2.2.1. The effect of polarization	24
2.2.2. Energy offset and k -values	26
2.2.3. Structural stability and reactivity	27

2.3. Interfaces states and bulk oxide traps	29
2.3.1. Energy distributions of interface states	29
2.3.2. Physical properties of interface states: capture cross-sections . . .	32
2.3.3. Electron states in transition regions	34
2.3.4. Bulk traps	35
2.4. Two ternary compounds: GdSiO and LaSiO	39
2.4.1. GdSiO	39
2.4.2. LaSiO	45
2.5. Metal gate technology	50
2.5.1. The metal/oxide barrier	51
2.5.2. FUSI NiSi metal gate technology for rapid material screening . . .	52
2.5.3. Gate-first integration of TiN metal gate electrodes	54
2.5.4. AlN buffer layer technology for tuning of mid-gap metal work function	55
2.6. Future outlook	56
2.7. Bibliography	58
Chapter 3. Strained Si and Ge Channels	69
D. LEADLEY, A. DOBBIE, M. MYRONOV, V. SHAH and E. PARKER	
3.1. Introduction	69
3.1.1. State-of-the-art strained silicon devices	69
3.1.2. Modulation doping results	72
3.2. Relaxation of strained layers	74
3.2.1. Critical thickness	74
3.2.2. Characterization of the degree of relaxation	75
3.2.3. Characterizing the threading dislocation density (TDD)	77
3.2.4. Supercritical highly tensile strained Si	80
3.3. High Ge composition $\text{Si}_{1-x}\text{Ge}_x$ buffers	83
3.3.1. Global strain platforms	83
3.3.2. Forward linear grading	85
3.3.3. Terrace-graded buffers	88
3.3.4. TDD reduction for forward graded buffers	90
3.3.5. Low temperature epitaxy for thin buffers	93
3.3.6. Reverse grading for high Ge content substrates	94
3.3.7. Ge condensation	100
3.4. Ge channel devices	105
3.4.1. Gate stack	106
3.4.2. Relaxed Ge p-channel devices	107
3.4.3. Relaxed Ge n-channel devices	109
3.4.4. Strained Ge devices	109
3.4.5. SiGe alloy channel MOSFETs	113
3.5. Acknowledgements	115
3.6. Bibliography	115

Chapter 4. From Thin Si/SiGe Buffers to SSOI	127
S. MANTL and D. BUCA	
4.1. Introduction	128
4.2. Nucleation of dislocations	129
4.3. Strain relaxation and strain transfer mechanisms	131
4.4. Overgrowth of strained Si and layer optimization	134
4.4.1. Growth of strained Si on a thin seed layer	134
4.4.2. Defect density reduction by strain adjusted Si/Si _{1-y} Ge _y heteroepitaxy	135
4.5. Characterization of the elastic strain	137
4.5.1. Raman spectroscopy	138
4.5.2. He ion channelling	139
4.6. SSOI wafer fabrication	141
4.6.1. Wafer bonding	141
4.6.2. Wafer splitting and layer transfer	142
4.6.3. Selective etching and epitaxial Si on SSOI growth	144
4.7. SSOI as channel material for MOSFET devices	145
4.7.1. High mobility long channel devices	145
4.7.2. SSOI mobility extraction	146
4.7.3. Effective electron mass in biaxial tensile SSOI	148
4.7.4. Uniaxial strained nanowires (NWs)	150
4.8. Summary	152
4.9. Bibliography	153
 Chapter 5. Introduction to Schottky-Barrier MOS Architectures: Concept, Challenges, Material Engineering and Device Integration	157
E. DUBOIS, G. LARRIEU, R. VALENTIN, N. BREIL and F. DANNEVILLE	
5.1. Introduction	157
5.2. Challenges associated with the source/drain extrinsic contacts	158
5.2.1. Source/drain resistance: critical role of the silicide/semiconductor interface	158
5.2.2. Schottky source/drain in advanced MOS architectures	162
5.2.3. Schottky barrier height and Fermi level pinning	164
5.3. Extraction of low Schottky barriers	166
5.3.1. Usual measurement techniques and their limitations	166
5.3.2. Measurement strategy for low Schottky barrier height	169
5.3.3. Current transport model at the Schottky interface	171
5.3.4. Model application and validation	176
5.4. Modulation of Schottky barrier height using low temperature dopant segregation	177
5.4.1. Towards sub-0.1eV Schottky barriers	177
5.4.2. History of dopant segregation	179
5.4.3. Electrostatics of dopant segregation	180

5.4.4. Practical implementation of dopant segregation	181
5.4.5. Dopant segregation applied to a p-type band-edge silicide PtSi . .	182
5.4.6. Dopant segregation applied to n-type band-edge silicides ErSi _{2-x} YbSi _{2-x}	188
5.5. State-of-the-art device integration	191
5.5.1. <i>n</i> -type SB-MOSFETs	191
5.5.2. <i>p</i> -type SB-MOSFETs	192
5.5.3. High-frequency performance	193
5.6. Conclusion	195
5.7. Acknowledgements	197
5.8. Bibliography	197
PART 2. ADVANCED MODELING AND SIMULATION FOR NANO-MOSFETs AND BEYOND-CMOS DEVICES	205
Chapter 6. Introduction to Part 2	207
E. SANGIORGI	
6.1. Modeling and simulation approaches for gate current computation . . .	208
6.2. Modeling and simulation approaches for drain current computation . . .	209
6.3. Modeling of end of the roadmap nMOSFET with alternative channel material	209
6.4. NEGF simulations of nanoscale CMOS in the effective mass approximation	210
6.5. Compact models for advanced CMOS devices	211
6.6. Beyond CMOS	211
6.7. Bibliography	212
Chapter 7. Modeling and Simulation Approaches for Gate Current Computation	213
B. MAJKUSIAK, P. PALESTRI, A. SCHENK, A. S. SPINELLI, C. M. COMPAGNONI and M. LUISIER	
7.1. Introduction	213
7.2. Calculation of the tunneling probability	216
7.3. Tunneling in nonconventional devices	228
7.3.1. Gate tunnel current in DG-SOI structures	228
7.3.2. 3D/2D tunneling in Si nanowire FETs and DG SOI FETs	233
7.4. Trap-assisted tunneling	237
7.5. Models for gate current computation in commercial TCAD	243
7.5.1. Fowler-Nordheim tunneling model	244
7.5.2. Direct tunneling model	244
7.5.3. Nonlocal tunneling model	247
7.6. Comparison between modeling approaches	249
7.7. Bibliography	251

Chapter 8. Modeling and Simulation Approaches for Drain Current Computation	259
M. VASICEK, D. ESSENI, C. FIEGNA and T. GRASSER	
8.1. Boltzmann transport equation for MOS transistors	260
8.2. Method of moments	262
8.2.1. Modeling of the scattering operator	264
8.2.2. Macroscopic models	264
8.3. Subband macroscopic transport models	276
8.3.1. The model	277
8.3.2. The quantum correction model	278
8.4. Comparison with device-SMC	278
8.4.1. Long channel device	279
8.4.2. Short channel devices	280
8.5. Conclusions	282
8.6. Bibliography	283
 Chapter 9. Modeling of End of the Roadmap nMOSFET with Alternative Channel Material	287
Q. RAFHAY, R. CLERC, G. GHIBAUDO, P. PALESTRI and L. SELMI	
9.1. Introduction: replacing silicon as channel material	287
9.2. State-of-the-art in the modeling of alternative channel material devices	290
9.2.1. Detailed literature review of the modeling of alternative channel material device	290
9.2.2. Summary of the main conclusion drawn in the literature	295
9.3. Critical analysis of the literature using analytical models	297
9.3.1. On state current of alternative channel material nMOSFET as a function of transport and substrate orientation	297
9.3.2. Issues in the modeling of the off state leakage current	303
9.3.3. Modeling the performances of alternative channel material nMOSFET in the fully ballistic limit	310
9.3.4. Conclusions	317
9.3.5. Role of the scattering in alternative channel materials: the case of electron transport in germanium channel	317
9.4. Conclusions	327
9.5. Bibliography	328
 Chapter 10. NEGF for 3D Device Simulation of Nanometric Inhomogeneities	335
A. MARTINEZ, A. ASENOV and M. PALA	
10.1. Introduction	335
10.1.1 Introduction	335
10.1.2. The 3D real space NEGF formulation (F3D)	336

10.1.3. The coupled mode space approach (CMS)	338
10.1.4. Comparisom between CMS and F3D	338
10.2. Variabilities for nanoscale CMOS	343
10.2.1. Poisson-NEGF loop	343
10.2.2. Random discrete dopants in 3D	345
10.3. Full quantum treatment of spatial fluctuations in ultra-scaled devices	361
10.3.1. Introduction	361
10.3.2. Models and methods	361
10.3.3. Surface roughness effects on silicon nanowire FETs	365
10.3.4. Remote Coulomb scattering in silicon nanowire FETs	370
10.3.5. Surface roughness effects on SOI double gate FETs	375
10.4. Bibliography	377

Chapter 11. Compact Models for Advanced CMOS Devices 381

B. INIGUEZ, F. LIME, A. LÁZARO and T. A. FJELDLY

11.1. Introduction	381
11.2. Electrostatics modeling issues	385
11.3. Transport modeling issues	388
11.4. 1D compact models	390
11.4.1. Undoped symmetric DG MOSFET modeling	390
11.4.2. Undoped cylindrical GAA MOSFET	395
11.4.3. Doped multigate MOSFETs	398
11.4.4. FinFET modeling	399
11.4.5. Asymmetric DG MOSFET	401
11.5. Ultimate MuGFET modeling issues: ballistic current and quantum confinement	405
11.6. Velocity saturation and channel length modulation modeling	409
11.7. Hydrodynamic transport model	411
11.8. Charge and capacitance modeling	413
11.8.1. Undoped symmetric DG MOSFET	414
11.8.2. Cylindrical gate-all-around MOSFETs	417
11.8.3. Independently biased DG MOSFET	418
11.9. Short-channel effects	420
11.9.1. Double-gate MOSFET	422
11.9.2. Cylindrical gate-all-around MOSFETs	424
11.9.3. FinFETs	426
11.9.4. 2D modeling based on conformal mapping	426
11.10. RF and noise modeling	434
11.11. Acknowledgements	437
11.12. Bibliography	438

Chapter 12. Beyond CMOS	443
G. IANNACCONI, G. FIORI, S. REGGIANI and M. PALA	
12.1. Introduction	443
12.2. Atomistic modeling of carbon-based FETs	444
12.3. Numerical simulation of CNT-FETs	447
12.4. Effective mass modeling of carbon nanotube FETs	451
12.4.1. Theory	452
12.4.2. Effective-mass model with nonparabolic corrections versus TB results	455
12.5. CNT versus graphene nanoribbon FETs	459
12.6. Full-quantum treatment of elastic and inelastic scattering in Si and SiC GAA nanowire FETs	461
12.6.1. Numerical methods and physical models	461
12.6.2. Channel-length dependence of low-field mobility	463
12.6.3. Comparison between Si and 3C-SiC nanowire FETs	466
12.7. Conclusions	467
12.8. Bibliography	468
PART 3. NANOCHARACTERIZATION METHODS	471
Chapter 13. Introduction to Part 3	473
D. FLANDRE	
Chapter 14. Accurate Determination of Transport Parameters in Sub-65 nm MOS Transistors	475
M. MOUIS and G. GHIBAUDO	
14.1. Impact of transport on device performance in the drift-diffusion regime	476
14.1.1. Underlying MOS transistor model	476
14.1.2. Mobility model	478
14.1.3. Effective field	480
14.1.4. Series resistance	481
14.2. Standard extraction techniques and their adaptation to short channel transistors	482
14.2.1. Gate oxide capacitance: C_{ox} and L_{eff} extraction	482
14.2.2. Parameter extraction from static characteristics: the Y-function method	490
14.2.3. Improved Y-function method for thin EOTs	493
14.2.4. Improved methods for series resistance extraction	500
14.2.5. Reduction of measurement noise	503
14.2.6. The standard split C-V method	503
14.2.7. Improved split C-V for short channel transistors	508
14.2.8. Influence of temperature	515

14.2.9. Range of application and limits of previous methods	517
14.3. Alternative extraction techniques	518
14.3.1. Magneto transport	518
14.3.2. Differential magnetoresistance	525
14.3.3. Piezoresistance	527
14.4. Out of equilibrium transport	531
14.4.1. Drain current expression in the quasi-ballistic regime	532
14.4.2. The apparent mobility concept	535
14.5. Conclusions	537
14.6. Bibliography	539
Chapter 15. Characterization of Interface Defects	545
P. HURLEY, O. ENGSTRÖM, D. BAUZA and G. GHIBAUDO	
15.1. Characterization using the capacitance-voltage (C-V) response	545
15.2. Characterization using the conductance-voltage (G-V) response	550
15.3. Charge pumping	553
15.3.1. Basic CP features, CP curves, and D_{it} extraction	553
15.3.2. D_{it} versus energy, $D_{it}(E)$, profiles	556
15.3.3. D_{it} extraction on various devices types	557
15.3.4. CP and device degradation	557
15.3.5. Si-SiO ₂ interface trap properties	558
15.3.6. CP curve simulation	559
15.3.7. Case of high- κ gate stacks	560
15.4. Low frequency noise	561
15.4.1. Theoretical background	561
15.4.2. Diagnostic of LF noise sources and trap density extraction	562
15.5. Bibliography	566
Chapter 16. Strain Determination	575
A. O'NEILL, S. OLSEN, P. DOBROSZ, R. AGAIBY and Y. TSANG	
16.1. Introduction	575
16.2. Characterization requirements	575
16.3. Characterization techniques	579
16.3.1. Wafer bowing	579
16.3.2. X-ray diffraction (XRD)	579
16.3.3. Ellipsometry	579
16.3.4. Electron diffraction	580
16.3.5. Raman Spectroscopy	582
16.4. Strain description	592
16.5. Bibliography	598