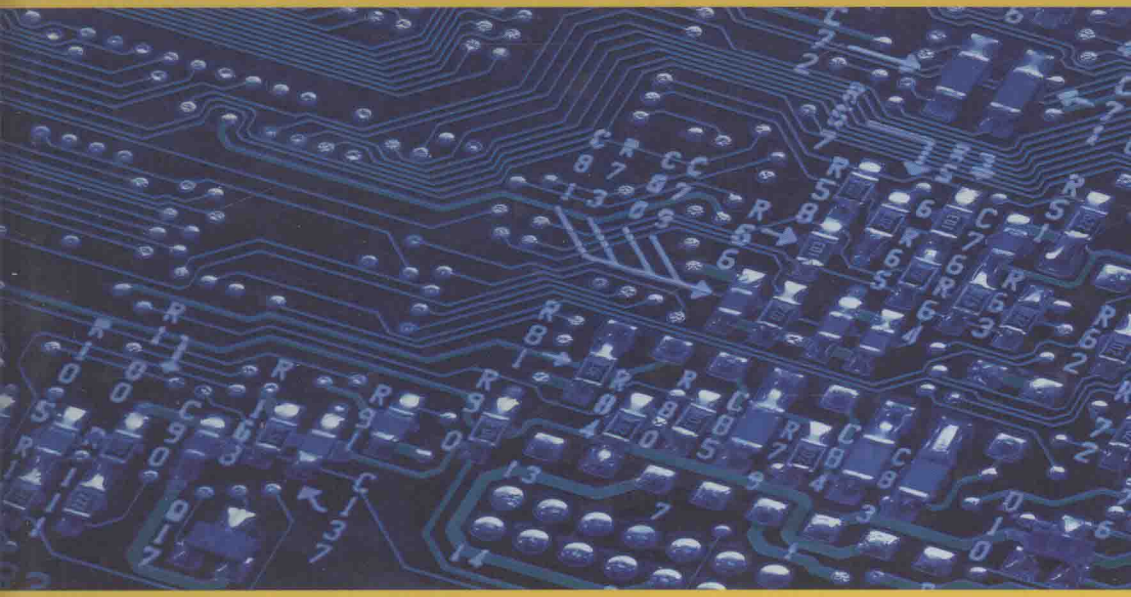

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Innovative Materials, Modeling and Characterization

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First published 2010 in Great Britain and the United States by ISTE Ltd and John Wiley & Sons, Inc.

ISTE Ltd
27-37 St George's Road
London SW19 4EU
UK

www.iste.co.uk

John Wiley & Sons, Inc.
111 River Street
Hoboken, NJ 07030
USA

www.wiley.com

Library of Congress Cataloging-in-Publication Data

Nanoscale CMOS: innovative materials, modeling, and characterization / edited by Francis Balestra.
p. cm.
Includes bibliographical references and index.
ISBN 978-1-84821-180-3
1. Metal oxide semiconductors, Complementary--Materials. I. Balestra, Francis.
TK7871.99.M44I545 2010
621.39'732--dc22

2010012627

British Library Cataloguing-in-Publication Data
A CIP record for this book is available from the British Library
ISBN: 978-1-84821-180-3

Printed and bound in Great Britain by CPI Antony Rowe, Chippenham and Eastbourne.

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Introduction

Microelectronics, based on CMOS (complementary metal oxide semiconductor) technology, is the essential hardware enabler for electronic product and service innovation in key growth markets, such as communications, calculating, consumer electronics, automotive, avionics, automated manufacturing, health and environment. The global semiconductor industry underpins 16% of the world's total economy and is growing every year. The worldwide market for electronic products is estimated at more than $1,100 billion, and the related electronics services market at more than $6,500 billion. These product and service markets are enabled by a $280 billion market for semiconductor components and an associated $80 billion market for semiconductor equipment and materials. The new era of nanoelectronics, which started at the beginning of the current millennium with the smallest patterns in state-of-the-art silicon-based devices below 100 nanometers, is enabling an exponential increase in system complexity and functionality.

Nanoelectronics enables the development of smart electronic systems by switching, storing, receiving and transmitting information. In respect to its societal relevance, the ubiquitous nanoelectronics is also closely linked to the notion of ambient intelligence, which is a vision of the future where people are surrounded by intelligent intuitive interfaces that are embedded in all kinds of objects and an environment that is capable of recognizing and responding to the presence of different individuals in a seamless way.

Since the invention of the transistor in 1947 at Bell Labs, followed by the first silicon transistor in 1954 and the concept of integrated circuits in 1958 in Texas Instruments, progress in the field of microelectronics has been tremendous, which has revolutionized the society. In these last 50 years, dramatic advances have been achieved in the packing density of transistors, resulting since the 1970s in a density of transistors on an integrated chip (IC) will doubles every two years (Moore's law). At the beginning of the 1970s, the first microprocessor had only about 2,000

transistors (10 μm gate length), the world's first two-billion transistor processor was reported in 2008 in 65 nm CMOS technology. The technology node will drop down to 9 nm in 2024. Meanwhile, development goes on apace with the 32 nm node coming on stream in late 2009. Today, the annual fabrication of MOSFET (metal oxide semiconductor field effect transistor) per person is about one billion.

The same trend is observed for memories. The DRAM (dynamic random access memory) capacity has been raised from 1 kb in 1970 to more than 2 Gb at present. Three billion transistor SRAM test chips have also been recently announced. For nonvolatile memories, a recent record of 64 Gb has been demonstrated. This increase in transistor count and memory capacity has led to increased processing power, measured now in thousands of MIPS (millions of instructions per second).

A dramatic increase in the transistor performance, measured as the ON to OFF ratio of drain current in DC mode, while lowering the supply voltage, has been obtained during recent decades. In AC mode, cut-off frequencies of several hundred GHz have been recently measured in bulk and SOI (silicon-on-insulator) CMOS technologies.

Moore's law also means decreasing cost per function, the transistor price has dropped at an average rate of about 1.5 per year (about 10^8 since the beginning of the semiconductor industry).

However, according to the International Technology Roadmap for Semiconductors [ITR 09] and ENIAC Strategic Research Agenda [SRA 07], there are big challenges to overcome in order to continue progress in the same direction. Si will remain the main semiconductor material for the foreseeable future, but the required performance improvements for the end of the roadmap for high performance, low and ultra-low power applications as well as memories will lead to a substantial enlargement of the number of new materials, technologies and device architectures.

SOI substrates are interesting candidates for the manufacturing of mainstream semiconductor products such as microprocessors, low-power devices or memories [CRI 09]. The classic CMOS architecture is approaching its scaling limits, "end-of-roadmap" alternative devices are also being investigated. Amongst the different types of SOI-based devices proposed, one clearly stands out for the end of the roadmap: the multigate field-effect transistor (multigate- or double-gate- or gate-all-around- or Fin-FET), enabling better electrostatic control of the channel(s), hence a more aggressive scalability and reduced leakage currents, higher driving currents and speed, reduced variability and enriched functionality. The

International Technology Roadmap for Semiconductors recognizes the importance of these devices.

In the sub-10 nm range, "beyond-CMOS" devices, based on nanowires, nanodots, carbon electronics or other nanodevices, could play an important role and could be integrated on CMOS platforms in order to pursue integration down to nanometer structures.

Therefore, new generations of nanoelectronic ICs present increasingly formidable multidisciplinary challenges at the most fundamental level (novel materials, new physical phenomena, ultimate technological processes, etc.). This long-term research is fundamental to prepare the path for future nanoelectronic technologies, as a 15 to 20 year time frame is usually necessary between the first validation of a new innovative idea and its full demonstration and acceptance into complex systems.

The three parts of this book have been written by scientists, from universities and research centers, strongly involved in teaching and research programs related to nanoelectronic devices; because of their expertise and international commitment, they are very well informed on the state-of-the-art of the physics and technologies and the evolution of nanoelectronic materials and components.

This book offers a comprehensive review of the state-of-the-art in innovative materials, advanced modeling and novel characterization methods for nanoscale CMOS dedicated to researchers, engineers and students. In the field of new materials, which has been a major drive to find new ways to enhance the performance of semiconductor technologies, this text covers three areas that will provide a dramatic impact on the approaches to future CMOS – global and local strained and alternative materials for high-speed channels on bulk substrate and insulator, very low access resistance and various high dielectric constant gate stacks for power scaling. It also focuses on the most reliable modeling and simulation methods of the electrical properties of ultimate MOSFETs, including ballistic transport, gate leakage, atomistic simulation and compact models for single- and multi-gate devices, nanowire and carbon-based FETs. Finally, the book presents an in-depth investigation of the main nanocharacterization techniques for an accurate determination of transport parameters, interface defects, channel strain as well as RF properties, including capacitance-conductance, improved split C-V, magnetoresistance, charge pumping, low frequency noise and Raman spectroscopy.

Part 1 reviews some of the progress being made in the key areas of new materials for nanoscale transistors that could be incorporated in future technology nodes. Chapter 2 focuses on general issues of high-k dielectrics and metal gates, and points out a range of different materials that will be able to circumvent fundamental

limitations in various applications. Chapter 3 reviews the current state-of-the-art for strained silicon and then discuss the route to higher strain and Ge channels, based on global strain tuning buffers. Interesting approaches for the realization of thin virtual substrates and strained silicon on oxide (SSOI) wafers and devices are described in Chapter 4. The conversion of the biaxial strain to uniaxial strain in order to develop nanowire FETs is also shown. The objective of Chapter 5 was to introduce recent developments in the field of Schottky barrier engineering and integration in nonconventional MOSFET architectures. Low temperature dopant segregation at the silicide-semiconductor interface is also analysed as a useful methodology to lower the barrier height. Practical implementation scenarios are described for *p*- and *n*-type devices and both static and high frequency performances of Schottky-barrier MOSFETs are also presented.

Part 2 outlines some of the progress being made in the key areas of simulation of nanoscale transistors including the simulation of drain and gate leakage currents, the role of alternative channel materials, the application of a full-quantum transport approach in the simulation of ultimate silicon nanodevices, the progress in the field of compact models for nano-CMOS and the advanced simulation approaches for beyond-CMOS devices. Chapter 7 illustrates how to calculate gate current in non conventional devices such as double gate SOI MOSFETs and addresses the problem of analyzing tunneling in 2D and 3D devices. An overview about trap-assisted tunneling is given. Finally, a comparison between different approaches for gate current computation applied to a template gate stack featuring high-*k* dielectric is reported. In Chapter 8, the general semi-classic modeling framework for drain current computation is introduced together with the methodology for the derivation of the moments of the Boltzmann transport equation. A systematic comparison of drain current simulations for long channel as well as nano scale MOSFETs obtained either with the Monte Carlo method or with the moment-based models is also addressed. In Chapter 9, the results of the theoretical evaluation of the performance of ultra-scaled nMOSFET with alternative channel material are presented. Both results from efficient and accurate semi-analytical models and by using state-of-the-art simulation tools are investigated. The simplicity of analytical models enable a better understanding of the relative importance of the various mechanisms which contribute to the overall device performance. Chapter 10 deals with the investigation of interface roughness and random discrete dopants, and related variability in nanoscale MOSFETs, which requires fully 3D quantum transport simulations. Then, we review and present several recent developments in compact modeling of nanoscale MOSFETs, in particular multigate devices. Electrostatic and transport modeling issues as well as the development of unified charge control models for different types of multigate MOSFETs are considered. Specific compact modeling issues for ultimate MOSFETs, including velocity saturation, channel length modulation, ballistic transport and quantum confinement, are also discussed. In Chapters 11 and 12, two different types of beyond-CMOS devices, based on carbon

nanotubes or graphene and gate-all-around transistors based on silicon or 3C silicon carbide nanowires, are analyzed using 3D device simulator able to solve the full band Schrödinger equation with open boundary conditions in the nonequilibrium Green's function (NEGF) framework coupled with the 3D Poisson equation.

In Part 3, the main nanocharacterization techniques for nanoscale devices are investigated. Chapter 14 shows the need to develop a reliable extraction method for transport parameters, which is playing a key role in device performance, and to correlate these electrical properties to materials and processing options. The aim of this chapter is to give an overview of how standard extraction methods have been progressively adapted to account for MOS transistors evolution, what their limits are, and which alternative methods may be used for highly scaled structures. In Chapter 15, we consider accurate methods for characterizing the density and energy distribution of interface states and trap density in the semiconductor/oxide system using measurements of capacitance or conductance of MOS structures, as well as charge pumping and low frequency noise. Chapter 16 shows the methods leading to a reliable evaluation of the channel strain for future nanoscale CMOS. In Chapter 17, we point out the importance of an accurate wideband characterization technique, well adapted to advanced MOS devices, in order to understand their static and dynamic behaviors, and thus to monitor and optimize the fabrication process steps for further reducing the impact of parasitic elements.

Francis BALESTRA

Acknowledgements

We would like to acknowledge David Leadley for coordinating Part 1, Enrico Sangiorgi for coordinating Part 2, and Denis Flandre for coordinating Part 3 of the book. All the Members of the Sinano Institute and the Partners of the Nanosil and Sinano Networks of Excellence are also gratefully acknowledged for their support.

Bibliography

[CRI 09] CRISTOLOVEANU S. and BALESTRA F., "Introduction to SOI technology and transistors", in J. GAUTIER (Ed.), *Physics and Operation of Silicon Devices and Integrated Circuits*, ISTE-Wiley, London, UK, New York, USA, 2009.

[ENI 07] http://www.eniac.eu/web/downloads/SRA2007.pdf

[ITR 09] http://www.itrs.net/Links/2009ITRS/Home2009.htm

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