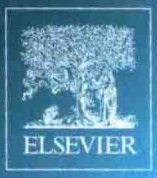

Third Edition

Edited by
Krishna Seshan

Handbook of Thin Film Deposition

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Techniques, Processes, and Technologies

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Handbook of Thin Film Deposition

Techniques, Processes, and Technologies

To my many teachers,
particularly Dr. David Dew-Hughes, teacher,
tutor, mentor, and friend.

Foreword

Gordon E. Moore

Increasingly, any reference to the current technology for the manufacture of integrated circuits as "semiconductor technology" is a misnomer. By now, the processing relating to the silicon itself contributes relatively few steps to the total while the various processes associated with the deposition and patterning of the increasing number of metal and insulating films have grown in importance. Where the first metal-oxide-transistor circuits of the 1960s took five masking steps to complete, and even early silicon-gate circuits with single metal layer interconnections took only seven, modern circuits with as many as six layers of metal take well in excess of twenty. Not only are there more layers but also the composition of those layers is often complex. Metal conduction layers might require barrier films to prevent interdiffusion or to enhance adhesion. Insulators not only isolate circuit elements electrically but are also used to prevent ions from harming the electrical properties of the transistors. In fact, if the technology for integrated circuit manufacture as practiced today were named for the majority of the processing steps, the technology could probably be more accurately described as *thin-film technology*.

Consistent with this change, the processing for the deposition and patterning of films has received major research and engineering emphasis and has evolved rapidly over the last few decades. Whereas in the 1960s, thermal oxidation or vapor deposition was sufficient for the insulators and evaporation or sputtering of aluminum took care of the needs for conductors, a large variety of sophisticated deposition techniques have since grown with the industry. Today, one can control both the electrical and the mechanical properties while achieving uniform and reproducible films from a few atomic layers thick to several micrometers. The chemistry and physics of the films are becoming increasingly better understood, but as they are, the demands of the device designer are becoming more stringent. For example, whereas the dielectric constant of silicon oxide-based insulators was accepted as a design parameter to live with for 30 years or so, capacitance associated with interconnections can now be a real limitation on circuit performance. Designers want an insulator with all the good properties they have come to love with SiO_2, but with a dielectric constant as close to that of a vacuum as possible. Similarly, with conductors no one will be happy until we have room-temperature superconducting films in multilayered structures.

The simple furnaces and evaporators of yesteryear have become multichamber creations of stainless steel that allow a series of processes to be done without exposing the work to air. The lithography machines for creating the desired precise and fine-scaled patterns now cost several million dollars each as the industry pushes the limits of optical systems in the continuing pursuit of performance and small size.

The cumulative investment in developing and improving processes must exceed a hundred billion dollars by now. Such a huge investment of money and technical talent has created a vast amount of knowledge, much of which is summarized in this volume.

The film technology developed primarily for the silicon integrated circuit industry is finding its way into several other areas of application. It has become a general technology for designing and constructing complex structures, layer by layer. Microelectromechanical devices use the same deposition and patterning techniques. Microfluidic gadgets with microsized pipes, valves, and all the plumbing necessary to make tiny chemical factories or analytical laboratories are increasingly important and again use the film technologies that grew up around semiconductor integrated circuits. Even the gene chips the biotech industry use to speed up their analysis come from the same bag of tricks.

This book takes a snapshot of the state of the art in various technologies relating to thin films. It brings together in one convenient location a collection of the research results that have been gathered by many groups over the last few decades. It will be something that the concerned engineer will return to time after time in the course of his or her work. This is the forefront of science and process engineering with important bearing on many modern industries.

Originally Published in Second Edition (2001)

Preface

No editor undertakes the reediting of a handbook lightly. However, the following reasons compel a reexamination and the addition of new chapters. The reason and the new organization are described below.

The semiconductor industry has undergone a sea change since the publication of the second edition (*Handbook of Thin Film Deposition*) in 2001. At that time, the 130 nm (0.13 μm) technology node was still being researched; most of the production was on 450 nm (0.45 μm). Optical lithography—with many doubts as to its longevity—of line and space below 100 nm (0.1 μm) was used with 8 in. wafers. Aluminum–copper (Al–Cu) interconnects—sometimes with tungsten (W) plugs insulated by plasma-enhanced chemical vapor deposition (PECVD-Oxide)—defined interconnect technology. Although IBM had developed lead (Pb) bumps (IBM C4 Process), wire bonding was used extensively for input-output in most other companies. Single-core 3 GHz processors were then current. Today, processors use strained layers to enhance p-channel mobility, while optical lithography seems to have no limit. Interconnects have changed entirely, with copper damascene defining both the interconnect and the via. Lead-free bumps on 12 in. wafers with 22 nm line and space width using optical lithography are the industry standard. Multicore processors have made the GHz benchmark obsolete, and computers are more efficient in thermal management than a decade ago.

This third edition is devoted to the new films and processes now used in the industry. It offers answers to the pressing question of how continued scaling of printed dimensions influences the choice of both thin-film composition and deposition conditions and equipment. Material new to this edition includes a section on copper interconnect technology, two chapters dealing with current CVD issues comprising a chapter on equipment development, and an entirely new chapter devoted to novel applications of CVD thin films. A whole new section with topics covered include "Optical Thin Films," "Solar Energy Applications," and "Thin Films in Memory Applications." A new chapter on Physical Vapor Deposition (PVD) has also been added.

Rather than a pedagogical textbook, this is a reference book where practicing engineers may get overviews of different aspects of this rapidly developing technical field. To prolong the relevance of this handbook in changing times, both a print and a web edition will be offered; the online version will provide continuing updates, as well as access to many classic chapters from the second edition.

The editor is of the opinion that optical signal transport and switches will have to become a part of the microprocessor, for speed and other benefits. Therefore, a new chapter on Optical Films, by Angus Macleod, has been included.

There are certain topics that intentionally are not covered. These include magnetic thin films for storage, thin films in light emitting diodes, and optical data storage. This is largely because these topics are well covered in other handbooks. Perhaps future editions of this book will include these subjects.

Krishna Seshan
June 2012

Acknowledgments

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Lastly, I must offer apologies to my wife Patricia, who has endured a year of absence and neglect and who continues to provide support.

About the Editor

Dr. K. Seshan has degrees in low-temperature physics (UK) and a PhD in Materials Engineering from the University of California, Berkeley. After teaching at the University of Arizona for 7 years, he worked at IBM and then Intel Corp. His work has largely been in process development and integration of the manufacture process. He is presently retired and involved in University teaching and curriculum development. He serves on the boards of start-ups, does consulting work, and is presently involved in robotic product development and technical writing.

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Contents

THIN FILM DEPOSITION, EQUIPMENT AND PROCESSING

NEW APPLICATIONS