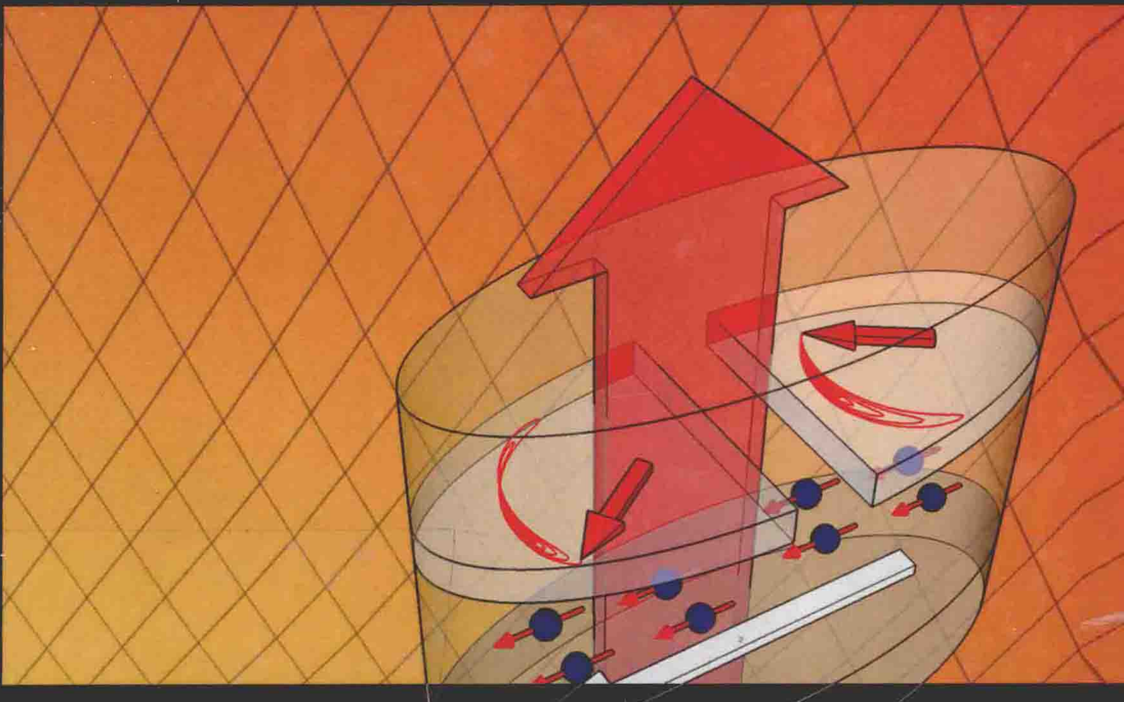
Future Trends in Microelectronics

Frontiers and Innovations

Serge Luryi • Jimmy Xu • Alex Zaslavsky



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FUTURE TRENDS IN MICROELECTRONICS

Preface

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This book is a brainchild of the seventh workshop in the *Future Trends in Microelectronics* series (FTM-7). The first of the FTM conferences, "*Reflections on the Road to Nanotechnology*", had gathered in 1995 on Ile de Bendor, a beautiful little French Mediterranean island.[1] The second FTM, "*Off the Beaten Path*", took place in 1998 on a larger island in the same area, Ile des Embiez.[2] Instead of going to a still larger island, the third FTM, "*The Nano Millennium*", went back to its origins on Ile de Bendor in 2001.[3] As if to compensate for small size of Bendor, the fourth FTM, "*The Nano, the Giga, the Ultra, and the Bio*", took place on the biggest French Mediterranean island of them all, Corsica.[4] Normally, the FTM workshops gather every three years; however, the FTM-4 was held one year ahead of the usual schedule, in the summer of 2003, as a one-time exception. Continuing its inexorable motion eastward, the fifth FTM workshop, "*Up the Nano Creek*", had convened on Crete, Greece, in June of 2006.[5] The inexorable motion was then interrupted to produce a semblance of a random walk in the Mediterranean and the FTM-6 "*Unmapped Roads*" went to the Italian island of Sardinia (June, 2009).[6] The last FTM gathering, "*Into the Cross Currents*", returned to our earlier venue on Corsica (June 2012).

The FTM workshops are relatively small gatherings (less than 100 people) by invitation only. If you, the reader, wish to be invited, please consider following a few simple steps outlined on the conference website. The FTM website at *www.ece.sunysb.edu/~serge/FTM.html* contains links to all past and planned workshops, their programs, publications, sponsors, and participants. Our attendees have been an illustrious lot. Suffice it to say that among FTM participants we find five Nobel laureates (Zhores Alferov, Herbert Kroemer, Horst Stormer, Klaus von Klitzing, and Harold Kroto) and countless others poised for a similar distinction. To be sure, high distinction is not a prerequisite for being invited to FTM, but the ability and desire to bring fresh ideas is. All participants of FTM-7 can be considered authors of this book, which in this sense is a collective treatise.

The main purpose of FTM workshops is to provide a forum for a free-spirited exchange of views, projections, and critiques of current and future directions, among the leading professionals in industry, academia, and government.

For better or worse our civilization is destined to be based on electronics. Ever since the invention of the transistor and especially after the advent of integrated circuits, semiconductor devices have kept expanding their role in our lives. Electronic circuits entertain us and keep track of our money, they fight our wars and decipher the secret codes of life, and one day, perhaps, they will relieve us from the burden of thinking and making responsible decisions. Inasmuch as that day has not yet arrived, we have to fend for ourselves. The key to success is to have a clear vision of where we are heading. In the blinding light of a bright future, the FTM community has remained mindful of the fact that what controlled the past will still control the future – the basic principles of science. Thus, the trendy, red-hot projections of any given epoch deserve and require critical scrutiny.

Some degree of stability is of importance in these turbulent times and should be welcome. Thus, although the very term "*microelectronics*" has been generally re-christened "*nanoelectronics*", we have stuck to the original title of the FTM workshop series.

The present volume contains a number of original papers, some of which were presented at FTM-7 in oral sessions, other as posters. From the point of view of the program committee, there is no difference between these types of contributions in weight or importance. There was, however, a difference in style and focus – and that was intentionally imposed by the organizers. All speakers were asked to focus on the presenter's views and projections of future directions, assessments or critiques of important new ideas/approaches, and *not* on their own achievements. This latter point is perhaps the most distinctive feature of FTM workshops. Indeed, we are asking scientists not to speak of their own work! This has proven to be successful, however, in eliciting powerful and frank exchange. The presenters are asked to be provocative and/or inspiring. Latest advances made and results obtained by the participants are to be presented in the form of posters and group discussions.

Each day of the workshop was concluded by an evening panel or poster session that attempted to further the debates on selected controversial issues connected to the theme of the day. Each such session was chaired by a moderator who invited two or three attendees of his or her choice to lead with a position statement, with all other attendees serving as panelists. The debate was forcefully moderated and irrelevant digressions cut off without mercy. Moderators were also assigned the hopeless task of forging a consensus on critical issues.

To accommodate these principles, the FTM takes a format that is less rigid than usual workshops to allow and encourage uninhibited exchanges and sometimes confrontations of different views. A central theme is designed together with the speakers for each day. Another traditional feature of FTM workshops is a highly informal vote by the participants on the relative importance of various fashionable current topics in modern electronics research. This tradition owes its origin to Horst Stormer, who composed the original set of questions and maintained the results over four conferences. These votes are perhaps too bold and irreverent for general publication, but they are carefully maintained and made available to every new generation of FTM participants. Another traditional vote concerned the best poster. The 2012 winning poster was "Mechanical energy harvesting with piezoelectric nanostructures: Great expectations for autonomous systems" by Gustavo Ardila.

A joyful tradition of FTM meetings is the settling of scientific bets, a custom that dates back to the 1998 wager between Nikolai Ledentsov (pro) and Horst Stormer (con) about the putative future dominance of quantum dot-based lasers – a bet that Horst collected in 2004, at FTM-4. Another risky bet on the future dominance of SOI technology is to be adjudicated at a future (2015) workshop. The precise statement of this "good" bet (worth a six-magnum case of very good champagne) is: by 2015, SOI will cover more than 35% of the CMOS market including memories by value. This bet, proposed by Sorin Cristoloveanu, attracted three cons – Detlev Grützmacher, Dimitris Ioannou, and Enrico Sangiorgi – who will have to divide the spoils, should SOI fail to reach the mark. Several "bad" (penniless) bets that were supposed to be resolved at FTM-7 were put off as premature by the principals. Hopefully, by 2015 it will become clear whether or not "10% of all man-produced light will be white LED" (Michael Shur), "we shall have hi-fi real-time pocket translators" (Hiroshi Iwai), "most cars will have IP addresses" (Jimmy Xu), or "the Si industry will no longer be recognizable and there will be (essentially) no further improvement in devices" (Paul Solomon).

Not every contribution presented at FTM-7 has made it into this book (not for the lack of persistence by the editors). Perhaps most sorely we miss the exciting contribution by David Miller of Stanford University, entitled "The heat death of information processing and why interconnects matter more than logic", in which he illustrated how the energy required by data communication is imposing severe limits on overall information processing, with the demand for communications bandwidth increasing a hundredfold every decade. As a result, he posited very low energy optoelectronics densely integrated with logic as a way of allowing the continued scaling of information processing systems. Abstracts of his and all other presentations can be found on the program webpage, *http://www.ee.sunysb.edu/~serge/ARW-7/program.html*

The FTM meetings are known for the professional critiques – or even demolitions – of fashionable trends, that some may characterize as hype. The previous workshops had witnessed powerful assaults on quantum computing, molecular electronics, and spintronics. This time Michel Dyakonov offered another thorough and conclusive update on quantum computing. It seems that by now most of the hype associated with some of these trends has dissipated and perhaps we can take some credit for the more balanced outlook that has emerged since.

We have grouped all contributions into four chapters: one dealing with transistors and CMOS or CMOS-compatible technology, another with photonics and lasers, and still another with solar cell and energy harvesting. The last chapter collected the contributions focused on fundamental physics and other, less technological subjects. The breakdown could not be uniquely defined, because some papers fit two or even three categories!

To produce a coherent collective treatise out of all of this, the interaction between FTM participants had begun well before their gathering at the workshop. All the proposed presentations were posted on the web in advance and could be subject to change up to the last minute to take into account peer criticism and suggestions. After the workshop is over, these materials (not all of which have made it into this book) remain on the web indefinitely, and the reader can peruse them starting at the *www.ece.sunysb.edu/~serge/FTM.html* home page.

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Finally, the organizers wish to thank all of the contributors to this volume and all the attendees for making the workshop a rousing success.

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CONTENTS

Part I

Innovations in Electronics and Systems

I. Innovations in Electronics and Systems

The incredibly powerful silicon electronics is still full of steam, charging ahead despite the putatively insurmountable barriers and walls (of thermal, power, wiring, and scaling, for example). Equally evident is that the challenges ahead are real, getting greater, and often without a clear answer. One example is transition to EUV lithography, discussed in the chapter by Banine. What are the biggest challenges anticipated and the biggest changes assumed in the existing roadmap? If science is not (yet) the ultimate limit to nanoelectronics, is it manufacturability, discussed in the chapter by Kelly? What are the most desired innovations, and the most disruptive, interesting, and controversial directions? While the drive for ever greater device performance – discussed in a number of chapters devoted to novel memory and logic devices – is becoming prohibitively costly, could the advances in systems and integrated functionalities be sufficiently rewarding to justify and become the next driving force? These questions are addressed in Part I of this book, which opens with an insightful and comprehensive discussion of technology innovation by Kim and Chung, from the innovation powerhouse of Samsung Electronics.

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Technology Innovation, Reshaping the Microelectronics Industry

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1. Introduction

The remarkable evolution of electronics was enabled by the rapidly advancing silicon technology. The performance of such devices as CPUs and memories has improved tremendously over the past 20 years: CPUs improved by a factor of 2,400, DRAM by a factor of 1,000 and NAND Flash by a factor of 32,000. Mobile network speed has also increased by a factor of 840, stimulated by an increased usage of smartphones and tablets, which have grown by 58%[1] and 260%[2] in 2011, respectively. Furthermore, Internet communication traffic is anticipated to increase by 32% annually, with the traffic reaching an order of zeta (10^{21}) bytes by 2015.[3]

These performance improvements have been made possible by silicon technology downscaling, which is nearing the 20 nm node and will soon reach 10 nm. Novel fabrication techniques, structures and materials will be required to continue scaling beyond 10 nm to satisfy the data handling, processing and storage requirements of the future.

Future device development will be constrained by power consumption, in addition to the traditional scaling issues, since faster and higher data handling and processing will unavoidably require a lot of power. For instance, 1.1 petaflop (10^{15}) computing in 2008[4] consumed 2.3 MW power for its operation, so an exascale (10^{18}) system might dissipate an estimated 2.3 GW, roughly equivalent to the electricity produced by two nuclear power plants. Most of this energy is lost in the inefficient metal interconnects, which could be reduced by combining photonics with Si technologies. This silicon-photonics convergence will create new applications and markets in the future.

Furthermore, silicon technology is bringing innovation to new areas, such as energy, health, and medical applications. Examples of this are ultrafast DNA sequencing, extremely compact and efficient medical imaging devices, and low-cost energy-efficient lighting, among others. These applications, fueled by Si technologies, could eventually take up a major portion of the semiconductor market in the next decade.

2. Mainstream silicon technology: Memory

- *Towards sub-20 nm DRAM*

DRAM density has doubled every 18 months through scaling of the critical dimensions, approaching the 20 nm node today, as shown in Fig. 1. Major challenges to downscaling to the sub-10 nm regime will require device innovations in cell storage capacitors, cell array transistors (CATs) and patterning processes.[5]

The minimum cell capacitance must be maintained to provide an adequate signal for sensing and to meet retention time specifications.[6] In order to maintain the cell capacitance, as DRAM downscaled from 90 nm to 20 nm, the capacitor structure has been changed from a simple 3D cylindrical shape to an extremely high aspect ratio (AR) supported cylinder or pillar structure, as shown in Fig. 2. For sub-10 nm DRAMs, structural innovation may not help any longer due to physical limitations in accommodating complex 3D structures. At sub-10 nm nodes, the distance between electrodes becomes ~10 nm or less, which in turn requires the physical thickness of the storage electrodes and the dielectrics to be thinner than 5 nm or less. These requirements will be very difficult to meet. However, the limitation of cell capacitance can be compensated by the technological innovation in CAT with extremely low leakage currents and/or array architecture and its integration process to provide high sensing signals.

From a device point of view, requirements related to the retention limit can be overcome by suppressing the storage node leakage current I_{LEAK}. The data retention time t_{RE} is fundamentally determined by the amount of the stored charge and the time-dependent charge loss at the storage node.[7] The sensing voltage ΔV_{BL} is as follows:

$$\Delta V_{BL} = \frac{C_S}{C_{BL} + C_S}\left(\frac{V_{ARR}}{2} - \Delta V_L\right), \quad (1)$$

where C_S is the cell storage capacitance, V_{ARR} is the array voltage, C_{BL} is the bit

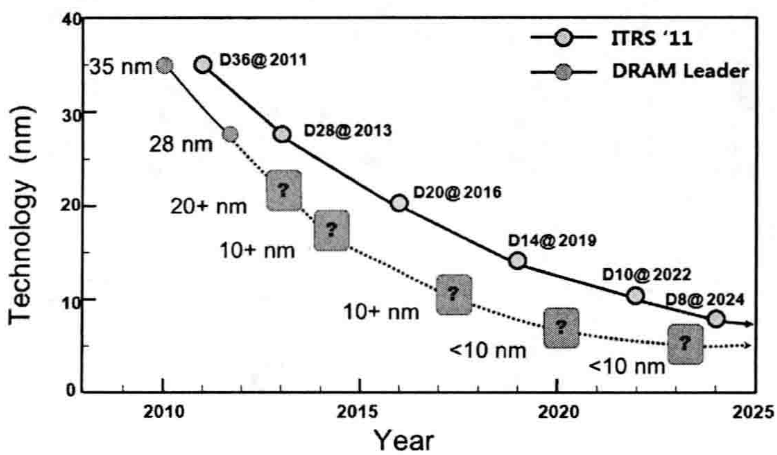

Figure 1. DRAM technology roadmap of ITRS and top DRAM supplier.