PROCEEDINGS OF THE SYMPOSIUM ON

LOW TEMPERATURE ELECTRONICS AND HIGH TEMPERATURE SUPERCONDUCTORS

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DIELECTRICS AND INSULATION DIVISION

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PREFACE

This Proceedings Volume includes papers that were presented at the Symposium on Low Temperature Electronics and High Temperature Superconductivity which was held during October 19-23, 1987 in Honolulu, Hawaii at a joint meeting of The Electrochemical Society and The Electrochemical Society of Japan in cooperation with The Japan Society of Applied Physics. Several papers on the same subject from a parallel Late News Paper session at this meeting are also included. The Symposium and this Proceedings Volume are sponsored by the Dielectrics and Insulation Division of The Electrochemical Society.

The included papers demonstrate that the study and use of low temperature electronics are increasing in many diverse areas, providing valuable benefits for many applications, as well as opportunities for research in materials and devices. Operating electronic devices and systems at low temperatures present many challenges for the designer and user. Although there is active interest in this area, it remains to be seen whether the advantages achieved by cooling electronics will lead to widespread practice.

Two recent developments, both discussed in this volume, have particularly focused attention on the field of low temperature electronics and could impact future applications. First, a supercomputer, the ETA-10, with its high speed VLSI processors populated with CMOS and cooled to 77°K during operation, was delivered to Florida State University and is presently being field-tested as it is brought up to its full operating potential. Secondly, superconductors with critical temperatures, T_c , in excess of 90°K were prepared by Chu et al. following the pioneering work of Mueller and Bednorz at the IBM Zurich Research Laboratory. Superconductivity can now be achieved at the same temperatures and with the same refrigerators used to cool semiconductor electronics. The consequences, from a user's perspective, of refrigerating the high speed processor of a supercomputer, and, secondly, high T_c superconductors and their possible role in electronics, are both discussed in these Proceedings.

The Proceedings, which is organized into six sections, contain 34 invited (designated by * in the Table of Contents) and 28 contributed papers. The first section, "Introduction", contains three invited papers. The first paper by P.M. Solomon considers the application of low temperature electronics for VLSI applications. A second paper by T. Sugano summarizes work from Japan in low temperature electronics. The third paper by D. Duke describes the status of the ETA-10 supercomputer, an important test case for supercomputer operation at low temperatures and considers the consequences, from a user's perspective, of refrigerating the high speed processor of a supercomputer.

Each of the remaining five sections is preceded by a section overview. The second section on "Low Temperature Microelectronics" consists of papers on silicon- based, liquid-nitrogen cooled, complementary MOS technologies for potential digital applications. The third section, "Refrigeration for Low Temperature Electronics", describes the methods of cooling electronics presently available for large and small applications. The fourth section, "Superconductivity and Superconducting Devices", provides a current report on high temperature superconductivity research, possible device applications, and the status of superconducting devices circuits, and processing using lower temperature superconductors. The fifth section, "III-V Compound Semiconductor Devices", describes improvements in heterojunction devices and new devices whose operation is improved at low temperatures. The sixth section, "Analog Characteristics and Applications", includes papers that deal with the properties and applications of a wide variety of semiconductor devices at frequencies from the audible to the visible. Experimental investigations of commercial and custom-made devices, with both discrete and integrated circuits, are represented.

A book on low temperature electronics was not available when this Symposium was initiated and it was our intent to make these Proceedings a useful resource book. Keeping with this aim, it is appropriate to note that one book in this field, Low Temperature Electronics, R.K. Kirschman (Ed.), IEEE Press, N.Y., 1986, and a journal issue, Special Issue on Low Temperature Semiconductor Electronics, IEEE Trans. Electron Dev., ***ED-34*** (January, 1987), were published in the interim. This Proceedings should be a useful, up-to-date supplement that includes topics not covered in these other publications.

Many people have assisted with the Symposium and the Proceedings Volume. We are particularly grateful to F. Bedard (NSA), R. Blaugher (Westinghouse), R. Brandt (ONR), R. Comizzoli (ATT), E. Edelsack (ONR), J. Mauer (IBM), M. Nisenoff (ONR), L. Rothman (IBM), and N. Welker (NSA); for suggestions and advice regarding the Symposium; to E. Edelsack (NRL), F. Gaensslen (IBM), R. Kiehl (IBM), K. Kitazawa (Univ. of Tokyo), T. Masuhara (Hitachi), B. Penswick (Sunpower, Inc.), W. Steyert (APD Cryogenics), G. Walker (Univ.

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S.I. Raider
R.K. Kirschman

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I. INTRODUCTION

OPTIONS FOR HIGH SPEED LOGIC AT 77K

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Abstract

The role of low temperatures in improving the performance of digital logic circuitry has been expounded by several authors in the past. This paper will attempt a re-evaluation of these advantages in the light of recent advances in semiconductor technology and the added promise of the low T_C superconductors. Most of the advantages, on critical analysis, appear to be of limited leverage i.e. they are useful but not essential to the attainment of future high speed systems. The one area of critical leverage is the wires, both on and off chip. To the extent that the 77K environment in increasingly utilized for large, high speed computers, this paper will comment on which logic technology is most appropriate, and whether superconducting logic devices, if available, offer any advantages.

Introduction

Even before the advent of the high T_C superconductors, the 77K environment has been considered by some researchers to be highly suitably for large digital computers. Indeed, ETA (1) has a supercomputer operating in the 77K environment for more than a year. Keyes (2) *et al.* have enumerated many of the advantages of the cryogenic environment and these have been expanded upon by Gaensslen *et al.* (3), Solomon (4), Matisoo (5), Coeure (6), Dennard (7), Dumke (8) and Abe *et al.* (9) among others. Much of the relevant material has been included in a book by R. Kirschman (10), and in ref. (11). For semiconductor devices at 77K the advantages are: 1)faster device operation 2) ease of device scaling 3)reduced power through lower voltage operation, 4) reduced wire resistance (including superconductivity now!) and electromigration, 5) increased thermal conductivity of the substrate. Along with these advantages come unpalatable disadvantages. These are: 1) the refrigeration burden 2)heat removal at the liquid-solid interface 3) thermal cycling, 4) testability, 5)freeze out and trapping of carriers, 6) enhanced hot-electron effects. In the following sections we will re-evaluate some of these factors and determine their relative importance and which logic technology is the most suitabled to the 77K environment. While Si CMOS is the de-facto technology (1), other technologies based on III-V heterojunction devices (12) promise higher performances. Of the III-V materials, the GaAS - (Al,Ga)As materials system is the most mature technologically. Types of Heterojunction transistor are FETs (HFETs), Bipolar Transistors (HBTs) (13) and Hot Electron Transistors (HETs) (14). N-channel HFETs such as the modulation doped FET (MODFET) (15), semiconductor-insulator-semiconductor FET (SISFET) (16-18), and metal-insulator-metal FET (MISFET) (19), have demonstrated a very high performances at 77K. Complementary HFETs (CHFETs) (20) circuits have also been demonstrated. We will review the properties of these devices below. Superconductivity at 77K allows Josephson Junctions and other superconducting devices to be used. Will these prove to be superior to the semiconductor based devices?

A. Faster Logic Devices.

Semiconductor based devices improve in speed as temperature is reduced because mobilities and saturation velocities are higher. Most circuit delays in semiconductor logic are caused by the time to charge and discharge capacitors and are related to the currents and voltages by:

$$\text{delay} = C_{device} + C_w V/I \qquad [1]$$

where C_{device} and C_w are the device and wiring capacitances, respectively. The delay is linked to the transit time τ_t of the charge carriers through the device, where $\tau_t = L/v$, L is the device length and v is the carrier velocity. This is because the current increases with carrier velocity and the capacitance increases with device length. For the FET in the long channel limit, the transit time is inversely proportional to mobility and is given by: $\tau_t = L/(\mu V)$ where L is the channel length of the FET, while in the short channel limit it is inversely proportional to some maximum limiting velocity v_s, ($\tau_t = L/v_s$) determined by the semiconductor properties. Mobility improves as temperature is reduced because of the reduction of phonon scattering (lattice vibrations) with temperature. This is especially dramatic for a GaAs modulation doped layer (see Fig. 1) where impurities have been separated from the carriers by the technique of modulation doping (21). Mobilities of $> 3\times10^6$ cm ^{2}/V-s have recently been reported at low temperatures. Bulk mobilities are given for various semiconductors are given in Table I, after Keyes (2). Mobilities in the channel of a field effect transistor are invariably lower than bulk, being reduced more in Si than in GaAs. Typical values are given in Table II. The high values of mobility obtainable especially in GaAs at low temperatures have a limited significance for short gate length FETs. This is for two reasons. Firstly, in small devices electric fields tend to be high, and the mobility decreases with field. This occurs when the electric field in the device is larger than the critical field as given by the ratio of the limiting velocity to the low field mobility. For FETs the electric field is determined by only a fraction of the supply voltage ($\simeq 1/4$) since conductivity of the FET is important in the low voltage state, and even more so for CMOS, where devices are connected in series. For GaAs FETs with a 1V power supply, the corresponding mobility would be 1×10^4 cm ^{2}/V-s. Secondly, the mobility of an FET decreases when the channel length becomes shorter than the electron mean free path (22). This occurs in 0.5μm devices for mobilities $>$ 150,000cm ^{2}/V-s, which is roughly equal to electron mobilities in GaAs at 77K. Measurements made by the author on 1μm heterojunction FETs at 77K give mobilities of $\simeq 3\times10^4$ cm ^{2}/V-s.

Maximum carrier velocities increase as well as temperature is lowered. The magnitude of the increase is not nearly as great as for mobility and is about 50% for GaAs (23) and 30% for Si (24) in going from 300K to 77K. The improvement of FET speeds will be bracketed by the improvements in mobility vs peak velocity depending on the ratio of voltage to channel length. Velocity overshoot in short channel length FETs has long been predicted (25), and should be more easily seen at low temperatures where electrons may more easily be accelerated by the field since they are not impeded by phonons. The issue of velocity overshoot for very short gate length FETs is still open. Even though both Si and GaAs FETs have been made with channel lengths down to 0.1μm (26,27), no unambiguous demonstration of velocity enhancement has been seen.

A measure for the velocity in the channel of an FET, in the saturated velocity regime, is given by the the ratio of transconductance per unit width to its capacitance per unit gate area. The transconductance per unit width is a useful figure of merit for the switching speed under heavily loaded conditions. Typical values of this ratio for some recently published devices are given in Table III for Si, GaAs and InGaAs channel devices at 300K and 77K.

Improvements in circuit speed will be related to improvements in device speed by eq. 1. Factors of improvement which have been reported are about 2x for silicon CMOS, about 1.5x for heterojunction FETs and about 2.5x for complementary heterojunction FETs. The latter large factor of improvement is due to the large increase in p-channel mobility from 400 to 3200 cm ^{2}/V-s (see Table II). Until recently the fastest semiconductor device was a modulation doped FET (MODFET) (28), operating at 77K with a delay of 5.5ps. This has now been bettered by the 5ps delay of heterojunction bipolar transistors (HBTs) at 300K (29). From this it may be inferred that raw speed cannot