PROCEEDINGS OF SPIE

SPIE—The International Society for Optical Engineering

Smart Structures and Materials 2004

Smart Electronics, MEMS, BioMEMS, and Nanotechnology

Vijay K. Varadan
Chair/Editor

15–18 March 2004
San Diego, California, USA

Sponsored by
SPIE—The International Society for Optical Engineering

Cosponsored by
AIAA—American Institute of Aeronautics and Astronautics (USA)
ASME—American Society of Mechanical Engineers (USA)
SEM—Society for Experimental Mechanics (USA)
The Boeing Company (USA)
Journal of Intelligent Materials Systems and Structures/SAGE Publications (USA)
Rhombus Consultants Group (USA)
CSA Engineering, Inc. (USA)
ISIS-Canada (Canada)

SPIE P PROCEEDINGS SERIES

Volume 5389

PROCEEDINGS OF SPIE
SPIE—The International Society for Optical Engineering

Smart Structures and Materials 2004

Smart Electronics, MEMS, BioMEMS, and Nanotechnology

Vijay K. Varadan
Chair/Editor

15–18 March 2004
San Diego, California, USA

Sponsored and Published by
SPIE—The International Society for Optical Engineering

Cosponsored by
AIAA—American Institute of Aeronautics and Astronautics (USA)
ASME—The American Society of Mechanical Engineers (USA)
SEM—Society for Experimental Mechanics (USA)
The Boeing Company (USA)
Journal of Intelligent Materials Systems and Structures/SAGE Publications (USA)
Rhombus Consultants Group (USA)
CSA Engineering, Inc. (USA)
ISIS-Canada (Canada)

Cooperating Organizations
DARPA—Defense Advanced Research Projects Agency (USA)
Intelligent Materials Forum (Japan)
Jet Propulsion Laboratory (USA)
National Science Foundation (USA)

SPIE P PROCEEDINGS SERIES

Volume 5389

The papers included in this volume were part of the technical conference cited on the cover and title page. Papers were selected and subject to review by the editors and conference program committee. Some conference presentations may not be available for publication. The papers published in these proceedings reflect the work and thoughts of the authors and are published herein as submitted. The publisher is not responsible for the validity of the information or for any outcomes resulting from reliance thereon.

Please use the following format to cite material from this book:

Author(s), "Title of Paper," in *Smart Structures and Materials 2004: Smart Electronics, MEMS, BioMEMS, and Nanotechnology*, edited by Vijay K. Varadan, Proceedings of SPIE Vol. 5389 (SPIE, Bellingham, WA, 2004) page numbers.

ISSN 0277-786X
ISBN 0-8194-5306-4

Published by
SPIE—The International Society for Optical Engineering
P.O. Box 10, Bellingham, Washington 98227-0010 USA
Telephone 1 360/676-3290 (Pacific Time) · Fax 1 360/647-1445
http://www.spie.org

Printed in the United States of America.

Conference Committee

Symposium Chairs

Vasundara V. Varadan, National Science Foundation (USA)
Yoseph Bar-Cohen, Jet Propulsion Laboratory (USA)

Conference Chair

Vijay K. Varadan, The Pennsylvania State University (USA)

Cochairs

Zeynep Celik-Butler, University of Texas/Arlington (USA)
Laszlo B. Kish, Texas A&M University (USA)

Program Committee

Vasu K. Aatre, Defence Research & Development Organisation (India)
Pratul K. Ajmera, Louisiana State University (USA)
Steven W. Arms, MicroStrain, Inc. (USA)
John H. Belk, The Boeing Co. (USA)
Jung-Chih Chiao, University of Texas/Arlington (USA)
Sang H. Choi, NASA Langley Research Center (USA)
Andras Der, Biophysical Research Institute (Hungary)
Claes-Göran Granqvist, Uppsala University (Sweden)
Peter Heszler, Uppsala University (Sweden)
Michael H. Hoffmann, University Ulm (Germany)
Ajay P. Malshe, University of Arkansas (USA)
Kathryn M. McGrath, University of Otago (New Zealand)
Y. Eugene Pak, Samsung Advanced Institute of Technology & CRI (South Korea)
Gabe Schmera, Space and Naval Warfare Center, San Diego (USA)
Andrei M. Shkel, University of California/Irvine (USA)
Ashok Srivastava, Louisiana State University (USA)
Maria Strømme, Uppsala University (Sweden)
Robert Vajtai, Rensselaer Polytechnic Institute (USA)
Lode K. J. Vandamme, Technische Universiteit Eindhoven (Netherlands)

Session Chairs

1 Smart Electronics I
Ashok Srivastava, Louisiana State University (USA)
K. A. Jose, The Pennsylvania State University (USA)

2 Smart Electronics II
Sang H. Choi, NASA Langley Research Center (USA)
Hargsoon Yoon, The Pennsylvania State University (USA)

3 RF MEMS
Sang H. Choi, NASA Langley Research Center (USA)
Vijay K. Varadan, The Pennsylvania State University (USA)

4 Modeling and Simulation of MEMS
Vijay K. Varadan, The Pennsylvania State University

5 Carbon Nanotubes and Applications
Nikhil A. Koratkar, Rensselaer Polytechnic Institute (USA)

6 Functionalized Nanomaterials
Satoshi Kishimoto, National Institute for Materials Science (Japan)

7 Microsensors, Actuators, and MEMS I
Pratul K. Ajmera, Louisiana State University (USA)
K. A. Jose, The Pennsylvania State University (USA)

8 Microsensors, Actuators, and MEMS II
Vijay K. Varadan, The Pennsylvania State University (USA)

9 Biosensors and BioMEMS
Vijay K. Varadan, The Pennsylvania State University (USA)

10 Microsensors, Actuators, and MEMS III
Marina Cole, University of Warwick (United Kingdom)

11 Microsensors, Actuators, and MEMS IV
Tian-Bing Xu, NASA Langley Research Center (USA)

12 Fuel Cells, Power Devices, and Wireless Network
Glen C. King, NASA Langley Research Center (USA)

Contents

Digital CMOS interface circuit for current and capacitance sensing

Ashok Srivastava*

Department of Electrical and Computer Engineering
Louisiana State University Baton Rouge, LA USA 70803-5901

ABSTRACT

A CMOS digital interface chip has been designed and implemented in standard 1.5 μm n-well CMOS technology for detection of current and capacitance variations across a sensing element. An on-chip digitally variable sensor element simulating current and capacitance is monolithically integrated with the readout circuitry. The chip gives an 8-bit digital output and can detect a minimum current and capacitance up to 150 μA and 2.5 fF, respectively.

Keywords: CMOS interface circuit, digital CMOS readout, ADC, DAC, sensors, CMOS mixed-signal circuit

1. INTRODUCTION

Current (I), voltage (V), capacitance (C) and charge (Q) are the essential sensing parameters which are required to be detected with increased sensitivity across a sensor which outputs one of these parameters. On chip integration of both the sensor element and the readout electronics on a common substrate such as silicon has allowed detecting weak signals in noisy and harsh environments and reduces system size. At present most of the sensors are made in MEMS process and readout electronics is in CMOS. Integration of MEMS and CMOS electronics on a common substrate has lead to the development of smart sensors[1-3] for chemical, biological and physical detection. The sensor output is an analog signal and processing analog signal for digital readout provides convenience in data processing, storage and instrumentation.

In the past, we have integrated gas sensors with CMOS devices for sensing hydrocarbon-based gases[4-6], reported design of a CMOS readout circuit for integration with capacitive sensors[7], and an ultra low-power operational amplifier CMOS chip for monolithic integration with neural microprobes[8]. We have also reported a CMOS circuit design for a novel scheme of converting a multiple-valued output voltage from a sensor into a binary-coded output for signal processing [9]. In the present work, we describe design and implementation of an 8-bit digital CMOS readout chip for detecting current and capacitance variations from sensors. Digital readout is designed in standard 1.5 μm n-well CMOS technology using the successive approximation method[10] and consists of an 8-bit shift register, SR module, 8-bit DAC and a comparator. To simulate experimental conditions of the sensor output, we have designed digitally programmable on-chip variable current and capacitor network and integrated with the readout circuit. In the following, we describe the design and experimental results for on-chip simulated sensing.

2. DIGITAL CMOS READOUT CHIP DESIGN

Figure 1 shows the block diagram of a current and capacitance sensing digital readout circuit. The circuit of Fig. 1 utilizes an on-chip digitally programmable variable current and capacitance. The signal is detected by the corresponding sensor circuit, which is selected by the sensor selection control circuit. Digital readout is obtained after analog-to-digital conversion.

*ashok@ece.lsu.edu; phone 1 225 578-5622; fax 1 225 578-5200

Smart Structures and Materials 2004: Smart Electronics, MEMS, BioMEMS, and Nanotechnology, edited by Vijay K. Varadan,
Proceedings of SPIE Vol. 5389 (SPIE, Bellingham, WA, 2004) · 0277-786X/04/$15 · doi: 10.1117/12.540114

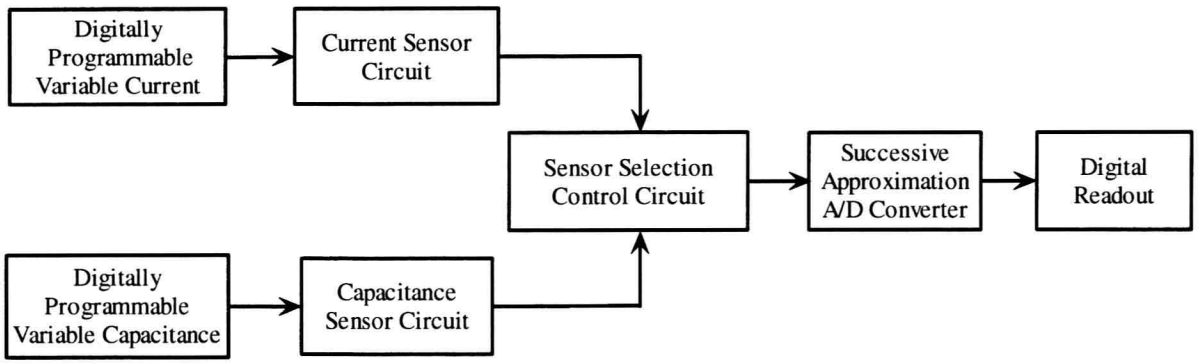


Figure 1: Block diagram of a current and capacitance sensing digital readout electronics.

2.1 Current sensing using digitally programmable variable current

Current sensing part of the digital readout of Fig. 1 is divided in two parts: current sensor circuit, which is basically an amplifier and digitally programmable current circuit for an on-chip simulated variable current. Figure 2 shows the amplifier circuit designed for current detection. In the circuit of Fig. 2, R_Sense is the sense resistor connected in series to the ground path. I_Sense is the sense current to be measured. V_n and V_p characterize the inverting and non-inverting inputs to the amplifier, respectively. Sense current (I_Sense) flows to the ground through the sense resistor, R_Sense and develops a voltage V_p proportional to the varying sense current. The amplifier output voltage (V_{out}) is proportional to the I_Sense.

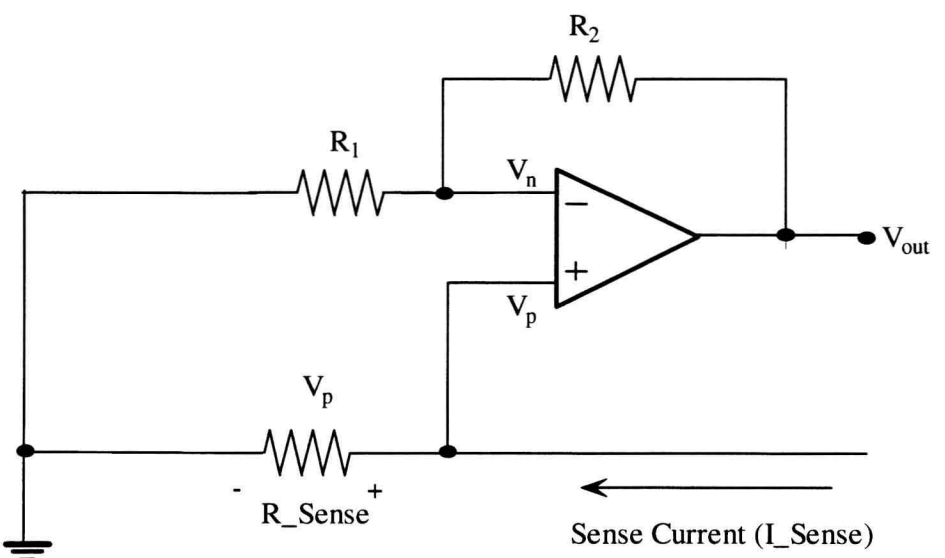


Figure 2: An amplifier circuit for current detection.

The circuit of Fig. 2 is designed to measure current as low as 150 μA of I_Sense (min) with R_Sense of nearly 17 kΩ. The method of current detection of Fig. 2 can also be used for voltage sensing and corresponding digital readout.

2.2 Digitally programmable variable current

On-chip digitally programmable variable current is achieved using a binary weighted unit MOSFET array as shown in Fig. 3. The unit MOSFET is designed for a W/L ratio of 1. The supply voltages, V_{DD} and V_{SS} are 3V and 0V, respectively. The drain current from a unit size transistor is 150 μA. Control signals applied to the gates in the

MOSFET array are obtained from a 4-bit binary synchronous counter as shown in Fig. 4. The counter switches the gates of appropriate MOSFETs in the MOSFET array to the reference voltage, V_{REF} by a 2 to 1 CMOS transmission gate multiplexer. The reference voltage, V_{REF} is 3V. MOSFET array along with the base unit MOSFET is capable of producing 2^4 (16) different equally incremented currents, which form the on-chip simulated sense current, I_Sense of the current sensor circuit.

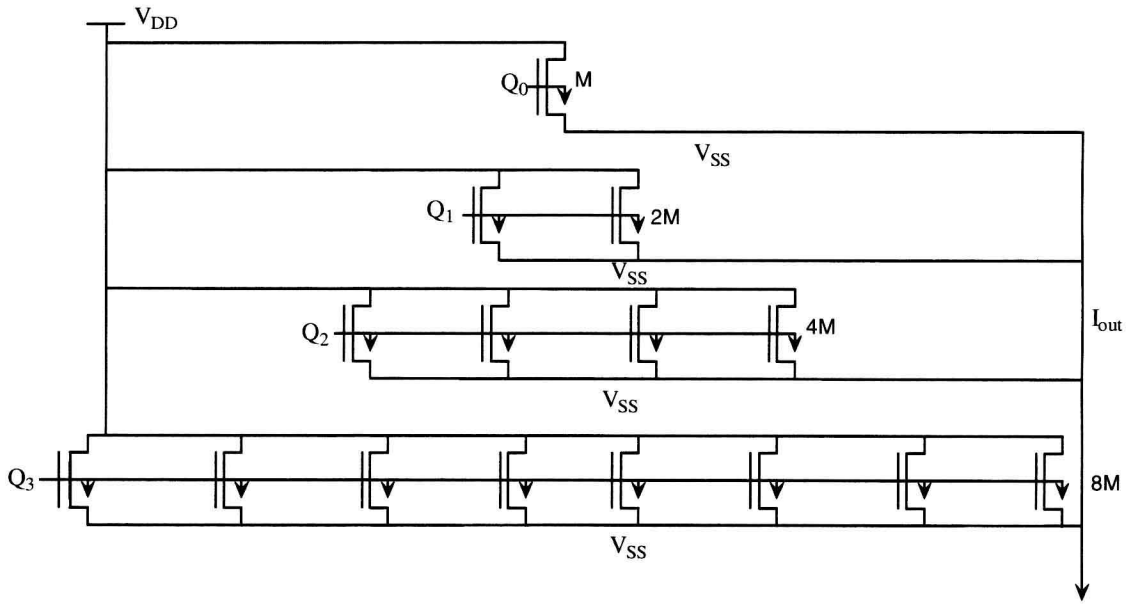


Figure 3: A binary weighted unit MOSFET array. Note: Q_0 - Q_3: LSB to MSB outputs of a 4 - bit synchronous binary counter, M: Unit MOSFET (W/L = 1).

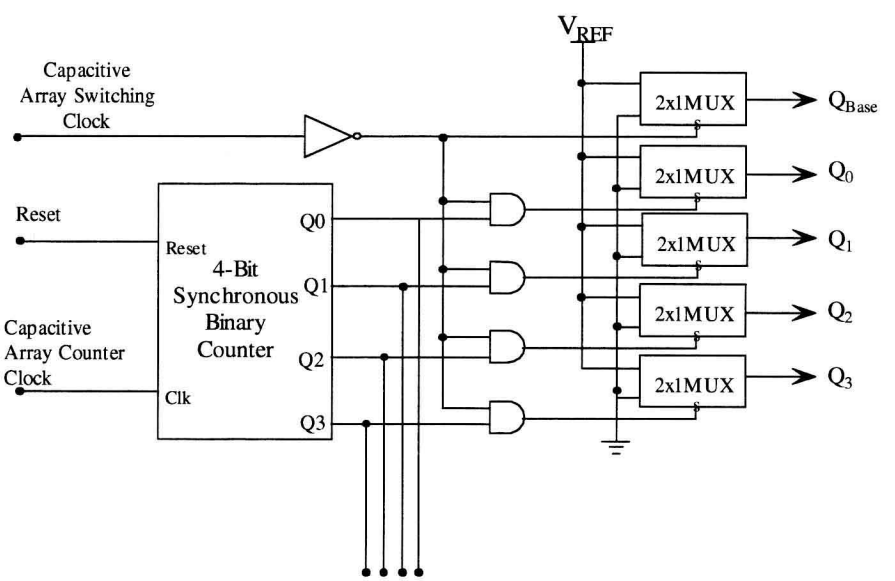


Figure 4: Block diagram of a MOSFET array controlled by a 4-bit synchronous binary counter.

2.3 Capacitance sensing using digitally programmable variable capacitance

The design of the circuit is divided in two parts: the analog part associated with the capacitive sensing and the digitally programmable on-chip capacitance. Figure 5 shows a typical block diagram of an analog circuit to measure the sensor capacitance C_S. In Fig. 5, C_R and C_C are the reference capacitor and the coupling capacitor, respectively[11]. C_R and C_S are charged to reference voltage, V_{REF} using complementary clock pulses, phi1 and phi2, respectively. The difference between the charges in C_R and C_S is applied to the inverting input of the amplifier, which produces an amplified output, V_{out}. The analog part of the sensing circuit is designed to operate from a voltage source of 3V.

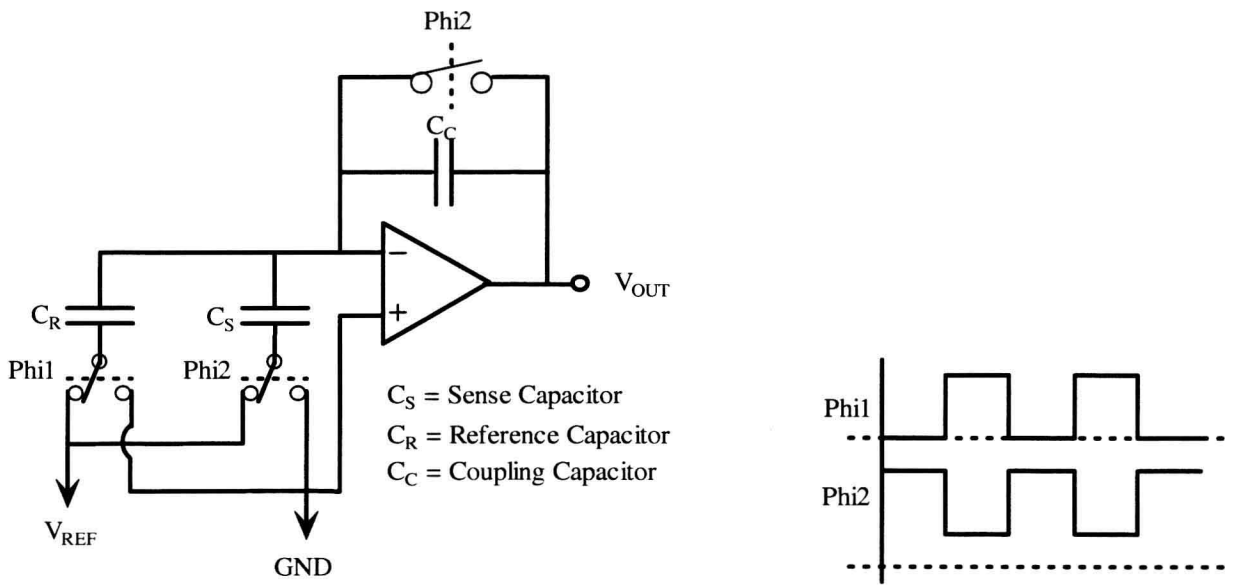


Figure 5: Analog circuit for capacitance sensing.

2.4 Digitally programmable variable capacitance

The sensing signal to the differential amplifier in Fig. 5 is produced by an array of sensing capacitors. A simple technique of putting an array of sense capacitors on the chip was realized by using a 4-bit synchronous binary counter[7]. Figure 6 shows the block diagram a capacitor array. In order to obtain 2^4 (16) distinct capacitive values, a base capacitance (C_S_Base) and four binary weighted capacitors (1C, 2C, 4C and 8C) are needed where C= C_Resolution. Thus, for instance, in a 2.5 fF resolution, 1C = 2.5 fF is as shown in Fig. 6. A 4-bit synchronous binary counter is needed to select the appropriate weighted capacitor in parallel with the base capacitor, which is switched to the V_{REF} by a 2 to 1 CMOS transmission gate multiplexer as shown in Fig. 7. The binary counter output is synchronized by the clock pulse phi2 through AND gates so that any switching will occur only when C_R is switched so that it is connected to ground. The counter can be initialized to 0000 at any time in order have only the C_S_Base switched. The reset input is active low and is pulled up by an active load in order to be functional even if that chip pin is floating. The speed of the capacitive change can be adjusted with the capacitive sensor array counter clock. It will be convenient to adjust it to a slow clock when taking measurement.

The capacitors were designed using poly-1 and poly-2 levels of the standard 1.5 μm n-well CMOS process. Approximately 160 μm^2 capacitor areas yielded a 40 fF capacitor value. A base capacitor of 40 fF was used in all three cases. The C_C and C_R for the 2.5 fF resolutions were chosen to be 50fF and 75fF, respectively. These latter values were determined by trial and error so that the measurable output voltage level could be attained. Three 25 fF capacitors were connected in parallel to realize C_R and a special capacitor of 50 fF was designed for C_C as shown in Fig. 8

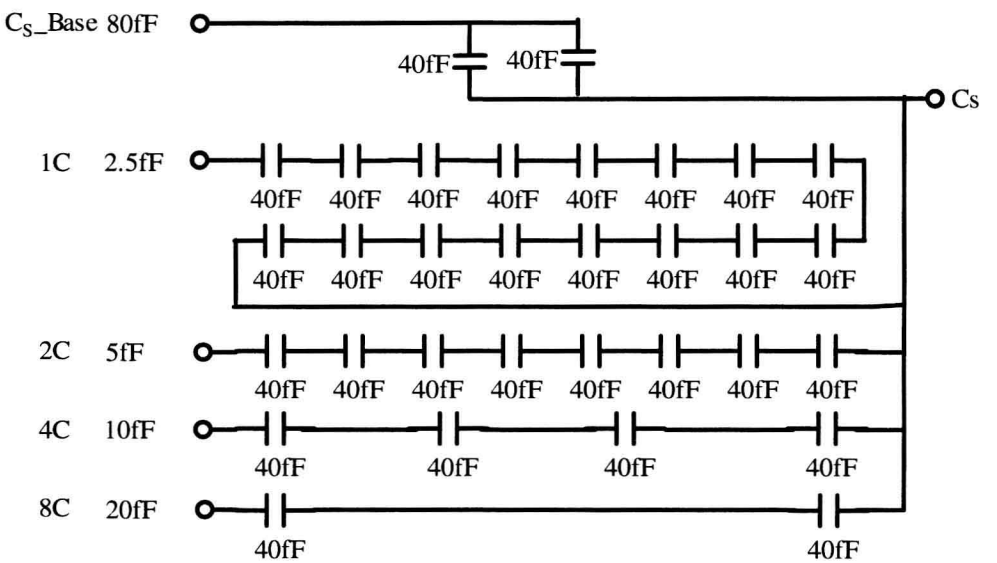


Figure 6: Design of a sense capacitor array for a 2.5fF resolution.

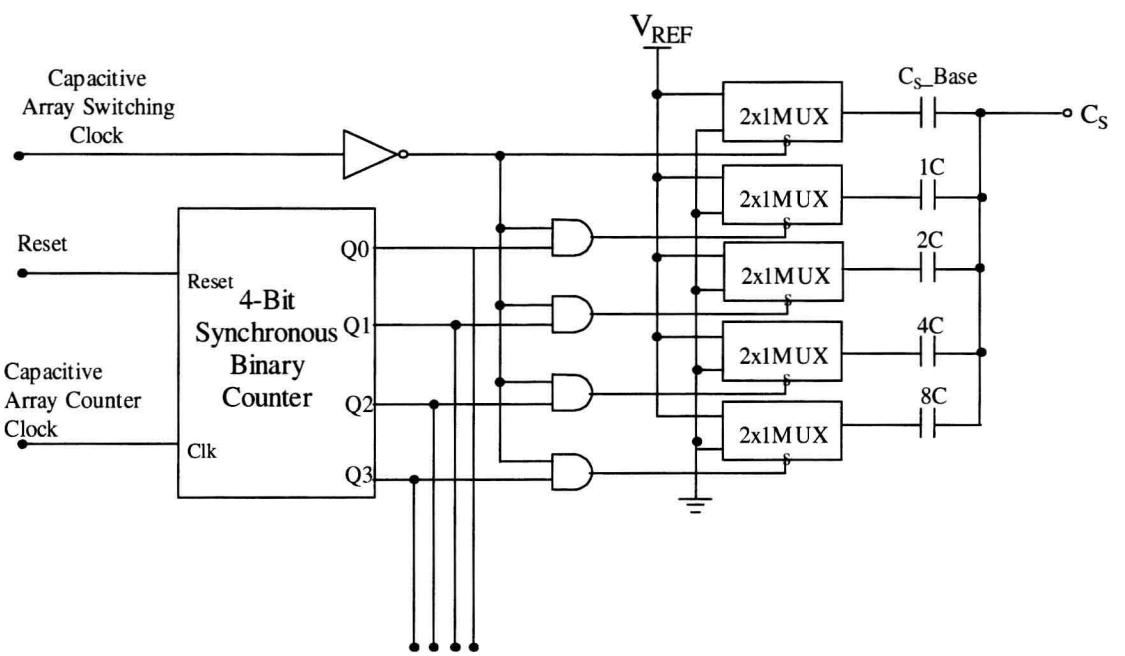


Figure 7: Block diagram of an on-chip simulated variable capacitor array controlled by a 4-bit synchronous binary counter.

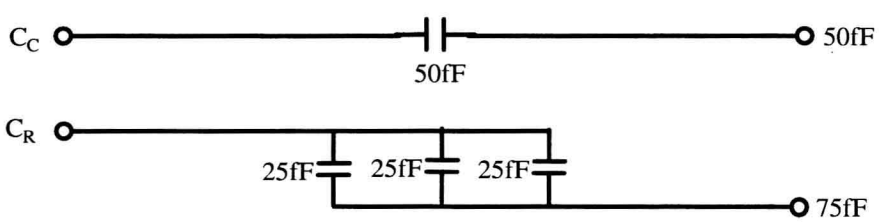


Figure 8: Design of reference and coupling capacitors.

2.5 Sensor selection control circuit (SSCL)

Analog output from the sensor circuit is fed to an analog-to-digital converter (ADC) through a sensor selection control (SSCL) circuit. The SSCL circuit is implemented using a CMOS transmission gate multiplexer and is controlled by an external input *Select*. The SSCL circuit chooses between sensors based on input *Select* and connects the output of sensor to an ADC for the digital output. *Select-High* emulates the current sensor. *Select-Low* emulates the capacitance sensor.

2.6 Readout circuit design

Digital readout is achieved with an ADC designed using a successive approximation technique as shown in Fig. 9. The circuit of ADC operates as follows. The start pulse sets a "1" in F/F1, and additionally drives F/F9 to the "1" state. Then the MSB analog switch is driven by F/F9 to connect the reference voltage, V_{REF} to the terminal of the capacitor array of digital-to-analog converter (DAC). The output of the DAC (V_{OA}), which is equivalent to the weighted MSB, is then compared with the input analog voltage (V_{IA}) by the comparator. After some delay time, the comparator output appears at the output of AND gate G1. The comparator generates a logic "1" output if the DAC output (V_{OA}) is greater than V_{IA} or a logic "0" if the reverse is true. When the positive half cycle of clock signal occurs, gate G1 changes to the "1" state if the comparator output is HIGH or to the "0" state if the comparator output is LOW. G2 is already in the "1" state and changes to either "1" or "0" accordingly. At the end of the positive half-cycle clock signal, gates G1 and G2 return to the "0" state. Transition from "1" to "0" at the gate G2 resets the F/F9 to the "0" state thereby driving the analog switch (AS1) to remove the reference voltage and connect ground to the MSB terminal of the DAC capacitor array. F/F9 remains in "1" state if there is no transition from "1" to "0" at the gate G2 at the end of positive half cycle. Next clock pulse shifts "1" in F/F1 to F/F2, thereby enabling AND gate G3 also F/F1's transition from "1" to "0" sets logic "1" in F/F10 and the weighing process of successive approximation logic repeats. This process is repeated until each bit is tried. After the LSB has been tried the digital word in the flip-flops (F/F9, F/F10, ... ,F/F16) is equivalent to V_{IA} with a precision of ±1/2 in 255. All 8-bits of the ADC are tried and settled after eight clock pulses.

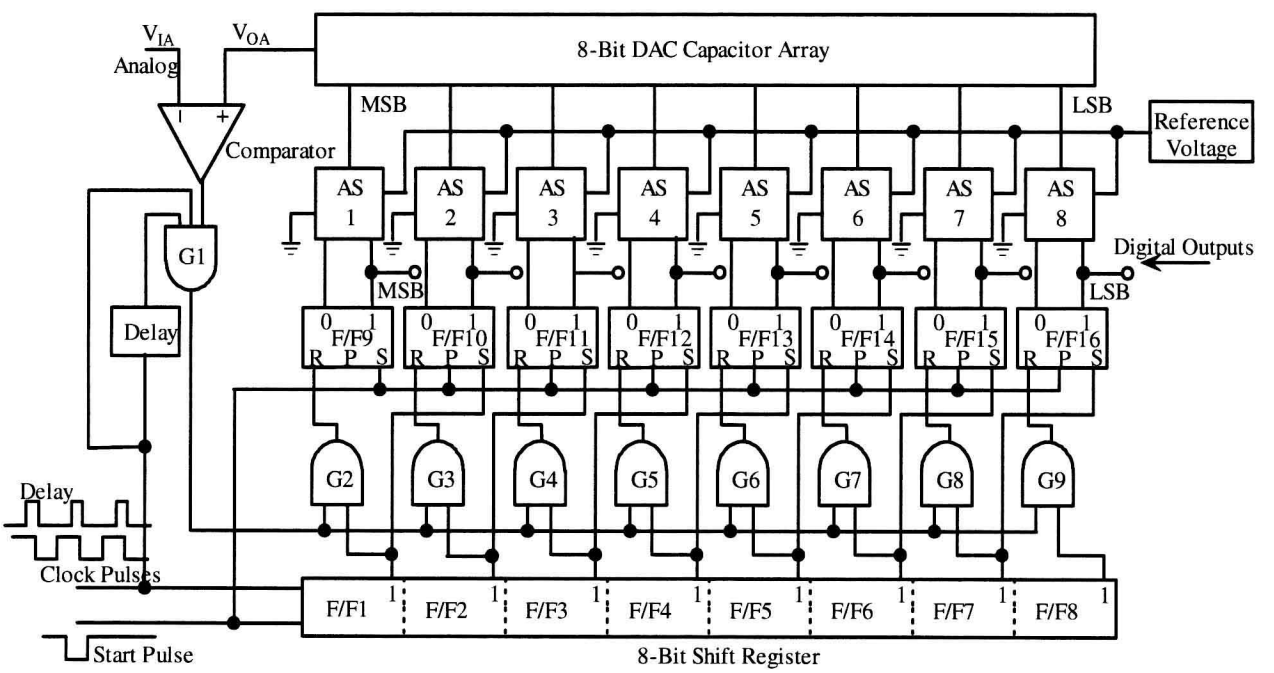


Figure 9: Digital readout using a successive approximation ADC technique.

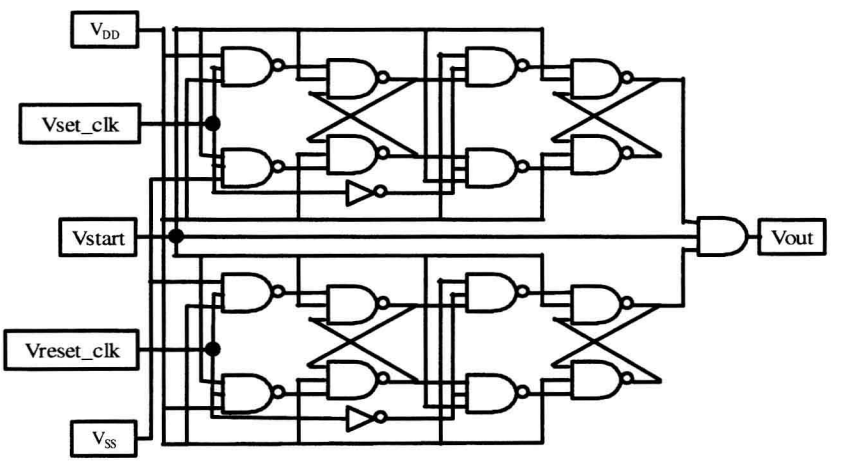
Digital readout circuit design of Fig. 9 is divided in four main blocks: 8-bit shift register, SR module, 8-bit DAC and comparator. In the following, design and function of individual modules are described with the help of associated control circuitry.

2.6.1 Eight-bit shift register design

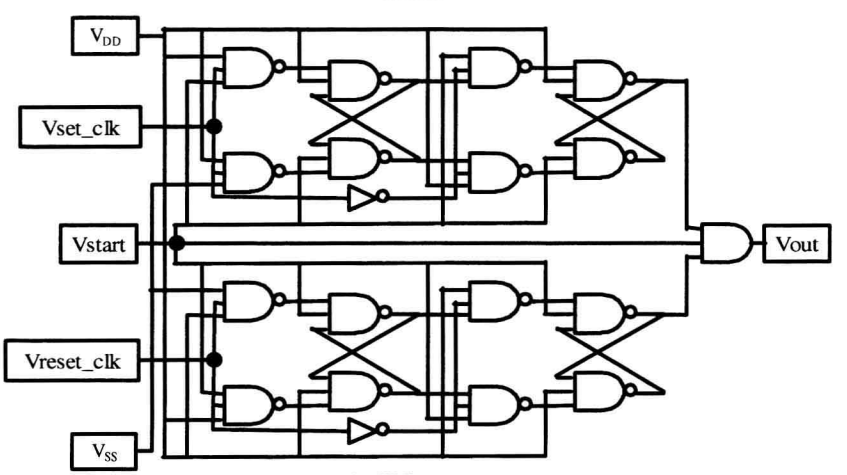
The 8-bit shift register is designed using negative edge-triggered D flip-flops. Flip-flops are connected in a ring fashion such that the output of one flip-flop drives the next flip-flop. Start pulse sets a "1" in F/F1 and also drives F/F2, F/F3,…,F/F8 to "0" state. This gives 10000000 outputs from the shift register. Negative edge of clock pulse shifts flip-flop state "1" by one position towards the LSB. After the first clock pulse output of shift register will be 01000000. This will be repeated as long as the clock is available and the logic "1" keeps shifting by one position at the negative edge of the clock. Shift register can be reset anytime with the start pulse.

2.6.2 SR module design

SR module, which is primarily responsible for implementing the successive approximation logic of ADC is designed using a simple technique of coupling two synchronous SR flip-flops. Circuits describing coupling of SR flip-flops are shown in Fig. 10. SR module is implemented using two types of coupled flip-flops SR1 and SR2. In Fig. 10, F/F9 is implemented using SR1 and remaining flip-flops in the SR module F/F10, F/F11, … ,F/F16 are implemented with SR2. SR1 and SR2 both have three inputs: Start (Vstart), Set_clock (Vset_clk) and Reset_clock (Vreset_clk). Start (Vstart) pulse sets "1" in SR1 and resets SR2 i.e. sets "0". After the start pulse is given, SR module in Fig. 10 will have output 10000000. Clock (Vreset_clk) is generated at the output of gate G1, this either resets the coupled flip-flops in SR module to "0" or leaves "1" in place based on the comparator's output. Set_clock (Vset_clk), generated by negative going output of shift register flip-flop, enables the AND gate to set coupled flip-flop of SR module to "1" state.



a: SR1



b: SR2

Figure 10: Coupling of SR flip-flops to implement the successive approximation logic of ADC.