

国外电子与通信教材系列

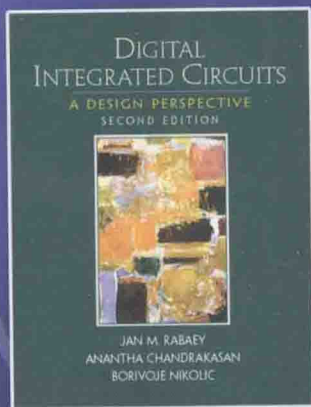
英文版

PEARSON

数字集成电路

——电路、系统与设计

(第二版)



Digital Integrated Circuits
A Design Perspective, Second Edition

Jan M. Rabaey

[美] Anantha Chandrakasan 著

Borivoje Nikolić



电子工业出版社

PUBLISHING HOUSE OF ELECTRONICS INDUSTRY

<http://www.phei.com.cn>

国外电子与通信教材系列

数字集成电路

——电路、系统与amp;设计

(第二版)(英文版)

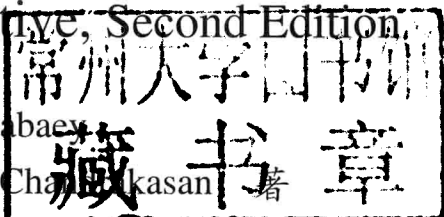
Digital Integrated Circuits

A Design Perspective, Second Edition

Jan M. Rabaey

[美] Anantha Chakrabandhan kasan 著

Borivoje Nikolic



电子工业出版社

Publishing House of Electronics Industry

北京·BEIJING

内 容 简 介

本书分三部分：基本单元、电路设计和系统设计。在对 MOS 器件和连线的特性做了简要介绍之后，深入分析了反相器，并逐步将这些知识延伸到组合逻辑电路、时序逻辑电路、控制器、运算电路及存储器这些复杂数字电路与系统的设计中。本书以 0.25 微米 CMOS 工艺的实际电路为例，讨论了深亚微米器件效应、电路最优化、互连线建模和优化、信号完整性、时序分析、时钟分配、高性能和低功耗设计、设计验证、芯片测试和可测性设计等主题，着重探讨了深亚微米数字集成电路设计面临的挑战和启示。本书内容已根据作者和中文版译者整理的勘误表进行了更正。

本书可作为高等院校电子科学与技术、电子与信息工程、计算机科学与技术等专业高年级本科生和研究生有关数字集成电路设计方面课程的双语教学教材，也可作为从事这一领域的工程技术人员的参考书。

Original edition, entitled Digital Integrated Circuits: A Design Perspective, Second Edition, 9780130909961 by Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolić, published by Pearson Education, Inc., publishing as Prentice Hall, Copyright © 2003 Pearson Education, Inc.

All rights reserved. No part of this book may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying, recording or by any information storage retrieval system, without permission from Pearson Education, Inc.

China edition published by PEARSON EDUCATION ASIA LTD., and PUBLISHING HOUSE OF ELECTRONICS INDUSTRY copyright © 2012. This edition is manufactured in the People's Republic of China, and is authorized for sale and distribution in the mainland of China exclusively(except Taiwan, Hong Kong SAR and Macau SAR).

本书英文影印版专有出版权由 Pearson Education（培生教育出版集团）授予电子工业出版社。未经出版者预先书面许可，不得以任何方式复制或抄袭本书的任何部分。本书在中国大陆地区出版，仅限在中国大陆发行。本书贴有 Pearson Education（培生教育出版集团）激光防伪标签，无标签者不得销售。

版权贸易合同登记号 图字：01-2012-0838

图书在版编目（CIP）数据

数字集成电路：电路、系统与amp;设计：第 2 版 = Digital Integrated Circuits:A Design Perspective; 英文 / (美) 拉贝艾 (Rabaey, J. M.), (美) 钱德卡桑 (Chandrakasan, A.), (美) 尼克里克 (Nikolić, B.) 著.

北京：电子工业出版社，2012.3

国外电子与通信教材系列

ISBN 978-7-121-15889-6

I. ①数… II. ①拉… ②钱… ③尼… III. ①数字集成电路 - 高等学校 - 教材 - 英文 IV. ①TN431.2

中国版本图书馆 CIP 数据核字（2012）第 025026 号

策划编辑：马 岚

责任编辑：马 岚

印 刷：三河市双峰印刷装订有限公司

装 订：电子工业出版社

北京市海淀区万寿路 173 信箱 邮编：100036

开 本：787 × 980 1/16 印张：49 字数：1427 千字

印 次：2012 年 3 月第 1 次印刷

定 价：89.00 元

凡所购买电子工业出版社的图书有缺损问题，请向购买书店调换；若书店售缺，请与本社发行部联系。联系及邮购电话：（010）88254888。

质量投诉请发邮件至 zlt@s@phei.com.cn，盗版侵权举报请发邮件至 dbqq@s@phei.com.cn。

服务热线：（010）88258888。

序

2001年7月间,电子工业出版社的领导同志邀请各高校十几位通信领域方面的老师,商量引进国外教材问题。与会同志对出版社提出的计划十分赞同,大家认为,这对我国通信事业、特别是对高等院校通信学科的教学工作会很有好处。

教材建设是高校教学建设的主要内容之一。编写、出版一本好的教材,意味着开设了一门好的课程,甚至可能预示着一个崭新学科的诞生。20世纪40年代MIT林肯实验室出版的一套28本雷达丛书,对近代电子学科、特别是对雷达技术的推动作用,就是一个很好的例子。


我国领导部门对教材建设一直非常重视。20世纪80年代,在原教委教材编审委员会的领导下,汇集了高等院校几百位富有教学经验的专家,编写、出版了一大批教材;很多院校还根据学校的特点和需要,陆续编写了大量的讲义和参考书。这些教材对高校的教学工作发挥了极好的作用。近年来,随着教学改革不断深入和科学技术的飞速进步,有的教材内容已比较陈旧、落后,难以适应教学的要求,特别是在电子学和通信技术发展神速、可以讲是日新月异的今天,如何适应这种情况,更是一个必须认真考虑的问题。解决这个问题,除了依靠高校的老师 and 专家撰写新的符合要求的教科书外,引进和出版一些国外优秀电子与通信教材,尤其是有选择地引进一批英文原版教材,是会有好处的。

一年多来,电子工业出版社为此做了很多工作。他们成立了一个“国外电子与通信教材系列”项目组,选派了富有经验的业务骨干负责有关工作,收集了230余种通信教材和参考书的详细资料,调来了100余种原版教材样书,依靠由20余位专家组成的出版委员会,从中精选了40多种,内容丰富,覆盖了电路理论与应用、信号与系统、数字信号处理、微电子、通信系统、电磁场与微波等方面,既可作为通信专业本科生和研究生的教学用书,也可作为有关专业人员的参考材料。此外,这批教材,有的翻译为中文,还有部分教材直接影印出版,以供教师用英语直接授课。希望这些教材的引进和出版对高校通信教学和教材改革能起一定作用。

在这里,我还要感谢参加工作的各位教授、专家、老师与参加翻译、编辑和出版的同志们。各位专家认真负责、严谨细致、不辞辛劳、不怕琐碎和精益求精的态度,充分体现了中国教育工作者和出版工作者的良好美德。

随着我国经济建设的发展和科学技术的不断进步,对高校教学工作会不断提出新的要求和希望。我想,无论如何,要做好引进国外教材的工作,一定要联系我国的实际。教材和学术专著不同,既要注意科学性、学术性,也要重视可读性,要深入浅出,便于读者自学;引进的教材要适应高校教学改革的需要,针对目前一些教材内容较为陈旧的问题,有目的地引进一些先进的和正在发展中的交叉学科的参考书;要与国内出版的教材相配套,安排好出版英文原版教材和翻译教材的比例。我们努力使这套教材能尽量满足上述要求,希望它们能放在学生们的课桌上,发挥一定的作用。

最后,预祝“国外电子与通信教材系列”项目取得成功,为我国电子与通信教学和通信产业的发展培土施肥。也恳切希望读者能对这些书籍的不足之处、特别是翻译中存在的问题,提出意见和建议,以便再版时更正。



中国工程院院士、清华大学教授
“国外电子与通信教材系列”出版委员会主任

出版说明

进入21世纪以来,我国信息产业在生产和科研方面都大大加快了发展速度,并已成为国民经济发展的支柱产业之一。但是,与世界上其他信息产业发达的国家相比,我国在技术开发、教育培训等方面都还存在着较大的差距。特别是在加入WTO后的今天,我国信息产业面临着国外竞争对手的严峻挑战。

作为我国信息产业的专业科技出版社,我们始终关注着全球电子信息技术的发展方向,始终把引进国外优秀电子与通信信息技术教材和专业书籍放在我们工作的重要位置上。在2000年至2001年间,我社先后从世界著名出版公司引进出版了40余种教材,形成了一套“国外计算机科学教材系列”,在全国高校以及科研部门中受到了欢迎和好评,得到了计算机领域的广大教师与科研工作者的充分肯定。

引进和出版一些国外优秀电子与通信教材,尤其是有选择地引进一批英文原版教材,将有助于我国信息产业培养具有国际竞争能力的技术人才,也将有助于我国国内在电子与通信教学工作中掌握和跟踪国际发展水平。根据国内信息产业的现状、教育部《关于“十五”期间普通高等教育教材建设与改革的意见》的指示精神以及高等院校老师们反映的各种意见,我们决定引进“国外电子与通信教材系列”,并随后开展了大量准备工作。此次引进的国外电子与通信教材均来自国际著名出版商,其中影印教材约占一半。教材内容涉及的学科方向包括电路理论与应用、信号与系统、数字信号处理、微电子、通信系统、电磁场与微波等,其中既有本科专业课程教材,也有研究生课程教材,以适应不同院系、不同专业、不同层次的师生对教材的需求,广大师生可自由选择 and 自由组合使用。我们还将与国外出版商一起,陆续推出一些教材的教学支持资料,为授课教师提供帮助。

此外,“国外电子与通信教材系列”的引进和出版工作得到了教育部高等教育司的大力支持和帮助,其中的部分引进教材已通过“教育部高等学校电子信息科学与工程类专业教学指导委员会”的审核,并得到教育部高等教育司的批准,纳入了“教育部高等教育司推荐——国外优秀信息科学与技术系列教学用书”。

为做好该系列教材的翻译工作,我们聘请了清华大学、北京大学、北京邮电大学、南京邮电大学、东南大学、西安交通大学、天津大学、西安电子科技大学、电子科技大学、中山大学、哈尔滨工业大学、西南交通大学等著名高校的教授和骨干教师参与教材的翻译和审校工作。许多教授在国内电子与通信专业领域享有较高的声望,具有丰富的教学经验,他们的渊博学识从根本上保证了教材的翻译质量和专业学术方面的严格与准确。我们在此对他们的辛勤工作与贡献表示衷心的感谢。此外,对于编辑的选择,我们达到了专业对口;对于从英文原书中发现的错误,我们通过作者联络、从网上下载勘误表等方式,逐一进行了修订;同时,我们对审校、排版、印制质量进行了严格把关。

今后,我们将进一步加强同各高校教师的密切关系,努力引进更多的国外优秀教材和教学参考书,为我国电子与通信教材达到世界先进水平而努力。由于我们对国内外电子与通信教育的发展仍存在一些认识上的不足,在选题、翻译、出版等方面的工作中还有许多需要改进的地方,恳请广大师生和读者提出批评及建议。

电子工业出版社

教材出版委员会

| | | |
|-----|------------|---|
| 主任 | 吴佑寿 | 中国工程院院士、清华大学教授 |
| 副主任 | 林金桐 杨千里 | 北京邮电大学校长、教授、博士生导师 总参通信部副部长，中国电子学会会士、副理事长 中国通信学会常务理事、博士生导师 |
| 委员 | 林孝康 | 清华大学教授、博士生导师、电子工程系副主任、通信与微波研究所所长 教育部电子信息科学与工程类专业教学指导分委员会委员 |
| | 徐安士 | 北京大学教授、博士生导师、电子学系主任 |
| | 樊昌信 | 西安电子科技大学教授、博士生导师 中国通信学会理事、IEEE 会士 |
| | 程时昕 | 东南大学教授、博士生导师 |
| | 郁道银 | 天津大学副校长、教授、博士生导师 教育部电子信息科学与工程类专业教学指导分委员会委员 |
| | 阮秋琦 | 北京交通大学教授、博士生导师 计算机与信息技术学院院长、信息科学研究所所长 国务院学位委员会学科评议组成员 |
| | 张晓林 | 北京航空航天大学教授、博士生导师、电子信息工程学院院长 教育部电子信息科学与电气信息类基础课程教学指导分委员会副主任委员 中国电子学会常务理事 |
| | 郑宝玉 | 南京邮电大学副校长、教授、博士生导师 教育部电子信息与电气学科教学指导委员会委员 |
| | 朱世华 | 西安交通大学副校长、教授、博士生导师 教育部电子信息科学与工程类专业教学指导分委员会副主任委员 |
| | 彭启琮 | 电子科技大学教授、博士生导师、通信与信息工程学院院长 教育部电子信息科学与电气信息类基础课程教学指导分委员会委员 |
| | 毛军发 | 上海交通大学教授、博士生导师、电子信息与电气工程学院副院长 教育部电子信息与电气学科教学指导委员会委员 |
| | 赵尔沅 钟允若 | 北京邮电大学教授、《中国邮电高校学报（英文版）》编委会主任 原邮电科学研究院副院长、总工程师 |
| | 刘彩 | 中国通信学会副理事长兼秘书长，教授级高工 信息产业部通信科技委副主任 |
| | 杜振民 | 电子工业出版社原副社长 |
| | 王志功 | 东南大学教授、博士生导师、射频与光电集成电路研究所所长 教育部高等学校电子电气基础课程教学指导分委员会主任委员 |
| | 张中兆 | 哈尔滨工业大学教授、博士生导师、电子与信息技术研究院院长 |
| | 范平志 | 西南交通大学教授、博士生导师、信息科学与技术学院院长 |

Preface^①

What is New?

Welcome to second edition of “*Digital Integrated Circuits: A Design Perspective.*” In the six years since the publication of the first, the field of digital integrated circuits has gone through some dramatic evolutions and changes. IC manufacturing technology has continued to scale to ever-smaller dimensions. Minimum feature sizes have scaled by a factor of almost ten since the writing of the first edition, and now are approaching the 100 nm realm. This scaling has a double impact on the design of digital integrated circuit. First of all, the complexity of the designs that can be put on a single die has increased dramatically. Dealing with the challenges this poses has led to new design methodologies and implementation strategies. At the same time, the plunge into the deep-submicron space causes devices to behave differently, and brings to the forefront a number of new issues that impact the reliability, cost, performance, and power dissipation of the digital IC. Addressing these issues in-depth is what differentiates this edition from the first.

A glance through the table of contents reveals extended coverage of issues such as deep-sub micron devices, circuit optimization, interconnect modeling and optimization, signal integrity, clocking and timing, and power dissipation. All these topics are illustrated with state-of-the-art design examples. Also, since MOS now represents more than 99% of the digital IC market, older technologies such as silicon bipolar and GaAs have been deleted (however, the interested reader can find the old chapters on these technologies on the web site of the book). Given the importance of methodology in today’s design process, we have included *Design Methodology Inserts* throughout the text, each of which highlights one particular aspect of the design process. This new edition represents a major reworking of the book. The biggest change is the addition of two co-authors, Anantha and Bora, who have brought a broader insight into digital IC design and its latest trends and challenges.

Maintaining the Spirit of the First Edition

While introducing these changes, our intent has been to preserve the spirit and goals of the first edition—that is, to bridge the gap between the **circuit and system visions** on digital design. While starting from a solid understanding of the operation of electronic devices and an in-depth analysis of the nucleus of digital design—the inverter—we gradually channel this knowledge into the design of more complex modules such as gates, registers, controllers, adders, multipliers, and memories. We identify the compelling questions facing the designers of today’s

① 登录华信教育资源网 (www.hxedu.com.cn) 可下载本书的彩色插图文件 (4 页)。

complex circuits: What are the dominant design parameters, what section of the design should he focus on and what details could she ignore? Simplification is clearly the only approach to address the increasing complexity of the digital systems. However, oversimplification can lead to circuit failure since global circuit effects such as timing, interconnect, and power consumption are ignored. To avoid this pitfall it is important to design digital circuits with both a circuits and a systems perspective in mind. This is the approach taken in this book, which brings the reader the knowledge and expertise needed to deal with complexity, using both analytical and experimental techniques.

How to Use This Book

The core of the text is intended for use in a *senior-level digital circuit design class*. Around this kernel, we have included chapters and sections covering the more advanced topics. In the course of developing this book, it quickly became obvious that it is difficult to define a subset of the digital circuit design domain that covers everyone's needs. On the one hand, a newcomer to the field needs detailed coverage of the basic concepts. On the other hand, feedback from early readers and reviewers indicated that an in-depth and extensive coverage of advanced topics and current issues is desirable and necessary. Providing this complete vision resulted in a text that exceeds the scope of a single-semester class. The more advanced material can be used as the basis for a *graduate class*. The wide coverage and the inclusion of state-of-the-art topics also makes the text useful as a reference work for professional engineers. It is assumed that students taking this course are familiar with the basics of logic design.

The organization of the material is such that the chapters can be taught or read in many ways, as long as a number of precedence relations are adhered to. The core of the text consists of Chapters 5, 6, 7, and 8. Chapters 1 to 4 can be considered as introductory. In response to popular demand, we have introduced a short treatise on semiconductor manufacturing in Chapter 2. Students with a prior introduction to semiconductor devices can traverse quickly through Chapter 3. We urge everyone to do at least that, as a number of important notations and foundations are introduced in that chapter. In addition, an original approach to the modeling of deep-submicron transistors enabling manual analysis, is introduced. To emphasize the importance of interconnect in today's digital design, we have moved the modeling of interconnect forward in the text to Chapter 4.

Chapters 9 to 12 are of a more advanced nature and can be used to provide a certain focus to the course. A course with a focus on the circuit aspects, for example, can supplement the core material with Chapters 9 and 12. A course focused on the digital system design should consider adding (parts of) Chapters 9, 10, and 11. All of these advanced chapters can be used to form the core of a graduate or a follow-on course. Sections considered *advanced* are marked with an *asterisk* in the text.

A number of possible paths through the material for a senior-level class are enumerated below. In the *instructor documentation*, provided on the book's web site, we have included a number of complete syllabi based on courses run at some academic institutions.

Basic circuit class (with minor prior device knowledge):

1, 2.1–3, 3, 4, 5, 6, 7, 8, (9.1–9.3, 12).

Somewhat more advanced circuit coverage:

1, (2, 3), 4, 5, 6, 7, 8, 9, 10.1–10.3, 10.5–10.6, 12.

Course with systems focus:

1, (2, 3), 4, 5, 6, 7, 8, 9, 10.1–10.4, 11, 12.1–12.2.

The *design methodology inserts* are, by preference, covered in concurrence with the chapter to which they are attached.

In order to maintain a consistent flow through each of the chapters, the topics are *introduced* first, followed by a detailed and in-depth discussion of the ideas. A *Perspective* section discusses how the introduced concepts relate to real world designs and how they might be impacted by future evolutions. Each chapter finishes with a *Summary*, which briefly enumerates the topics covered in the text, followed by *To Probe Further* and *Reference* sections. These provide ample references and pointers for a reader interested in further details on some of the material.

As the title of the book implies, one of the goals of this book is to stress the design aspect of digital circuits. To achieve this more practical viewpoint and to provide a real perspective, we have interspersed actual *design examples* and layouts throughout the text. These case studies help to answer questions, such as “How much area or speed or power is really saved by applying this technique?” To mimic the real design process, we are making extensive use of design tools such as circuit- and switch-level simulation as well as layout editing and extraction. Computer analysis is used throughout to verify manual results, to illustrate new concepts, or to examine complex behavior beyond the reach of manual analysis.

Finally, to facilitate the learning process, there are numerous examples included in the text. Each chapter contains a number of *problems or brain-teasers* (answers for which can be found in the back of the book), that provoke thinking and understanding while reading.

The Worldwide Web Companion

A worldwide web companion (<http://bwrc.eecs.berkeley.edu/IcBook/index.htm>) provides fully worked-out design problems and a complete set of overhead transparencies, extracting the most important figures and graphs from the text.

In contrast to the first edition, we have chosen **NOT to include problems sets and design problems** in the text. Instead we decided to make them available **on the book’s web site**. This gives us the opportunity to dynamically upgrade and extend the problems, providing a more effective tool for the instructor. More than 300 challenging *exercises* are currently provided. The goal is to provide the individual reader an independent gauge for his understanding of the material and to provide practice in the use of some of the design tools. Each problem is keyed to the text sections it refers to (e.g., <1.3>), the design tools that must be used when solving the problem (e.g., SPICE) and a rating, ranking the problems on difficulty: (E) easy, (M) moderate, and

(C) challenging. Problems marked with a (D) include a design or research elements. Solutions to the problem sets are available only to instructors of academic institutions that have chosen to adopt our book for classroom use. They are available through the publisher on a password-protected web site.

Open-ended *design problems* help to gain the all-important insight into design optimization and trade-off. The use of design editing, verification and analysis tools is recommended when attempting these design problems. Fully worked out versions of these problems can be found on the web site.

In addition, the book's web site also offers samples of hardware and software laboratories, extra background information, and useful links.

Compelling Features of the Book

- Brings both circuit and systems views on design together. It offers a profound understanding of the design of complex digital circuits, while preparing the designer for new challenges that might be waiting around the corner.
- Design-oriented perspectives are advocated throughout. Design challenges and guidelines are highlighted. Techniques introduced in the text are illustrated with real designs and complete SPICE analysis.
- Is the first circuit design book that *focuses solely on deep-submicron devices*. To facilitate this, a simple transistor model for manual analysis, called the *unified MOS model*, has been developed.
- Unique in showing how to use the latest techniques to design complex high-performance or low-power circuits. Speed and power treated as equal citizens throughout the text.
- Covers crucial real-world system design issues such as signal integrity, power dissipation, interconnect, packaging, timing, and synchronization.
- Provides unique coverage of the latest design methodologies and tools, with a discussion of how to use them from a designers' perspective.
- Offers perspectives on how digital circuit technology might evolve in the future.
- Outstanding illustrations and a usable design-oriented four-color insert.
- To Probe Further and Reference sections provide ample references and pointers for a reader interested in further details on some of the material.
- Extensive instructional package is available over the internet from the author's web site. Includes design software, transparency masters, problem sets, design problems, actual layouts, and hardware and software laboratories.

The Contents at a Glance

A quick scan of the table of contents shows how the ordering of chapters and the material covered are consistent with the advocated design methodology. Starting from a model of the semiconductor devices, we will gradually progress upwards, covering the inverter, the complex logic gate (NAND, NOR, XOR), the functional (adder, multiplier, shifter, register) and the system

module (datapath, controller, memory) levels of abstraction. For each of these layers, the dominant design parameters are identified and simplified models are constructed, abstracting away the nonessential details. While this layered modeling approach is the designer's best handle on complexity, it has some pitfalls. This is illustrated in Chapters 9 and 10, where topics with a global impact, such as interconnect parasitics and chip timing, are discussed. To further express the dichotomy between circuit and system design visions, we have divided the book contents into two major parts: Part II (Chapters 4–7) addresses mostly the circuit perspective of digital circuit design, while Part III (Chapters 8–12) presents a more system oriented vision. Part I (Chapters 1–4) provides the necessary foundation (design metrics, the manufacturing process, device and interconnect models).

Chapter 1 serves as a global *introduction*. After a historical overview of digital circuit design, the concepts of hierarchical design and the different abstraction layers are introduced. A number of fundamental metrics, which help to quantify cost, reliability, and performance of a design, are introduced.

Chapter 2 provides a short and compact introduction to the *MOS manufacturing process*. Understanding the basic steps in the process helps to create the three-dimensional understanding of the MOS transistor, which is crucial when identifying the sources of the device parasitics. Many of the variations in device parameters can also be attributed to the manufacturing process as well. The chapter further introduces the concept of design rules, which form the interface between the designer and the manufacturer. The chapter concludes with an overview of the chip packaging process, an often-overlooked but crucial element of the digital IC design cycle.

Chapter 3 contains a summary of the primary design building blocks, *the semiconductor devices*. The main goal of this chapter is to provide an intuitive understanding of the operation of the MOS as well as to introduce the device models, which are used extensively in the later chapters. Major attention is paid to the artifacts of modern submicron devices, and the modeling thereof. Readers with prior device knowledge can traverse this material rather quickly.

Chapter 4 contains a careful analysis of the *wire*, with interconnect and its accompanying parasitics playing a major role. We visit each of the parasitics that come with a wire (capacitance, resistance, and inductance) in turn. Models for both manual and computer analysis are introduced.

Chapter 5 deals with the nucleus of digital design, the *inverter*. First, a number of fundamental properties of digital gates are introduced. These parameters, which help to quantify the performance and reliability of a gate, are derived in detail for two representative inverter structures: the static complementary CMOS. The techniques and approaches introduced in this chapter are of crucial importance, as they are repeated over and over again in the analysis of other gate structures and more complex gate structures.

In **Chapter 6** this fundamental knowledge is extended to address the design of *simple and complex digital CMOS gates*, such as NOR and NAND structures. It is demonstrated that, depending upon the dominant design constraint (reliability, area, performance, or power), other CMOS gate structures besides the complementary static gate can be attractive. The properties of a number of contemporary gate-logic families are analyzed and compared. Techniques to optimize the performance and power consumption of complex gates are introduced.

Chapter 7 discusses how memory function can be accomplished using either positive feedback or charge storage. Besides analyzing the traditional bistable flip-flops, other sequential circuits such as the mono- and astable multivibrators are also introduced. All chapters prior to **Chapter 7** deal exclusively with combinational circuits, that is circuits without a sense of the past history of the system. *Sequential logic circuits*, in contrast, can remember and store the past state.

All chapters preceding **Chapter 8** present a circuit-oriented approach towards digital design. The analysis and optimization process has been constrained to the individual gate. In this chapter, we take our approach one step further and analyze how gates can be connected together to form the building blocks of a system. The system-level part of the book starts, appropriately, with a discussion of *design methodologies*. Design automation is the only way to cope with the ever-increasing complexity of digital designs. In **Chapter 8**, the prominent ways of producing large designs in a limited time are discussed. The chapter spends considerable time on the different implementation methodologies available to today's designer. Custom versus semi-custom, hardwired versus fixed, regular array versus ad-hoc are some of the issues put forward.

Chapter 9 revisits the impact of *interconnect wiring* on the functionality and performance of a digital gate. A wire introduces parasitic capacitive, resistive, and inductive effects, which are becoming ever more important with the scaling of the technology. Approaches to minimize the impact of these interconnect parasitics on performance, power dissipation and circuit reliability are introduced. The chapter also addresses some important issues such as supply-voltage distribution, and input/output circuitry.

In **Chapter 10** details how that in order to operate sequential circuits correctly, a strict ordering of the switching events has to be imposed. Without these *timing* constraints, wrong data might be written into the memory cells. Most digital circuits use a synchronous, clocked approach to impose this ordering. In **Chapter 10**, the different approaches to digital circuit timing and clocking are discussed. The impact of important effects such as clock skew on the behavior of digital synchronous circuits is analyzed. The synchronous approach is contrasted with alternative techniques, such as self-timed circuits. The chapter concludes with a short introduction to synchronization and clock-generation circuits.

In **Chapter 11**, the design of a variety of complex *arithmetic building blocks* such as adders, multipliers, and shifters, is discussed. This chapter is crucial because it demonstrates how the design techniques introduced in chapters 5 and 6 are extended to the next abstraction layer. The concept of the critical path is introduced and used extensively in the performance analysis and optimization. Higher-level performance models are derived. These help the designer to get a fundamental insight into the operation and quality of a design module, without having to resort to an in-depth and detailed analysis of the underlying circuitry.

Chapter 12 discusses in depth the different memory classes and their implementation. Whenever large amounts of data storage are needed, the digital designer resorts to special circuit modules, called *memories*. Semiconductor memories achieve very high storage density by compromising on some of the fundamental properties of digital gates. Instrumental in the design of reliable and fast memories is the implementation of the peripheral circuitry, such as the decoders, sense amplifiers, drivers, and control circuitry, which are extensively covered.

Finally, as the primary issue in memory design is to ensure that the device works consistently under all operating circumstances, the chapter concludes with a detailed discussion of memory reliability. This chapter as well as the previous one are optional for undergraduate courses.

Acknowledgments

The authors would like to thank all those who contributed to the emergence, creation and correction of this manuscript. First of all, thanks to all the graduate students that helped over the years to bring the text to where it is today. Thanks also to the students of the eeecs141 and eeecs241 courses at Berkeley and the 6.374 course at MIT, who suffered through many of the experimental class offerings based on this book. The feedback from instructors, engineers, and students from all over the world has helped tremendously in focusing the directions of this new edition, and in fine-tuning the final text. The continuous stream of e-mails indicate to us that we are on the right track.

In particular, we would like to acknowledge the contributions of Mary-Jane Irwin, Vijay Narayanan, Eby Friedman, Fred Rosenberger, Wayne Burlison, Shekhar Borkar, Ivo Bolsens, Duane Boning, Olivier Franza, Lionel Kimerling, Josie Ammer, Mike Sheets, Tufan Karalar, Huifang Qin, Rhett Davis, Nathan Chan, Jeb Durant, Andrei Vladimirescu, Radu Zlatanovici, Yasuhisa Shimazaki, Fujio Ishihara, Dejan Markovic, Vladimir Stojanovic, SeongHwan Cho, James Kao, Travis Simpkins, Siva Narendra, James Goodman, Vadim Gutnik, Theodoros Konstantakopoulos, Rex Min, Vikas Mehrotra, and Paul-Peter Sotiriadis. Their help, input, and feedback are greatly appreciated. Obviously, we remain thankful to those who helped create and develop the first edition.

I am extremely grateful to the staff at Prentice Hall, who have been instrumental in turning a rough manuscript into an enjoyable book. First of all, I would like to acknowledge the help and constructive feedback of Tom Robbins, Publisher, Daniel Sandin, Production Editor, and David George, Managing Editor. A special word of thanks to Brenda Vanoni at Berkeley, for her invaluable help in the copy editing and the website creation process. The web expertise of Carol Sitea came in very handy as well.

I would like to highlight to role of computer aids in developing this manuscript. All drafts were completely developed on the FrameMaker publishing system (Adobe Systems). Graphs were mostly created using MATLAB. Microsoft Frontpage is the tool of choice for the web-page creation. For circuit simulations, we used HSPICE (Avant!). All layouts were generated using the Cadence physical design suite.

Finally, some words of gratitude to the people that had to endure the creation process of this book, Kathelij, Karthiyayani, Krithivasan, and Rebecca. While the generation of a new edition brings substantially less pain than a first edition, we consistently underestimate what it takes, especially in light of the rest of our daily loads. They have been a constant support, help and encouragement during the writing of this manuscript.

JAN M. RABAEY
ANANTHA CHANDRAKASAN
BORIVOJE NIKOLIĆ
Berkeley, Calistoga, Cambridge

Contents

| | | |
|------------------|--|-----------|
| Part 1 | The Fabrics | 1 |
| Chapter 1 | Introduction | 3 |
| 1.1 | A Historical Perspective | 4 |
| 1.2 | Issues in Digital Integrated Circuit Design | 6 |
| 1.3 | Quality Metrics of a Digital Design | 15 |
| 1.3.1 | Cost of an Integrated Circuit | 16 |
| 1.3.2 | Functionality and Robustness | 18 |
| 1.3.3 | Performance | 27 |
| 1.3.4 | Power and Energy Consumption | 30 |
| 1.4 | Summary | 31 |
| 1.5 | To Probe Further | 31 |
| | Reference Books | 32 |
| | References | 33 |
| Chapter 2 | The Manufacturing Process | 35 |
| 2.1 | Introduction | 36 |
| 2.2 | Manufacturing CMOS Integrated Circuits | 36 |
| 2.2.1 | The Silicon Wafer | 37 |
| 2.2.2 | Photolithography | 37 |
| 2.2.3 | Some Recurring Process Steps | 41 |
| 2.2.4 | Simplified CMOS Process Flow | 42 |
| 2.3 | Design Rules—The Contract between Designer and Process Engineer | 47 |
| 2.4 | Packaging Integrated Circuits | 51 |
| 2.4.1 | Package Materials | 52 |
| 2.4.2 | Interconnect Levels | 53 |
| 2.4.3 | Thermal Considerations in Packaging | 59 |
| 2.5 | Perspective—Trends in Process Technology | 61 |
| 2.5.1 | Short-Term Developments | 61 |
| 2.5.2 | In the Longer Term | 63 |
| 2.6 | Summary | 64 |

| | | |
|--|--|------------|
| 2.7 | To Probe Further | 64 |
| | References | 64 |
| <i>Design Methodology Insert A IC LAYOUT</i> | | 67 |
| A.1 | To Probe Further | 71 |
| | References | 71 |
| <i>Chapter 3 The Devices</i> | | 73 |
| 3.1 | Introduction | 74 |
| 3.2 | The Diode | 74 |
| 3.2.1 | A First Glance at the Diode—The Depletion Region | 75 |
| 3.2.2 | Static Behavior | 77 |
| 3.2.3 | Dynamic, or Transient, Behavior | 80 |
| 3.2.4 | The Actual Diode—Secondary Effects | 84 |
| 3.2.5 | The SPICE Diode Model | 85 |
| 3.3 | The MOS(FET) Transistor | 87 |
| 3.3.1 | A First Glance at the Device | 87 |
| 3.3.2 | The MOS Transistor under Static Conditions | 88 |
| 3.3.3 | The Actual MOS Transistor—Some Secondary Effects | 114 |
| 3.3.4 | SPICE Models for the MOS Transistor | 117 |
| 3.4 | A Word on Process Variations | 120 |
| 3.5 | Perspective—Technology Scaling | 122 |
| 3.6 | Summary | 128 |
| 3.7 | To Probe Further | 129 |
| | References | 130 |
| <i>Design Methodology Insert B Circuit Simulation</i> | | 131 |
| | References | 134 |
| <i>Chapter 4 The Wire</i> | | 135 |
| 4.1 | Introduction | 136 |
| 4.2 | A First Glance | 136 |
| 4.3 | Interconnect Parameters—Capacitance, Resistance, and Inductance | 138 |
| 4.3.1 | Capacitance | 138 |
| 4.3.2 | Resistance | 144 |
| 4.3.3 | Inductance | 148 |
| 4.4 | Electrical Wire Models | 150 |
| 4.4.1 | The Ideal Wire | 151 |
| 4.4.2 | The Lumped Model | 151 |
| 4.4.3 | The Lumped RC Model | 152 |
| 4.4.4 | The Distributed rc Line | 156 |
| 4.4.5 | The Transmission Line | 159 |

| | | |
|-------|-------------------------------------|-----|
| 4.5 | SPICE Wire Models | 170 |
| 4.5.1 | Distributed rc Lines in SPICE | 170 |
| 4.5.2 | Transmission Line Models in SPICE | 170 |
| 4.5.3 | Perspective: A Look into the Future | 171 |
| 4.6 | Summary | 174 |
| 4.7 | To Probe Further | 174 |
| | References | 174 |

| | | |
|---------------|------------------------------|------------|
| Part 2 | A Circuit Perspective | 177 |
|---------------|------------------------------|------------|

| | | |
|------------------|--------------------------|------------|
| Chapter 5 | The CMOS Inverter | 179 |
|------------------|--------------------------|------------|

| | | |
|-------|---|-----|
| 5.1 | Introduction | 180 |
| 5.2 | The Static CMOS Inverter—An Intuitive Perspective | 180 |
| 5.3 | Evaluating the Robustness of the CMOS Inverter: The Static Behavior | 184 |
| 5.3.1 | Switching Threshold | 185 |
| 5.3.2 | Noise Margins | 188 |
| 5.3.3 | Robustness Revisited | 191 |
| 5.4 | Performance of CMOS Inverter: The Dynamic Behavior | 193 |
| 5.4.1 | Computing the Capacitances | 194 |
| 5.4.2 | Propagation Delay: First-Order Analysis | 199 |
| 5.4.3 | Propagation Delay from a Design Perspective | 203 |
| 5.5 | Power, Energy, and Energy Delay | 213 |
| 5.5.1 | Dynamic Power Consumption | 214 |
| 5.5.2 | Static Consumption | 223 |
| 5.5.3 | Putting It All Together | 225 |
| 5.5.4 | Analyzing Power Consumption Using SPICE | 227 |
| 5.6 | Perspective: Technology Scaling and its Impact on the Inverter Metrics | 229 |
| 5.7 | Summary | 232 |
| 5.8 | To Probe Further | 233 |
| | References | 233 |

| | | |
|------------------|--|------------|
| Chapter 6 | Designing Combinational Logic Gates in CMOS | 235 |
|------------------|--|------------|

| | | |
|-------|--|-----|
| 6.1 | Introduction | 236 |
| 6.2 | Static CMOS Design | 236 |
| 6.2.1 | Complementary CMOS | 237 |
| 6.2.2 | Ratioed Logic | 263 |
| 6.2.3 | Pass-Transistor Logic | 269 |
| 6.3 | Dynamic CMOS Design | 284 |
| 6.3.1 | Dynamic Logic: Basic Principles | 284 |
| 6.3.2 | Speed and Power Dissipation of Dynamic Logic | 287 |

| | | |
|---|---|------------|
| 6.3.3 | Signal Integrity Issues in Dynamic Design | 290 |
| 6.3.4 | Cascading Dynamic Gates | 295 |
| 6.4 | Perspectives | 303 |
| 6.4.1 | How to Choose a Logic Style? | 303 |
| 6.4.2 | Designing Logic for Reduced Supply Voltages | 303 |
| 6.5 | Summary | 306 |
| 6.6 | To Probe Further | 307 |
| | References | 308 |
| Design Methodology Insert C How to Simulate Complex Logic Circuits | | 309 |
| C.1 | Representing Digital Data as a Continuous Entity | 310 |
| C.2 | Representing Data as a Discrete Entity | 310 |
| C.3 | Using Higher-Level Data Models | 315 |
| | References | 317 |
| Design Methodology Insert D Layout Techniques for Complex Gates | | 319 |
| Chapter 7 | Designing Sequential Logic Circuits | 325 |
| 7.1 | Introduction | 326 |
| 7.1.1 | Timing Metrics for Sequential Circuits | 327 |
| 7.1.2 | Classification of Memory Elements | 328 |
| 7.2 | Static Latches and Registers | 330 |
| 7.2.1 | The Bistability Principle | 330 |
| 7.2.2 | Multiplexer-Based Latches | 332 |
| 7.2.3 | Master-Slave Edge-Triggered Register | 333 |
| 7.2.4 | Low-Voltage Static Latches | 339 |
| 7.2.5 | Static SR Flip-Flops—Writing Data by Pure Force | 341 |
| 7.3 | Dynamic Latches and Registers | 344 |
| 7.3.1 | Dynamic Transmission-Gate Edge-triggered Registers | 344 |
| 7.3.2 | C ² MOS—A Clock-Skew Insensitive Approach | 346 |
| 7.3.3 | True Single-Phase Clocked Register (TSPCR) | 350 |
| 7.4 | Alternative Register Styles* | 354 |
| 7.4.1 | Pulse Registers | 354 |
| 7.4.2 | Sense-Amplifier-Based Registers | 356 |
| 7.5 | Pipelining: An Approach to Optimize Sequential Circuits | 358 |
| 7.5.1 | Latch- versus Register-Based Pipelines | 360 |
| 7.5.2 | NORA-CMOS—A Logic Style for Pipelined Structures | 361 |
| 7.6 | Nonbistable Sequential Circuits | 364 |
| 7.6.1 | The Schmitt Trigger | 364 |
| 7.6.2 | Monostable Sequential Circuits | 367 |
| 7.6.3 | Astable Circuits | 368 |
| 7.7 | Perspective: Choosing a Clocking Strategy | 370 |
| 7.8 | Summary | 371 |