GRAY • HURST • LEWIS • MEYER

Analysis and Design of Analog Integrated Circuits

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INTERNATIONAL STUDENT VERSION

ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

Fifth Edition

International Student Version

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Preface

Since the publication of the first edition of this book, the field of analog integrated circuits has developed and matured. The initial groundwork was laid in bipolar technology, followed by a rapid evolution of MOS analog integrated circuits. Thirty years ago, CMOS technologies were fast enough to support applications only at audio frequencies. However, the continuing reduction of the minimum feature size in integrated-circuit (IC) technologies has greatly increased the maximum operating frequencies, and CMOS technologies have become fast enough for many new applications as a result. For example, the bandwidth in some video applications is about 4 MHz, requiring bipolar technologies as recently as about 23 years ago. Now, however, CMOS easily can accommodate the required bandwidth for video and is being used for radio-frequency applications. Today, bipolar integrated circuits are used in some applications that require very low noise, very wide bandwidth, or driving low-impedance loads.

In this fifth edition, coverage of the bipolar 741 op amp has been replaced with a low-voltage bipolar op amp, the NE5234, with rail-to-rail common-mode input range and almost rail-to-rail output swing. Analysis of a fully differential CMOS folded-cascode operational amplifier (op amp) is now included in Chapter 12. The 560B phase-locked loop, which is no longer commercially available, has been deleted from Chapter 10.

The SPICE computer analysis program is now readily available to virtually all electrical engineering students and professionals, and we have included extensive use of SPICE in this edition, particularly as an integral part of many problems. We have used computer analysis as it is most commonly employed in the engineering design process—both as a more accurate check on hand calculations, and also as a tool to examine complex circuit behavior beyond the scope of hand analysis.

An in-depth look at SPICE as an indispensable tool for IC robust design can be found in The SPICE Book, 2nd ed., published by J. Wiley and Sons. This text contains many worked out circuit designs and verification examples linked to the multitude of analyses available in the most popular versions of SPICE. The SPICE Book conveys the role of simulation as an integral part of the design process, but not as a replacement for solid circuit-design knowledge.

This book is intended to be useful both as a text for students and as a reference book for practicing engineers. For class use, each chapter includes many worked problems; the problem sets at the end of each chapter illustrate the practical applications of the material in the text. All of the authors have extensive industrial experience in IC design and in the teaching of courses on this subject; this experience is reflected in the choice of text material and in the problem sets.

Although this book is concerned largely with the analysis and design of ICs, a considerable amount of material also is included on applications. In practice, these two subjects are closely linked, and a knowledge of both is essential for designers and users of ICs. The latter compose the larger group by far, and we believe that a working knowledge of IC design is a great advantage to an IC user. This is particularly apparent when the user must choose from among a number of competing designs to satisfy a particular need. An understanding of the IC structure is then useful in evaluating the relative desirability of the different designs under extremes of environment or in the presence of variations in supply voltage. In addition, the IC user is in a

much better position to interpret a manufacturer's data if he or she has a working knowledge of the internal operation of the integrated circuit.

The contents of this book stem largely from courses on analog integrated circuits given at the University of California at the Berkeley and Davis campuses. The courses are senior-level electives and first-year graduate courses. The book is structured so that it can be used as the basic text for a sequence of such courses. The more advanced material is found at the end of each chapter or in an appendix so that a first course in analog integrated circuits can omit this material without loss of continuity. An outline of each chapter is given below with suggestions for material to be covered in such a first course. It is assumed that the course consists of three hours of lecture per week over a 15-week semester and that the students have a working knowledge of Laplace transforms and frequency-domain circuit analysis. It is also assumed that the students have had an introductory course in electronics so that they are familiar with the principles of transistor operation and with the functioning of simple analog circuits. Unless otherwise stated, each chapter requires three to four lecture hours to cover.

Chapter 1 contains a summary of bipolar transistor and MOS transistor device physics. We suggest spending one week on selected topics from this chapter, with the choice of topics depending on the background of the students. The material of Chapters 1 and 2 is quite important in IC design because there is significant interaction between circuit and device design, as will be seen in later chapters. A thorough understanding of the influence of device fabrication on device characteristics is essential.

Chapter 2 is concerned with the technology of IC fabrication and is largely descriptive. One lecture on this material should suffice if the students are assigned the chapter to read.

Chapter 3 deals with the characteristics of elementary transistor connections. The material on one-transistor amplifiers should be a review for students at the senior and graduate levels and can be assigned as reading. The section on two-transistor amplifiers can be covered in about three hours, with greatest emphasis on differential pairs. The material on device mismatch effects in differential amplifiers can be covered to the extent that time allows.

In Chapter 4, the important topics of current mirrors and active loads are considered. These configurations are basic building blocks in modern analog IC design, and this material should be covered in full, with the exception of the material on band-gap references and the material in the appendices.

Chapter 5 is concerned with output stages and methods of delivering output power to a load. Integrated-circuit realizations of Class A, Class B, and Class AB output stages are described, as well as methods of output-stage protection. A selection of topics from this chapter should be covered.

Chapter 6 deals with the design of operational amplifiers (op amps). Illustrative examples of dc and ac analysis in both MOS and bipolar op amps are performed in detail, and the limitations of the basic op amps are described. The design of op amps with improved characteristics in both MOS and bipolar technologies are considered. This key chapter on amplifier design requires at least six hours.

In Chapter 7, the frequency response of amplifiers is considered. The zero-value time-constant technique is introduced for the calculations of the –3-dB frequency of complex circuits. The material of this chapter should be considered in full.

Chapter 8 describes the analysis of feedback circuits. Two different types of analysis are presented: two-port and return-ratio analyses. Either approach should be covered in full with the section on voltage regulators assigned as reading.

Chapter 9 deals with the frequency response and stability of feedback circuits and should be covered up to the section on root locus. Time may not permit a detailed discussion of root locus, but some introduction to this topic can be given.

In a 15-week semester, coverage of the above material leaves about two weeks for Chapters 10, 11, and 12. A selection of topics from these chapters can be chosen as follows. Chapter 10 deals with nonlinear analog circuits and portions of this chapter up to Section 10.2 could be covered in a first course. Chapter 11 is a comprehensive treatment of noise in integrated circuits and material up to and including Section 11.4 is suitable. Chapter 12 describes fully differential operational amplifiers and common-mode feedback and may be best suited for a second course.

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Berkeley and Davis, CA, 2008

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Symbol Convention

Unless otherwise stated, the following symbol convention is used in this book. *Bias* or *dc* quantities, such as transistor collector current I_C and collector-emitter voltage V_{CE}, are represented by uppercase symbols with uppercase subscripts. Small-signal quantities, such as the incremental change in transistor collector current i_c, are represented by lowercase symbols with lowercase subscripts. Elements such as transconductance g_m in small-signal equivalent circuits are represented in the same way. Finally, quantities such as *total* collector current I_c, which represent the sum of the bias quantity *and* the signal quantity, are represented by an uppercase symbol with a lowercase subscript.

CHAPTER 1

Models for Integrated-Circuit Active Devices

1.1 Introduction

The analysis and design of integrated circuits depend heavily on the utilization of suitable models for integrated-circuit components. This is true in hand analysis, where fairly simple models are generally used, and in computer analysis, where more complex models are encountered. Since any analysis is only as accurate as the model used, it is essential that the circuit designer have a thorough understanding of the origin of the models commonly utilized and the degree of approximation involved in each.

This chapter deals with the derivation of large-signal and small-signal models for integrated-circuit devices. The treatment begins with a consideration of the properties of *pn* junctions, which are basic parts of most integrated-circuit elements. Since this book is primarily concerned with circuit analysis and design, no attempt has been made to produce a comprehensive treatment of semiconductor physics. The emphasis is on summarizing the basic aspects of semiconductor-device behavior and indicating how these can be modeled by equivalent circuits.

1.2 Depletion Region of a *pn* Junction

The properties of reverse-biased *pn* junctions have an important influence on the characteristics of many integrated-circuit components. For example, reverse-biased *pn* junctions exist between many integrated-circuit elements and the underlying substrate, and these junctions all contribute voltage-dependent parasitic capacitances. In addition, a number of important characteristics of active devices, such as breakdown voltage and output resistance, depend directly on the properties of the depletion region of a reverse-biased *pn* junction. Finally, the basic operation of the junction field-effect transistor is controlled by the width of the depletion region of a *pn* junction. Because of its importance and application to many different problems, an analysis of the depletion region of a reverse-biased *pn* junction is considered below. The properties of forward-biased *pn* junctions are treated in Section 1.3 when bipolar-transistor operation is described.

Consider a *pn* junction under reverse bias as shown in Fig. 1.1. Assume *constant doping densities* of N_D atoms/cm^3 in the n-type material and N_A atoms/cm^3 in the p-type material. (The characteristics of junctions with nonconstant doping densities will be described later.) Due to the difference in carrier concentrations in the p-type and n-type regions, there exists a region at the junction where the mobile holes and electrons have been removed, leaving the fixed acceptor and donor ions. Each acceptor atom carries a negative charge and each donor atom carries a positive charge, so that the region near the junction is one of significant space charge and resulting high electric field. This is called the *depletion* region or *space-charge*

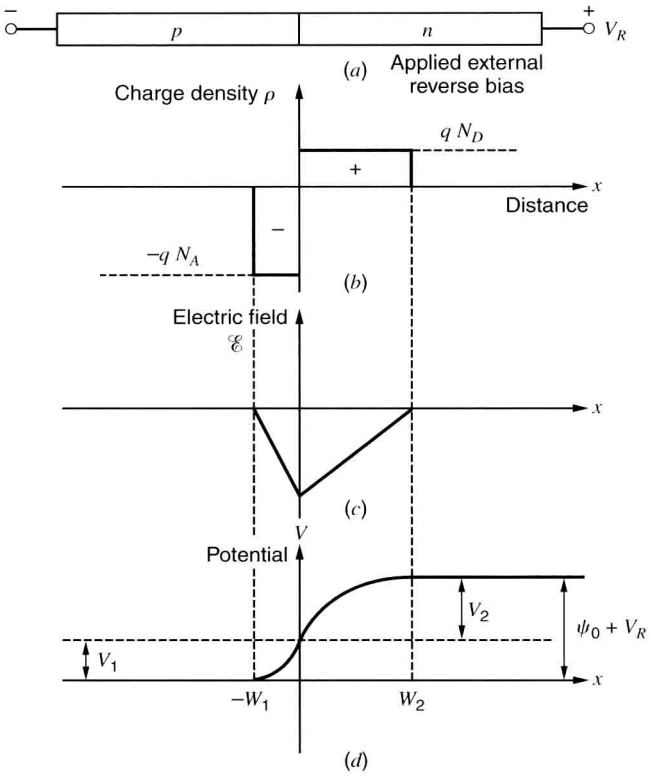

Figure 1.1 The abrupt junction under reverse bias V_R. (*a*) Schematic. (*b*) Charge density. (*c*) Electric field. (*d*) Electrostatic potential.

region. It is assumed that the edges of the depletion region are sharply defined as shown in Fig. 1.1, and this is a good approximation in most cases.

For zero applied bias, there exists a voltage ψ_0 across the junction called the *built-in potential*. This potential opposes the diffusion of mobile holes and electrons across the junction in equilibrium and has a value[1]

$$\psi_0 = V_T \ln \frac{N_A N_D}{n_i^2} \tag{1.1}$$

where

$$V_T = \frac{kT}{q} \simeq 26 \text{ mV} \quad \text{at} \quad 300^\circ\text{K}$$

the quantity n_i is the intrinsic carrier concentration in a pure sample of the semiconductor and $n_i \simeq 1.5 \times 10^{10}\text{cm}^{-3}$ at 300°K for silicon.

In Fig. 1.1 the built-in potential is augmented by the applied reverse bias, V_R, and the total voltage across the junction is $(\psi_0 + V_R)$. If the depletion region penetrates a distance W_1 into the p-type region and W_2 into the n-type region, then we require

$$W_1 N_A = W_2 N_D \tag{1.2}$$

because the total charge per unit area on either side of the junction must be equal in magnitude but opposite in sign.

Poisson's equation in one dimension requires that

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\epsilon} = \frac{qN_A}{\epsilon} \quad \text{for} \quad -W_1 < x < 0 \tag{1.3}$$

where ρ is the charge density, q is the electron charge (1.6×10^{-19} coulomb), and ϵ is the permittivity of the silicon (1.04×10^{-12} farad/cm). The permittivity is often expressed as

$$\epsilon = K_S \epsilon_0 \tag{1.4}$$

where K_S is the dielectric constant of silicon and ϵ_0 is the permittivity of free space (8.86×10^{-14} F/cm). Integration of (1.3) gives

$$\frac{dV}{dx} = \frac{qN_A}{\epsilon}x + C_1 \tag{1.5}$$

where C_1 is a constant. However, the electric field $\mathscr{E}$ is given by

$$\mathscr{E} = -\frac{dV}{dx} = -\left(\frac{qN_A}{\epsilon}x + C_1\right) \tag{1.6}$$

Since there is zero electric field outside the depletion region, a boundary condition is

$$\mathscr{E} = 0 \quad \text{for} \quad x = -W_1$$

and use of this condition in (1.6) gives

$$\mathscr{E} = -\frac{qN_A}{\epsilon}(x + W_1) = -\frac{dV}{dx} \quad \text{for} \quad -W_1 < x < 0 \tag{1.7}$$

Thus the dipole of charge existing at the junction gives rise to an electric field that varies linearly with distance.

Integration of (1.7) gives

$$V = \frac{qN_A}{\epsilon}\left(\frac{x^2}{2} + W_1 x\right) + C_2 \tag{1.8}$$

If the zero for potential is arbitrarily taken to be the potential of the neutral p-type region, then a second boundary condition is

$$V = 0 \quad \text{for} \quad x = -W_1$$

and use of this in (1.8) gives

$$V = \frac{qN_A}{\epsilon}\left(\frac{x^2}{2} + W_1 x + \frac{W_1^2}{2}\right) \quad \text{for} \quad -W_1 < x < 0 \tag{1.9}$$

At $x = 0$, we define $V = V_1$, and then (1.9) gives

$$V_1 = \frac{qN_A}{\epsilon}\frac{W_1^2}{2} \tag{1.10}$$

If the potential difference from $x = 0$ to $x = W_2$ is V_2, then it follows that

$$V_2 = \frac{qN_D}{\epsilon}\frac{W_2^2}{2} \tag{1.11}$$

and thus the total voltage across the junction is

$$\psi_0 + V_R = V_1 + V_2 = \frac{q}{2\epsilon}(N_A W_1^2 + N_D W_2^2) \tag{1.12}$$