

**1997**

**INTERNATIONAL SYMPOSIUM ON  
VLSI TECHNOLOGY, SYSTEMS,  
AND APPLICATIONS**

**PROCEEDINGS OF**

**TECHNICAL PAPERS**

**June 3 - 5, 1997**

**LAI LAI SHERATON HOTEL  
TAIPEI, TAIWAN, ROC**

Library of Congress Number  
IEEE Catalog Number 97TH8303

73.7551083  
I 22



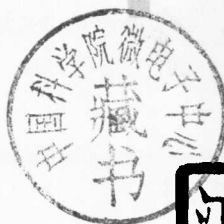
1997

INTERNATIONAL SYMPOSIUM ON  
VLSI TECHNOLOGY, SYSTEMS,  
AND APPLICATIONS

PROCEEDINGS OF

TECHNICAL PAPERS

001688



江苏工业学院图书馆  
藏书章

RBC85 / 04

Library of Congress Number  
IEEE Catalog Number 97TH8303

June 3 - 5, 1997  
LAI LAI SHERATON HOTEL  
TAIPEI, TAIWAN, ROC



Abstracting is permitted with credit to the source. Libraries are permitted to photocopy articles in this volume beyond the limits of U.S. copyright law without fee if for private, non-commercial use of patrons. Instructors are permitted to photocopy isolated articles for non-commercial classroom use without fee. For other copying, reprint, or republication permission, write to Director, Publishing Services, IEEE, 345 East 47th Street, New York, NY 10017. All rights reserved. Copyright 1989, 1991, 1993 by the Institute of Electrical and Electronics Engineers, Inc. 1983, 1985, 1987, 1989, 1991, 1993, 1995 by the NSC and ITRI.

---

Library of Congress Number

IEEE Catalog Number 97TH8303

ISBN: 0-7803-4131-7      Softbound Edition

0-7803-4132-5      Microfiche Edition

---

**Publication Office**

ERSO, ITRI

B000, Bldg. 11, 195-4 Sec. 4, Chung Hsing Rd.,

Chutung, Hsinchu, Taiwan, (31015), R.O.C.

**Copies of this Proceedings may be obtained from:**

ERSO, ITRI

B400, Bldg. 11, 195-4, Sec. 4, Chung Hsing Rd.,

Chutung, Hsinchu, Taiwan (31015), R.O.C.

Tel: +886-3-5917232

Fax: +886-3-5820056

E-mail: [rachel@erso.itri.org.tw](mailto:rachel@erso.itri.org.tw)

**IEEE Service Center:**

445 Hoës Lane

P.O. Box 1331

Piscataway, NJ 08855-1331

U.S.A

Tel: (908) 562-3900

Fax: (908) 562-1571

## FOREWORD

### Welcome to the 1997 International Symposium on VLSI-TSA

This year marks the 14th anniversary of the Symposium, and it also coincides with the 50th birthday of the transistor. As we all know, ever since the commercialization of the first integrated circuits, the "Moore's Law" has ruled the microelectronics industry, and there are reasons to believe that this exponential trend will continue for the foreseeable future. Therefore, it is befitting to see a continued growth of this symposium, as it not only reflects the technical advances in VLSI around the world, but also echoes the rapid development of the VLSI industry in Taiwan, the host location of this symposium.

This year's Technical Program Committee selected 65 contributed papers out of 183 abstracts submitted from 19 countries and regions around the world. The paper acceptance ratio is thus a record low of 36%, and the Committee had a difficult task of rejecting many high quality papers. The contributed papers constitute 10 technical sessions, which coincide with the number of invited papers given by leading experts in their respective fields.

To celebrate the 50th anniversary of the invention of the transistor, we are honored to have Dr. Ian M. Ross, President Emeritus of AT&T Bell Laboratories, USA, to give the opening keynote speech entitled "The Transistor Anniversary". We also have the pleasure of two other distinguished plenary speakers, Dr. Hiroyoshi Komiya, COO of SELETE, Japan, who will talk about "Challenges to the 300mm Technology", and Mr. Peter Baltus of the Philips Research Laboratories, the Netherlands, whose topic is "Design Issues for Low Power Mobile Transceiver Frontends". To top it off, this year we have the pleasure of a special luncheon speech by Dr. F. H. Hsu of the IBM Deep Blue team, who will talk about the well publicized chess match last year and the recent rematch between Deep Blue and Garry Kasparov, the World Champion.

I would like to express my gratitude to all members of the Technical Program Committee for their dedication and hard work in putting together this program. In particular, I would like to thank Drs. Tak Ning and Jyuo-Min Shyu, the Co-Chairs of the Program Committee, for their critical support, and Drs. K. Fujishima and W. Sansen for their coordination in Japan and Europe. My special thanks go to Dr. Ping Yang, the Symposium Chair, for sharing his experience and continued help. It is also my sincere wish to thank Drs. Chintay Shih, Genda Hu, Lewis Terman, and H. N. Yu for their unwavering support and invaluable guidance. In addition, I would like to acknowledge the sponsoring organizations, the Industrial Technology Research Institute (ITRI) and National Science Council of ROC for making this symposium possible. In closing, I wish to extend my deepest gratitude to Ms. Rachel Huang, our Symposium Secretary, for all the detailed preparation and thoughtful arrangements that every attendee of this symposium enjoys.

T. P. Ma

Technical Program Committee Chairman

## SYMPOSIUM ORGANIZATION

### Honorary Chairman

Chintay Shih      ITRI, ROC

### Symposium Chairman

Ping Yang      TI, USA

### Symposium Co-Chairmen

Lewis M. Terman      IBM, USA

Genda J. Hu      ERSO/ITRI, ROC

### ADVISORY COMMITTEE

Morris Chang      TSMC/Vanguard, ROC

Parkson Chen      TMC, ROC

Chao-Yih Chen      Dept. of Industrial Technology,  
MOEA, ROC

Alex Cheng      TI-Acer, ROC

D. H. Hu      Macronix, ROC

Archie Huang      Hermes, ROC

C. C. Huang      Sunplus, ROC

Nicky Lu      Etron, ROC

Simon M. Sze      National Chiao Tung University, ROC

H. C. Hu      Mosel-Vitellic, ROC

Robert H. C. Tsao      UMC, ROC

F. C. Tseng      Vanguard, ROC

Keith Wu      Holtek, ROC

D. Y. Yang      Winbond, ROC

### STEERING COMMITTEE

C. Y. Chang      National Chiao Tung University, ROC

John Chen      WaferTech, USA

Alice Chiang      Teratech, USA

L. P. Hsu      Philips, ROC

John Hsuan      UMC, ROC

Min-Shyong Lin      ITRI, ROC

Eric Lean      OES/ITRI, ROC

C.Y. Lu      Vanguard, ROC

Min Wu      Macronix, ROC

Hwa-Nien Yu      IBM Emeritus, USA

### TECHNICAL PROGRAM COMMITTEE

#### Chairman

T. P. Ma      Yale University, USA

#### Co-Chairmen

Tak Ning      IBM, USA

Jyuo-Min Shyu      ERSO/ITRI, ROC

#### Technology Subcommittee

Tak Ning      IBM, USA (Chair)

Ih-Chin Chen      TI, USA

Albert Chin      National Chiao Tung Univ., ROC

K. Y. Chiu      Winbond, ROC

Aart van Gorkum      Philips, ROC

Charles C. H. Hsu      National Tsing Hua Univ., ROC

Chenming Hu      UC Berkeley, USA

Jammy J. M. Huang      ERSO/ITRI, ROC

Dim-Lee Kwong      University of Texas, USA

Stefan Lai      Intel, USA

Chien-Ping Lee      National Chiao Tung University, ROC

Vojin G. Oklobdzija      UC Davis, USA

Fuchia Shone      Macronix, ROC

Jack Y.-C. Sun      IBM, USA

S. C. Sun      TSMC, ROC

Shih-Wei Sun      UMC, ROC

Hong-Hsiang Tsai      Vanguard, ROC

Ben B. C. Tseng      Powerchip, ROC

Hsing-Huang Tseng      Motorola, USA

Cary Y. Yang      Santa Clara University, USA

#### CAD/CAM Subcommittee

Andrew T. Yang      Avanti, USA (Chair)

Mi-Chang Chang      TI, USA

Shieh-Wuu Lee      Intel, USA

Pole-Shang Lin      Silicon-based Technology, ROC

Shen Lin      LSI Logic, USA

Young-Lung Lin      National Tsing Hua Univ., ROC

Wen-Zen Shen      National Chiao Tung Univ., ROC

Jyuo-Min Shyu      ERSO/ITRI, ROC

Y-Fu Tsao            TSMC, ROC  
 Zhipping Yu        Stanford University, USA

#### **Circuits Subcommittee**

Belle W. Y. Wei      San Jose State University, USA (Chair)  
 Peter J. Lim          Oak Technology, USA  
 Ming-Guan Lin      Silicon-based Technology, ROC  
 Marios Papaefthymiou Yale Univ., USA

Mehmet Soyuer      IBM, USA  
 Jeffrey Y. Tang      Myson, ROC  
 Joseph T. K. Ting    Etron, ROC  
 Jieh-Tsorng Wu      National Chiao Tung University., ROC  
 Jin-Tsuan Wu        National Chiao Tung University., ROC  
 Ran-Hong Yan        Lucent Technology, USA

#### **Systems Subcommittee**

Eric Kronstadt        IBM, USA (Chair)  
 Peng H. Ang          TeraLogic, USA  
 Liang-Gee Chen      National Taiwan University., ROC  
 Chi-Yuang Chin      CCL/ITRI, ROC  
 Ran-Fun Chiu        HP, USA  
 Sharon Chuang        IBM, USA  
 Wen-Jay Hsu          Sun Microsystems, USA  
 Chein-Wei Jen        National Chiao Tung Univ., ROC  
 C. Bernard Shung    National Chiao Tung Univ., ROC  
 Jeremy C. P. Tzeng    Alfa, ROC

#### **Technical Program Japanese Subcommittee**

Kazuyasu Fujishima   Mitsubishi, Japan (Chair)  
 Hisakazu Edamatsu    Matsushita, Japan  
 Hiroshi Hanafusa      Sanyo Electric, Japan  
 Noboru Ishihara        NTT System Electronics Lab., Japan  
 Masakazu Kakumu      Toshiba, Japan  
 Seiichi Kawamura      Fujitsu, Japan  
 Koichiro Mashiko      Mitsubishi, Japan  
 Makoto Motomura      NEC, Japan  
 Yoshinobu Nakagome   Hitachi, Japan  
 Futao Yamaguchi        SONY, Japan

#### **Technical Program European Subcommittee**

Willy Sansen          Katholieke Universiteit Leuven,  
                                  Belgium (Chair)  
 Giorgio Baccarani    University of Bologna, Italy  
 Mart Graef            Philips Research Labs.,  
                                  The Netherlands  
 Rudolf Koch          Siemens, Germany

#### **LOCAL ORGANIZING COMMITTEE**

Jyuo-Min Shyu        Chair  
 Rachel L.C. Huang    Secretary  
 C. C. Hu              Registration  
 Christy C. F. Pai      Public Relations  
 C. C. Liu              Conference Assistance  
 G. Y. Chao            Art Work  
 G. M. Chiou            Facility  
 S. F. Wang            Treasurer

# CONTENT

## PLENARY SESSION

<b>K1. The Transistor Anniversary</b>	
Dr. Ian M. Ross .....	1
<b>K2. Design Issues for Low power Mobile Transceiver Frontends</b>	
Peter Baltus .....	9
<b>K3. Challenges to the 300mm Technology</b>	
Hiroyoshi Komiya .....	14

## SESSION A: Interconnect Technology/ESD

<b>A1. Copper Interconnect: Fabrication and Reliability (Invited)</b>	
C.-K. Hu and J.M.E. Harper .....	18
<b>A2. Study of Integration Issues of Ti Salicide Process with Pre-amorphization for Sub-0.18 <math>\mu</math>m Gate Length CMOS Technologies</b>	
J.A. Kittl, A. Chatterjee, I.-C. Chen, G.A. Dixit, P.P. Apte, D.A. Prinslow, and Q.Z. Hong .....	23
<b>A3. Device Degradation Associated with Preamorphization Implant (PAI) of the Ti SALICIDE Process</b>	
Jiunn-Yann Tsai and Stanley W.-C. Yeh .....	28
<b>A4. Electrical Characteristics of Ti-Saliced nMOSFETs with Asymmetric Source/Drain Regions</b>	
Jaesung Lee, Kwangsoo Kim, Jinsu Han, Jaegab Kim, and Hunsu Park .....	34
<b>A5. Challenges and Issues of Low-K Dielectrics (Invited)</b>	
Chien Chiang, Anne. S. Mack, Chuanbin Pan, and David B. Fraser .....	37
<b>A6. Efficient Output ESD Protection of High-Speed SRAM IC with Well-Couple Technique in Sub-<math>\mu</math>m CMOS Technology</b>	
C.-N. Wu, M.-D. Ker*, T.-L. Yu, S.-T. Lin, K.-L. Young, and K.-Y. Chiu .....	40
<b>A7. Advanced Layout Design for Deep-Submicron CMOS Output Buffer with Higher Driving Capability and Better ESD Reliability</b>	
Ming-Dou Ker, Chung-Yu Wu*, and Tung-Yang Chen* .....	45
<b>A8. Fluorine Penetration Suppression by Applying Amorphous Silicon in WSi Gate Process</b>	
Han-Ching Wang, Chun-Hsing Shih, and Wen-Yueh Jang .....	50

## SESSION B: High-Performance Circuits & Mixed Signal Design Techniques

<b>B1. Image Capture Circuits in CMOS (Invited)</b>	
Eric R. Fossum .....	52
<b>B2. A High-Resolution CMOS Imager with Active Pixel using Capacitively-Coupled Bipolar Operation</b>	
Min-hwa Chi, Tobi Delbruck*, Nick Mascarenhas*, Albert Bergemont, and Carver Mead* .....	58
<b>B3. An Easy to Design Rail-to-Rail CMOS Op Amp with High CMRR</b>	
Geoffroy Klisnick and Michel Redon .....	62
<b>B4. A CMOS 10-bit 80 Msample/s ADC with Reference</b>	
Tzi-Hsiung Shu, Bruce J. Tesch, and Kantilal Bacrania .....	65

<b>B5. Area-Efficient VDD-to-VSS ESD Clamp Circuit by Using Substrate-Triggering Field-Oxide Device (STFOD) for Whole-Chip ESD Protection</b>	
Ming-Dou Ker .....	69
<b>B6. Reduction of Crosstalk in Mixed Signal Integrated Circuits</b>	
Drago Strle .....	74
<b>B7. A Delayed Synchronizer in High-Speed Memory Applications</b>	
Sanghun Jung and Wonchan Kim .....	79
<b>B8. A Current-Mode Circuit for Euclidean Distance Calculation</b>	
Chuen-Yau Chen, Chun-Yueh Huang, Ju-Ying Tsao, and Bin-Da Liu .....	83

## SESSION C: Graphic Processors and Communications

<b>C1. Programmable Media &amp; Graphics Processors (Invited)</b>	
Le Trong Nguyen .....	87
<b>C2. A Hardware-Efficient Architecture for 3-D Graphics Processor</b>	
Bor-Sung Liang, You-Cheng Nieh, Yih-Pwu Niou, Chein-Wei Jen, and Gene Chuang* .....	88
<b>C3. A High-Performance Video Format Conversin System for MPEG-4</b>	
Kuan-Tsang Wang and Oscar T.-C. Chen .....	93
<b>C4. A Parallel VLSI Architecture for the LZW Data Compression Algorithm</b>	
Ming-Bo Lin .....	98
<b>C5. ARC: An ATM Routing and Concentration Chip</b>	
H. Jonathan Chao and Necdet Uzun .....	102
<b>C6. NETDTIC: A Single Fully Digital Chip Trunk Interface Circuit with Interrupt Pin and an Optional E&amp;M Channel Feature</b>	
Hakan Sakman .....	108
<b>C7. Bit-Serial Systolic Array Implementations of Euclid Algorithm for Inversion and Division in GF(2<sup>m</sup>)</b>	
Jyh-Huei Guo and Chin-Liang Wang .....	113

## SESSION D: Advanced Devices (I).

<b>D1. Status and Trends in SOI CMOS technology (Invited)</b>	
J.-P. Colinge .....	118
<b>D2. Extraction of LOCOS Edge Defect Information in SOI/MOSFETs</b>	
Yujun Li and T.P. Ma .....	123
<b>D3. High Performance Gate-All-Around TFT (GAT) for High-Density, Low-Voltage-Operation, and Low-Power SRAMs</b>	
S. Miyamoto, S. Maegawa, S. Maeda, T. Ipposhi, H. Kuriyama, and T. Nishimura .....	128
<b>D4. A Shall-Trench Isolation Study for 0.18 <math>\mu</math> m CMOS Technology with Emphasis on the Effects of Well Design, Channel Stop Implants, Trench Depth, and Salicide Process</b>	
S. Murtaza, A. Chatterjee, P. Mei, A. Amerasekara, P. Nicollian, T. Breedijk, M. Hanratty, S. Nag, I. Ali, and I.-C. Chen .....	133
<b>D5. Design Rule Related Defect Formation</b>	
Y. F. Hsieh and B.Y. Tsui* .....	138



<b>D6. Effects of Hydrogen Annealing on Data Retention Time for High Density DRAMs</b>	
L.C. Hsia, Thomas Chang, S.J. Chang, D. Fan, H.Y. Wei, and Jack Jan	142
<b>D7. Possibility of MMIC on Si: The Lossy Substrate Issue</b>	
A. Chin, D. Prinslow, V. Tsai, G. Nasserbakht, and B. Eklund	148

## SESSION L

<b>L1. Computer Chess, Then and Now : The Deep Blue Saga</b>	
Feng-hsiung Hsu	153

## SESSION E: Advanced Dielectrics

<b>E1. Integrated Ferroelectric Technology for Nonvolatile Memory (Invited)</b>	
Tatsumi Sumi	157
<b>E2. Enhanced Hot Carrier Effects in Scaled Flash Memory Devices</b>	
C. Chen, Z. Liu, and T.P. Ma	162
<b>E3. A Comparative pMOS study of 33 Nitrided Oxides Prepared by either N<sub>2</sub>O or Nitrogen Implant before Gate Oxidation for 0.18-0.13um CMOS Technologies</b>	
J.C. Hu, J. Kuehne, T. Grider, M. Rodder, and I.-C. Chen	167
<b>E4. Ultra-Thin Nitride/Oxide Stack Dielectric Produced by in-situ Jet Vapor Deposition</b>	
Y. Shi, X.W. Wang, T.P. Ma, G.J. Cui*, T. Tamagawa*, B.L. Halpern*, and J.J. Schmitt*	172
<b>E5. Ultra-thin Oxide with Atomically Smooth Interfaces</b>	
A. Chin, R.H. Kao, W.J. Chen*, B.C. Lin, T. Chang, C. Tsai, and J.C.-M. Huang**	177
<b>E6. Impact of Boron Penetration on Gate Oxide Reliability and Device Lifetime in p+-poly PMOSFETs</b>	
B.Y. Kim, I.M. Liu, H.F. Luan, M. Gardner*, J. Fulford*, and D.L. Kwong	182
<b>E7. The Effects of Passivation and Post-Passivation Anneal on the Integrity of Thin Gate Oxides</b>	
Carol Gelatos, Hsing-Huang Tseng, Stanley Filipiak, David Sieloff, Jack Grant, Philip Tobin and Randy Cotton	188
<b>E8. The Use of Jet-Vapor Deposited Silicon Nitride for Scaled DRAM Applications</b>	
X. Guo, X.W. Wang, and T.P. Ma, G.J. Cui*, T. Tamagawa*, B.L. Halpern*, and J.J. Schmitt*	193

## SESSION F: Advanced Microprocessors

<b>F1. Details in the Design of GHz Microprocessors (Invited)</b>	
Ray Stephany	198
<b>F2. A 550 MHz Alpha Microprocessor Targeted at PC Applications</b>	
Soichi Kobayashi, Yuichi Saito, Fumihiko Terayama, Tatsuya Ueda, Keiichi Higashitani, and Anil Jain*	203
<b>F3. A 15Kb 1.5 ns Access On-chip Tag SRAM</b>	
P.-F. Lu, S.P. Kowalczyk, A.P. Pelella, W.V. Huott, U. Bakhru, J. Rawlins, P. Patel, Y.H. Chan, and K.A. Jenkins	208
<b>F4. A Cost -Effective Fixed/Floating-Point Digital Signal Processor</b>	
Kai-Ming Tsou, Oscar T. -C. Chen, and Chou-Yeu Hu	213
<b>F5. SMPC: A RDBMS Microprocessor Containing Multi-Processor on a Chip</b>	
Yonghwan Lee, Wookyeong Jeong, Yongsurk Lee, and Surkhan Yoon*	217

<b>F6. Implementation of a Radix-4 SRT Divider/Square-root Supporting Two Concurrent Division/ Square-root Operations</b>	
Hokyung Kwon, Taeyoung Lee, Yonghwan Lee, and Yongsurk Lee .....	223
<b>F7. VLSI Implementation of a High-Throughput CORDIC Processor for Both Angle Calculation and Vector Rotation</b>	
Shen-Fu Hsiao and Jen-Ying Chen .....	227

## SESSION G: Technology Computer-Aided Designs

<b>G1. Predictive Simulation for Nanoscale Silicon Technology (Invited)</b>	
M. Pinto, M. Alam, J. Bude, Rafferty H.-H. Vuong .....	232
<b>G2. Predictive and Efficient Modeling of Substrate Currents in N-channel MOS-Transistors</b>	
B. Meinerzhagen, C. Jungemann*, S. Decker, S. Keith, S. Yamaguchi*, H. Goto* .....	233
<b>G3. Model and Solution of Reverse Short Channel Effect</b>	
Bing-Yue Tsui, Chih-Chiang Wang, Tzung-Zu Yang, Shyang Hwang-Leu, Geeng-Lih Lin, and Shyh-Chyi Wong .....	237
<b>G4. Design Strategy of MLSCR Devices for Submicron CMOS Technology</b>	
T. C. Lu, J. C. Guo, M. T. Wang and F. Shone .....	241
<b>G5. AC Charge Centroid Model for Quantization of Inversion Layer in n-MOSFET</b>	
Ya-Chin King, Hiroshi Fujioka*, Shi-roo Kamohara**, Wen-Chin Lee and Chenming Hu .....	245
<b>G6. A Complete Asymmetric Drain Current Model for Post-Stress Submicron pMOSFET</b>	
Young-Shying Chen and Sheng-Lyang Jang .....	250
<b>G7. A Behavioral Modeling Approach for 0.25um Dual-Gate MOSFET Design Optimization</b>	
Jiun-Jer Yang, Chih-Hsien Lin, Konrad Young, and Kuang-Yi Chiu .....	255

## SESSION H: Low-Voltage Low-Power Circuit Design

<b>H1. Noise Suppression in Low Voltage Differential I/O</b>	
Tord Haulin and Mats Hedberg .....	260
<b>H2. A Low-Power Low-Voltage Direct Digital Frequency Synthesizer</b>	
Shyuan Liao and Liang-Gee Chen .....	265
<b>H3. Low-Voltage Low-Power IF-Baseband Digital Down Converter</b>	
Shyh-Jye Jou, Tsan-I Hsu, and C.K. Wang .....	270
<b>H4. A 0.18um Hybrid Dual-threshold Library for High-Performance and Low-Power Processors</b>	
Uming Ko, Anthony Hill, Andrew Pua, and Pranjali Srivastava .....	275
<b>H5. 1.5V CMOS and BiCMOS Bootstrapper Dynamic Logic Circuits Suitable for Low-Voltage VLSI</b>	
J. H. Lou and J.B. Kuo .....	279
<b>H6. Low-Power High-Speed Complementary GaAs Dynamic Logic Circuit Design</b>	
Khaled Ali Shehata and Douglas J. Fouts .....	283
<b>H7. Dual-Mode Parasitic Bipolar Effect in Dynamic CVSL XOR Circuit with Floating Body Partially- Depleted SOI Devices</b>	
C. T. Chuang, P.F. Lu, J. Ji*, L.F. Wagner, S. Chu, and C.J. Anderson .....	288

## SESSION I: Advanced Devices(II)

<b>I 1. CMOS Technology for 1.8V and Beyond (Invited)</b>	
Jack Y.-C. Sun .....	293
<b>I 2. Modeling Short-Channel Effects of CMOSFET's Taking Account for Channel Engineering, Defect-enhanced-diffusion, and Gate Depletion</b>	
Bin Yu, Wen-Chin Lee, and Chenming Hu .....	298
<b>I 3. Optimization of Tilt-Implanted Punchthrough Stopper on Short-Channel Behavior in Quarter-micron MOSFET with Low-Concentration Wells</b>	
Chih-Hsien Lin, Jiunn-Jer Yang, Konrad Young, and K.-Y. Chiu .....	303
<b>I 4. An Extension of BSIM3 Model Incorporating Velocity Overshoot</b>	
Dennis Sinitsky, Fariborz Assaderaghi*, Michael Orshansky, Jeffrey Bokor, and Chenming Hu .....	307
<b>I 5. High-Performance Deep Submicron MOSTs with Polycrystalline-(Si,Ge) Gates</b>	
Y.V. Ponomarev, C. Salm*, J. Schmitz, P.H. Woerlee** and D.J. Gravesteijn .....	311
<b>I 6. Combination Effects of Nitrogen implantation at S/D Extension and N2O Oxide on 0.18um n-and p-MOSFETs</b>	
T.S. Chao, C.H. Chien*, S. K. Chiao, H.C. Lin, M.C. Liaw, L.P. Chen, T.Y. U.Huang**, T. F. Lei ** and C.Y. Chang** .....	316
<b>I 7. Hot Carrier Reliability Consideration for High Performance Submicron MOSFETs</b>	
Honda Huang, Jiunn-Jer Yang, Ta-Lee Yu, Konrad Young, and K.-Y. Chiu .....	321
<b>I 8. High-Energy Implanted BiCMOS (HEIBiC) Technology for Fabricating a 2-Ghz Services PCS Single Superchip</b>	
K.H. Lee, Y.F. Chyan, S. Chaudhry, Y. Ma, A.S. Chen, M.S. Carrol, W.J. Nagy, J.L.Becerro, and J.L. Lee .....	325

## SESSION J: Computer-Aided Design for VLSI

<b>J 1. TCAD Accomplishments and Challenges in VLSI (Invited)</b>	
Bhaskar Gadepalli .....	328
<b>J 2. Design for Signal Integrity: The New Paradigm for Deep-Submicron VLSI Design</b>	
Howard H. Chen and L.K. Wang .....	329
<b>J 3. SOI Low Power Model for Analog and Digital Circuits Calibrated using Virtual Wafer Fab.</b>	
J. C. Lai, J. Yue, and K.P. Beaudoin .....	334
<b>J 4. Simulation of Floating Body Effect in SOI Circuits Using BSIM3SOI</b>	
Robert Tu*, Dennis Sinitsky, Fari Assaderaghi**, Clement Wann**, and Chenming Hu .....	339
<b>J 5. Layout Verification for Submicron CMOS Cell Libraries to Improve ESD/Latchup Reliability</b>	
Ming-Dou Ker, Sue-Mei Hsiao, and Jiann-Horng Lin .....	343
<b>J 6. A Hierarchical Bridging Fault Extraction Approach for VLSI Circuit Layouts</b>	
Tzuhao Chen and Ibrahim N. Hajj .....	348
<b>J 7. Low-Power Testing for C-testable Iterative Logic Arrays</b>	
Shih-Arn Hwang and Cheng-Wen Wu .....	355
<b>J 8. BIST Testability Enhancement Using High Level Test Synthesis Techniques</b>	
Kowen Lai, Christos A. Papachristou, and Mikhail Baklashov .....	359

# The Transistor Anniversary

Ian M. Ross

President Emeritus

AT & T Bell Laboratories\*

## Setting the Course

In the summer of 1947, the forerunner of IEEE could have held a Symposium to commemorate the 50th anniversary of the discovery of the electron by J J Thomson. That event in 1897 could surely qualify as the start of the electronics discipline and the industry that followed. It was the new understanding of the properties of the electron that created the field of electronics, and that combined with our developing capability in the electrical, magnetic and mechanical arts, enabled a rich array of new products and services.

The Symposium would have been an upbeat event. Vacuum tube technology had fully matured with a wide range of tubes - diodes, pentodes, CRTs, klystrons and traveling wave tubes - in high volume manufacture. Vacuum tubes were the key component in an array of electronic equipment that seemed to meet all conceivable information needs.

The then Director of Research of Bell Telephone Laboratories might well have been invited to submit a paper to the Symposium. Mervin Kelly, who later became president of Bell Labs, would also have been upbeat. Electromechanical relay technology had provided fully automatic telephone dialing and switching. Microwave radio provided high quality telephone transmission across the continent. Again, available technology appeared capable of meeting the needs.

Yet Kelly would also have raised a word of caution. Although relays and vacuum tubes were apparently making all things possible in telephony, he had predicted for some years that the low speed of relays and the short life and high power consumption of tubes would eventually limit further progress in telephony and other electronic endeavors. He not only predicted the problem, he had already taken action to find a solution. In the summer of 1945, Kelly had established a research group at Bell Labs to focus on the understanding of semiconductors. It also had a long term goal of creating a solid-state device that might eventually replace the tube and the relay.

Kelly's vision triggered one of the most remarkable technical odysseys in the history of mankind, a journey

that has continued through 50 years. The semiconductor odyssey produced a revolution in our society at least as profound as the introduction of steel, of steam engines and the total industrial revolution. Electronics today pervades our lives and impacts everything we do whether at work or at home.

My purpose in this paper is to discuss the events that led to the invention of the transistor plus the hurdles that had to be overcome and the breakthroughs that were needed to make the semiconductor revolution a reality. In doing this I have tried to select those events that made 'the' difference rather than cover the multitude of contributions that made 'a' difference. I admit that there is some judgment in making this selection.

## The Scientific phase

By January of 1946 Kelly's semiconductor group was in place at Bell Labs under the leadership of William Shockley and Stanley Morgan. Bill Shockley was a very capable physicist, an analyst, and a man with a fascination for finding practical applications of science. Two key members of the team were John Bardeen and Walter Brattain. John Bardeen was a remarkably talented theoretical physicist as evidenced by the fact that he was awarded two Nobel prizes in physics each in a field of major significance. Walter Brattain was also an accomplished physicist with a flair for ingenious experiments. Other members included Gerald Pearson, Bert Moore, and Bob Gibney. The team was embedded in the unusually creative environment that existed in Bell Labs Murray Hill after World War II. As such they were able to seek the advice of resident experts in almost any relevant discipline.

The group had a number of other assets to call on in their pursuit of Kelly's goal. There existed a large body of empirical knowledge of semiconductor devices based on experience with diodes for detection of radio signals. These diodes ranged from the 'cat's whisker' crystal diodes at the heart of early radio receivers to the microwave diodes used in great quantities during the war for radio and radar detection. There was also considerable experience with power rectifiers such as copper oxide diodes. These devices were made from a variety of materials including selenium, lead sulfide (galena), copper oxide, germanium and silicon. All were

---

\* This is a shortened version of a paper scheduled for publication in the January 1998 issue of the Proceedings of the IEEE.

semiconductor materials, most were highly impure and none was single crystal. There was much art, much tinkering but little engineering understanding and almost no science.

There was already some basis for understanding the physics of semiconductor materials. The concepts of band gaps existed. Two types of conduction, already named n-type and p-type, had been identified in semiconductors, and attributed to the presence of certain impurities in very small concentrations. P-n junctions had been found within ingots formed by melting and re-freezing the purest silicon then commercially available. Their electrical and electro-optical characteristics had been explored. Considerable progress had already been made at Purdue University, Bell Labs, and elsewhere on producing semiconductor materials of increasing purity and on understanding their properties.

However, there was also much uncertainty, much still unknown. The highest purity semiconductor available - 99.8% - was characteristic of a soap advertisement, and orders of magnitude short of that eventually needed. Semiconductor materials were polycrystalline at best and frequently used in powder form. Single crystals of adequate perfection had yet to be grown. The key properties of these materials relevant for device applications had yet to be fully understood and evaluated.

Finally, there was a long, and persistent history of proposals for a solid state amplifier. Most were based on the so called field-effect mechanism. The concept was that an electric field applied through the surface of a semiconductor could modify the density of mobile charge in the body of the material and thereby change its conductivity. Typically the field was to be created by applying voltage to a metal plate close to but insulated from the base material. Modulating the voltage on the plate would modulate a current flow through the base material with the possibility of power gain. The first documented invention of this kind was made by Lilienfeld as early as 1925. All attempts to make such a device had however failed.

Both before and after the war, Shockley had studied and analyzed possible field-effect structures and had concluded that the effect should lead to amplification in achievable structures. Shockley's existence proof that amplification was theoretically possible in practical semiconductor materials provided major encouragement that the challenge undertaken by the Bell Labs group could indeed be accomplished.

By January 1946 two critical decisions had been made. The first was to focus the group's attention on crystals of silicon and germanium and ignore other more complex materials frequently used in prior investigations. It was recognized that silicon and germanium were stable elements that readily assumed the crystalline state, and therefore showed the best promise of being made into high purity, high perfection

single crystals. Such materials would permit the investigation to move forward on a sound scientific base. The second decision was to pursue the field-effect principle as the one having the most assurance of leading to a useful device.

Numerous attempts to demonstrate the field-effect in semiconductors had been made over the years and all had failed. Before the war, Shockley had participated in one such failure using a structure with a grid of metal filaments buried in the body of a semiconductor. Given the renewed focus, a number of new experiments were carried out by J R Haynes, H J McSkimin, W A Yager and R S Ohl in attempts to observe the field-effect. All gave negative results. Bardeen proposed that these experiments failed because the electric field was not penetrating the body of the semiconductor material but was terminated by immobile charges trapped in states at the semiconductor surface [1]. He calculated that a quite small number of such surface states, low compared to the density of surface atoms, would be adequate to shield the body from any measurable field-effect.

Bardeen and Brattain attempted to confirm this theory by experimenting with metal probes on the surface of germanium. The theory seemed to be correct. Thus for the first time there was some understanding of the persistent failure to observe the field-effect, and an opportunity to intervene. In the course of their work, they tried to modify the surface states with electrolytes surrounding the metal contacts to the germanium surface. Following a suggestion by Gibney [2], they found that applying voltage to the electrolyte created major changes in the current flow through a reverse biased contact. Brattain later replaced the electrolyte with an evaporated gold spot adjacent to the point contact. Finally, he replaced both contacts by an ingenious arrangement of two strips of gold foil separated by just a few mils and pressed onto the germanium surface. With one gold contact forward biased and the other reverse biased he observed power gain. The transistor effect had been discovered [3]. This was on December 16, 1947 a mere two and a half years after the formation of the Shockley group!

On Christmas Eve of 1947, the transistor action was demonstrated by Brattain and Moore for the top management of Bell Labs. This time the device was operated as an oscillator, an acid test of the existence of power gain. The announcement of the transistor discovery was, however, delayed until June 1948. This six month period was used to gain more understanding of the device and its possible applications and to obtain an adequate patent position.

The above is an abbreviated account of the events that led to the invention of the transistor. I believe it to be essentially correct. It is consistent with a memorandum written in December 1949 by W S Gorton, an assistant to the Director of Research of Bell Labs [4]. Gorton had been asked by his management, "while the memories were reasonably clear, to write an account of the

thinking, work, and events which resulted in the transistor". Gorton's memorandum is probably the most authentic summary in existence. In preparing his account, Gorton addressed the question of giving full credit to all who had contributed. Gorton's memorandum includes the names of twelve people who had taken a substantial part in the work. Those names all appear in the foregoing account.

With the invention of the point contact transistor -the gold foil having been replaced by two closely spaced point contacts - and with the demonstration of transistor action, the door had been opened to a whole new era of electronics. But the process of inventing the transistor still had a long way to go! Transistor action had been observed but no one understood just what was the mechanism. Was it a surface effect or was the action occurring in the semiconductor body? Ironically, the mechanism certainly was not the field-effect that had helped guide the whole effort.

Bardeen and Brattain leaned in the direction of a surface effect and continued experiments on that basis. Shockley, however, had recognized the role of minority carriers and by late January of 1948 he had completed a thorough formulation of p-n junction theory and the role played by the injection of minority carriers in forward bias and their collection in reverse bias. His analysis concluded with the invention of a junction transistor, a sandwich of lightly doped n-type material between two regions of p-type - or the other way around. With one p-n junction forward biased and the other reverse biased, minority carriers would be injected from the forward biased junction into the n-type material. They could then diffuse across the n-type region and, if it were thin enough, a large fraction would be collected at the reverse junction. Thus current generated in a low impedance circuit, the emitter, would create a similar current flow in a high impedance circuit, the collector, and power gain would result [5]. But this so far was just theory.

One month later, in February of 1948, John Shive carried out a critical experiment [6]. He applied two phosphor-bronze contacts to the opposite sides of a 0.01 cm thick slice of germanium. With this arrangement he observed transistor action from one contact to the other with substantial power gain. The length of the surface path around the semiconductor slice effectively ruled out a surface effect. The action had to take place through the semiconductor body. The behavior he observed was nicely explained by Shockley's recently developed theory of the junction transistor. Thus, while the point contact transistor may have exhibited some surface effects, bulk propagation was also surely taking place and was probably the dominant effect.

The next major advance was made in 1948. G K Teal and J B Little succeeded in growing a single crystal of germanium by slowly pulling a seed crystal from a melt of high purity germanium [7]. Using such material it was at last possible to detect and characterize minority

carriers injected by metal contacts into filaments of germanium. Various elegant experiments by Haynes, Pearson, Suhl and Shockley confirmed the behavior of both types of minority carriers and yielded measurements on injection efficiency, mobility, diffusion coefficients and lifetime [8]. These results showed that useful devices could be made according to Shockley's junction transistor theory. All that remained was to make one.

That required further refinement of the techniques of crystal growth and particularly of the controlled doping of the crystals during growth. In April 1950 a team of Shockley, Sparks and Teal succeeded in growing a crystal containing a thin region of p-type embedded in n-type material. The crystal was cut into n-p-n rods and contacts applied. The electrical properties of the resulting devices were largely consistent with the Shockley theory [9]. Transistor electronics now had a solid foundation.

There was one other event that completed this phase of the transistor saga. That was the publication in 1950 of Shockley's book "Electrons and Holes in Semiconductors" [10]. This was an exquisite account of the current understanding of semiconductors and transistors. It makes enlightening reading today after almost 50 years. In the 50s it provided an excellent means, and almost the only means, for scientists and engineers to get up to speed on a rapidly developing technology. It was required reading for those entering the business in its early days and, particularly so if you found yourself reporting to its author, as I did in March of 1952.

So in a period of only 5 years from the establishment of the semiconductor group at Bell Labs, the invention of the transistor was essentially complete, understood and documented. The scientific phase was coming to an end. The next phase would focus on solving development and engineering issues so that a brilliant invention could be converted into an important innovation.

### **The Development and Engineering Phase**

Having invented the transistor, the challenge was then to find ways to design a product that could be manufactured, and that could sustain a market. This phase took the industry approximately 8 years during which many challenging problems were addressed and solved. Whereas the scientific phase had been dominated by Bell Labs, there were now other companies in the business, and they also made major innovations.

What follows is an attempt to select and describe some of the major hurdles that had to be overcome and the major breakthroughs that were made. There are many events that made 'a' difference. I will focus here on those that made 'the' difference.

#### *The early manufacturing problems*



In early 1951 there were two transistor structures that were proven to work, but neither of them was suitable for large scale manufacture. The point contact transistor had all the frailties of its cat's whisker heritage. It was difficult to make, its electrical characteristics were far from ideal, very variable, hard to control, and inherently unstable. Point contact transistors were, nevertheless, manufactured for 10 years, but were never popular with the manufacturing engineer nor with the circuit designer.

The junction transistor, on the other hand, had predictable and more desirable electrical characteristics. It was, however, prodigal in its use of precious semiconductor material and required tricky contacting techniques not conducive to automation.

The grown junction transistor was manufactured starting in 1952. In the same year, J E Saby at General Electric announced the development of the alloy junction transistor [11]. The original version was made by alloying dots of indium, an acceptor material, on opposite sides of thin slices of n-type germanium. The starting point was the growth of uniformly doped crystals that were relatively easy to produce. Slices were cut from the crystal most of which could be used. Arrays of indium dots could be positioned in jigs on either side of the slices and, after alloying, the slice could be diced to yield a great many individual transistors. Contacts were easy to apply. The alloy transistor had well behaved performance characteristics, made efficient use of semiconductor material and could be manufactured with some degree of batch processing and automation. The alloy device was the first transistor to be readily manufactured, and for some years was the mainstay of the industry. One drawback was that precise control of dimensions and alloying temperatures were required to create thin enough base layers for high frequency performance.

#### *The quest for silicon*

It was understood from the beginning that, silicon would be a better transistor material than germanium for most applications. This mainly resulted from the higher energy gap of silicon - 1.1 eV compared to 0.67 eV for germanium. In germanium at room temperature the thermal generation of minority carriers led to substantial reverse currents in p-n junctions. The reverse current in silicon was orders of magnitude smaller and made a much superior rectifier.

The most serious problem with silicon was that critical chemical and metallurgical processes all took place at substantially higher temperatures. For example, the melting point of silicon was 1415 C compared to 937C for germanium. Silicon was also more chemically reactive than germanium. For example, silicon would react with the quartz crucibles that were used to contain germanium during crystal growth and purification by zone refining.

The critical breakthrough came in 1953 with the development by Theuerer of the floating zone method

[12]. He was able, in a vertical rod of silicon, to create a zone of molten material contained only by surface tension. Thus the zone refining technique could be used for silicon and resulted in crystals of purity comparable to the best obtained in germanium.

In 1954, Gordon Teal, now at TI, made the first silicon transistor using the grown junction method [13]. All the pieces were then in place for silicon devices to assume a major role.

#### *The Bob Wallace revelation*

Having overcome the hurdle of being able to make transistors with some degree of reproducibility, a major goal was to replace the vacuum tube in as many applications as possible. This was not as simple as it first appeared. Transistors were easiest to make in small sizes which inherently led to limited power handling capability. High frequency response called for smaller not larger devices. In seeking higher power at higher frequencies we seemed to be bucking nature.

One day I was in a small meeting at Bell Labs with a colleague named Bob Wallace. In the meeting on that day we were, as was frequently the case, discussing our problems in emulating the vacuum tube. Bob suddenly said "Gentlemen, you've got it all wrong! The advantage of the transistor is that it is inherently a small size and low power device. This means that you can pack a large number of them in a small space without excessive heat generation and achieve low propagation delays. And that's what we need for logic applications. The significance of the transistor is not that it can replace the tube but that it can do things that the vacuum tube could never do!" And this was a revelation to us all. We realized that in chasing the vacuum tube we had the wrong emphasis.

I am sure that the same idea occurred independently to other people in other organizations at about that time. The net result was that the semiconductor community began to relax about replacing the tube and focused on developing the transistor in its own right.

There is a lesson in this story. Having the clear goal of an application for an invention is a powerful stimulus for innovation. But frequently the original application turns out not to be the most important application.

#### *The speed problem - controlling the depth dimension*

The fundamental determinant of the frequency response of a junction transistor was the transit time of minority carriers across the base region, and therefore the thickness of the base layer. In practice alloy transistors were manufactured with bases as thin as 10 $\mu$ , yielding a frequency response approaching 10 MHz. Although this was quite a feat of manufacturing engineering, performance up to a few gigahertz was needed to support a full range of electronic applications.

The base width problem was solved by using the process of diffusion of donors and acceptors into the

semiconductor surface, which eventually yielded precise control of the depths of diffused layers in the range from  $20\mu$  to a fraction of a micron.

In 1954, C A Lee made first the germanium diffused transistor [14]. He diffused a base layer of arsenic to a depth of  $1.5\mu\text{m}$ , created an emitter region, by alloying aluminum to a depth of  $0.5\mu\text{m}$ , producing base thickness was about  $1.0\mu$ . This first diffused p-n-p transistor had a cutoff frequency of 500 MHz. A year later the first diffused silicon transistor was made and had a frequency cutoff at 120 MHz [15].

The speed problem was almost solved - but not quite. The frequency limitation had moved from the base region to the collector region. The collector had the highest resistivity of the three regions - an inevitable result of the additive nature of the diffusion process. This led to significant series resistance in the collector and that, combined with the capacitance of the collector junction, limited the frequency response.

The eventual solution was to add a totally different process, that of the epitaxial growth of a lightly doped layer of single crystal semiconductor on a substrate of a heavily doped single crystal - a process called epitaxial growth. A transistor base and emitter layer was then diffused into the epitaxial layer. The results were published in June 1960 by Theuerer, Kleimack, Loar, and Christensen [16].

#### *Oxide masking and photolithography - controlling the surface dimensions*

In 1955 C J Frosch and L Derick made a very important observation. They had been studying the pitting of the surface of silicon wafers during the diffusion process, and its dependence on the presence of oxygen. They further discovered that a few thousand angstrom layer of silicon dioxide grown on the surface prior to diffusion could mask the diffusion of certain donor and acceptor atoms into the silicon. They also demonstrated that diffusion would occur unimpeded through windows etched in the oxide layer [17]. Somewhat later, J Andrus and W L Bond showed that certain photoresists deposited on the oxide surface would prevent etching of the oxide [18]. Hence optical exposure of the resist by projection or contact masks could be used to create precise window patterns in the oxide and in turn provide precise control of areas in which diffusion would occur.

Thus four people in the course of a few weeks had invented the complete process of oxide masking of diffusion and the application of photolithography to the precise control of the geometry of diffused regions. This was a natural batch process that has since been developed to the point that junction areas can be controlled to a fraction of a micron. This complements the precision of the depth control of junctions diffused into the silicon surface providing the means to control the fabrication of silicon devices in three dimensions to the precision of a fraction of a micron.

It also ended the role of Ge as a major player. No material was found that would provide diffusion masking for germanium. Germanium became the niche material for specialty devices that rely critically on some special property.

#### *The reliability problem*

It was found in the early days that the transistor was very sensitive to its environment and particularly to humidity. This lack of reliability was a huge setback and embarrassment to the semiconductor community. The transistor had been lauded as a device with no failure mechanisms, with nothing to wear out. Instead we had a severe reliability problem and one that took almost 20 years before there was a complete solution.

The immediate remedy was to hermetically seal the devices in packages using the metal to glass seals from vacuum tube technology. This was a further blow to the pride of the semiconductor engineer. The packaging art evolved using a variety of empirical procedures including vacuum baking, dry gas baking and gettering. It is remarkable that with these unscientific approaches, germanium transistors were eventually manufactured with failure rates less than 10 per billion operating hours.

There were also ongoing systematic studies to try and understand the problem and find a more fundamental solution. At Bell Labs, Brattain continued his experimental work on surface states as did Shive. M. M. Atalla had a group that studied the surface properties of silicon in the presence of a silicon dioxide layer. They speculated that growing an oxide layer under very clean and controlled circumstances on the surface of carefully cleaned silicon could lead to a reduced density of states at the silicon surface and might serve to protect the surface against further change. In 1959 they did confirm that the presence of an oxide layer could reduce the density of surface states to such a level that the field-effect could be observed. However they had difficulties gaining enough control of the process to get reproducible results. Nevertheless the concept that an oxide layer might provide a solution to the reliability problem was a major step forward [19].

The final breakthrough in the solution of the reliability problem came with an invention made by J A Hoerni at Fairchild in late 1957 or early 1958. His idea was later reduced to practice and published in 1960 [20]. Hoerni proposed that, in the course of fabricating diffused silicon transistors, the silicon dioxide layer that was used as a diffusion mask be left in place. The junctions thus intersected the silicon surface under the oxide layer, and Hoerni speculated that that the oxide could protect the junction areas from contamination. He indeed found that such junctions had acceptable characteristics without further treatment. This was a startling result particularly for those who believed that a passivating oxide would need to be grown under meticulously clean conditions.

This was not the end of the story, but the Hoerni result put us on the right track. It was later found that not all 'diffusion' oxides gave adequate initial performance and that all were subject to degradation with time. It was not until about 1966 that techniques were developed to produce satisfactory oxide layers and to 'overcoat' them to retain their properties. Silicon devices then only needed to be further encapsulated in plastic for protection against gross environmental effects. Transistors, after all of 20 years, no longer looked like small vacuum tubes.

#### *The planar transistor*

In his 1960 paper, J A Hoerni also described the planar transistor. In this concept both the base and emitter regions were diffused through windows in silicon dioxide masks so that both collector and emitter junctions terminated at the surface. The masking oxides were left in place and provided protection and eventually passivation of the silicon surface. Ohmic contact was made to both emitter and base regions through windows in the oxide layer. It was noted that connection to the collector region could also be made on the top surface if that were desirable. The metal used for all contacts was aluminum which Moore and Noyce had previously shown would make good contact to either n or p-type silicon [21]. Moore had also shown that the aluminum could be extended over the oxide to form larger pads to ease connections to the chip. Somewhat later the epitaxial process was added to the planar transistor to minimize collector resistance.

This structure brought it all together. All the key development and engineering problems were either solved or on course for an elegant solution. There was a sound foundation for the long term manufacture of semiconductor devices. Silicon, the semiconductor of choice, could be produced with the crystalline perfection and purity more than adequate to the task. Critical dimensions in all three directions could if necessary be controlled to a fraction of a micron. Electrical contacts could be made with a single metal and without the need for microscopic precision. The resulting devices would eventually be solidly reliable. And all this could be done with batch processing with the promise of high yield and low unit cost.

Some 13 years after its discovery the transistor now had a sound engineering foundation. This provided the base for the next giant step. The integrated circuit was invented in 1958 by J S Kilby at TI [22] with a major added contribution from R N Noyce at Fairchild [23].

#### *The Integrated circuit*

The problem the integrated circuit was designed to solve had been vexing the semiconductor community for a number of years. Given the transistor's inherent small size, low power dissipation and potential for high reliability it had long been appreciated that the transistor should make it possible to build systems with thousands of active devices working together and operating at high speed. There were pressing

applications for such systems in computers, telephone switches and in several military projects.

It was Kilby In 1958 who first demonstrated that it was possible to produce transistors, diodes, capacitors and resistors in one piece of semiconductor and interconnect them to create functioning circuits. His early circuits had about ten components. Kilby used wire bonding to interconnect the components within the chip. This would have made manufacturing very difficult and surely would have limited the number of components per chip. Kilby recognized this problem. In his patent he suggested that suitable contacts could be made by deposition of a metal over a previously deposited layer of silicon dioxide. Later that year, and independent of the Kilby suggestion, Noyce proposed to replace the wires with the batch deposition of aluminum on a planar structure. As a consequence, Kilby and Noyce are jointly recognized as the inventors of the IC.

There was at the time a surprising degree of reluctance in the industry to pursue the IC approach. There had been considerable prior speculation about the benefits of fabricating several components on a single chip. There were several objections to the idea, the most serious of which was the expectation of very low yields and reliability. It was argued that if a single transistor could be made at only a 20% yield, which was an acceptable yield for many years, or even at 90% yield, which was considered to be excellent for many years, the yield of a chip containing 100 to 1000 transistors would be minuscule. It was similarly argued that the reliability of a chip would approximate the reliability of a discrete transistor degraded by the power of the number of transistors. These arguments carried great weight. They assumed of course that yields and failure rates were governed by random events which turned out not to be the case.

However, Kilby and Noyce by inventing and pursuing the IC concept, effectively settled the argument. It took hard work and several years to demonstrate that the feared problems hardly existed. As it turned out neither yield nor reliability was dominated by random events. This was really the consequence of the batch nature of silicon processing. In the case of yield, there tended to be large areas of a silicon slice in which the yield was effectively 100% while the yield in the remaining areas approached zero. Thus if the IC chip was small compared to the areas of 'good' material, the yield would be substantially independent of the size of the chip and the number of components on the chip.

The yield and reliability bugaboo was the only critical hurdle, the only 'make or break' issue, that had to be overcome to permit the IC to proceed on its incredible journey. All the needed transistor principles and processes were in place. From then on it took much ingenuity, much effort, and much investment to apply them and further refine them but no major transistor breakthroughs were needed.

#### *The major impact of Moore's law*