

international
**ELECTRON
DEVICES**
meeting

1995

WASHINGTON, DC
DECEMBER 10-13, 1995

David H. ...

Sponsored by Electron Devices Society of IEEE

iee
TECHNICAL DIGEST

001570

international
**ELECTRON
DEVICES**
meeting

1995

WASHINGTON, DC
DECEMBER 10-13, 1995

江苏工业学院图书馆
藏书章

ie
TECHNICAL DIGEST

WELCOME FROM THE GENERAL CHAIRMAN

The Conference Committee and I welcome you to the 1995 IEEE International Electron Devices Meeting. This year the conference returns to Washington, DC and continues a 41 year tradition as the premier forum for the presentation of the latest research and development in the area of electron devices and their application. The conference reflects the strong international nature of our industry with invited and plenary speakers from the major semiconductor centers around the world. Over 600 abstracts were submitted from 30 countries. The total number of accepted abstracts for this year was 221.

Two short courses are scheduled for Sunday. These are designed for broad appeal to IEDM participants including those unfamiliar with the topics. One course is entitled "Nonvolatile RAM Technology and Applications" and the other "Technologies for Portable Systems."

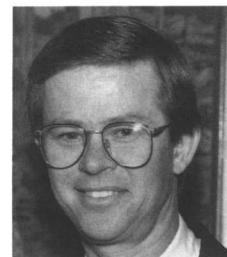
The Plenary talks on Monday feature speakers from Japan, U.S., and Europe, and span the topics of consumer electronics, smart power, and CMOS imaging.

An emerging technologies session, which was introduced last year, will highlight invited speakers discussing, among other topics, sensors in the food industry and power devices.

This year's luncheon speaker, Dr. Arati Prabhakar, Director of NIST, will deliver a presentation on industry-government technology partnerships and the role of congressional proposals to eliminate this aspect of America's science and technology infrastructure.

On Tuesday night, two panel sessions are planned, "Technology of the Future or Nano-Niche?" and "Flash or DRAM: Memory Choice for the Future?"

On behalf of the IEEE Electron Devices Society, which sponsors the IEDM, Steve Hillenius, Technical Program Chairman and Ken Galloway, Technical Program Vice Chairman, I wish to express my sincere appreciation and congratulations to the members of the Conference Committee for the outstanding job they have done in planning and organizing the 1995 meeting. The authors are to be commended for their efforts in preparing and presenting the high-quality papers that form the foundation of this conference. It is with great pleasure that I extend a warm welcome to them and to all the attendees of the 1995 IEEE International Electron Devices Meeting.



Rick Sivan
General Chairman



Steve Hillenius
Technical Program
Chairman



Ken Galloway
Technical Program
Vice Chairman

001570



AWARD PRESENTATIONS

PLENARY SESSION Monday, December 11

1994 ROGER A. HAKEN BEST STUDENT PAPER AWARD:

To: Julie Sheridan
Stanford University, Stanford, CA

For the paper entitled: "Direct Measurement of Transit Time Effects in Short-Channel MODFETs"

PAUL RAPPAPORT AWARD

To: Kazuo Yano, Tomoyuki Ishii, Takashi Hashimoto, Takashi Kobayashi, Fumio Murai and Koichi Seki
Hitachi Central Research Laboratory, Tokyo, Japan

For the paper entitled: "Room-Temperature, Single-Electron Memory"

EDS DISTINGUISHED SERVICE AWARD

To: Lewis M. Terman
IBM, T.J. Watson Research Center, Yorktown Heights, NY
"To recognize and honor outstanding service to the Electron Devices Society"

J. J. EBERS AWARD

To: Martin A. Green
University of New South Wales, Sydney, Australia
"For outstanding technical contributions to electron devices"

IEDM LUNCHEON Tuesday, December 12

1995 IEEE CLEDO BRUNETTI AWARD

To: Henry I. Smith (F'IEEE), Joseph F. and Nancy P. Keithley
Massachusetts Institute of Technology, Cambridge, MA
"For contributions to microfabrication science and technology, notably microlithography"

1995 IEEE JACK A. MORTON AWARD

To: Yoshio Nishi (F'IEEE)
Texas Instruments, Dallas, TX
"For contributions to the basic understanding and innovative development of MOS device technology"

1995 IEEE DAVID SARNOFF AWARD

To: Karl Hess (F'IEEE)
Beckman Institute, University of Illinois, Urbana, IL
"For contributions to high field transport and real space transfer effects in semiconductor heterolayer structures"

CONFERENCE HIGHLIGHTS

<u>Date</u>	<u>Time</u>	<u>Place</u>	<u>Event</u>
12/10	9:00 a.m. - 5:30 p.m.	Int'l Ballroom East & West	Short Courses
12/11	9:00 a.m. - 12:00 p.m.	Int'l Ballroom Center	Plenary Session
12/11	1:00 p.m. - 3:10 p.m.	Lincoln Room	Emerging Technologies Session
12/11	6:00 p.m. - 7:00 p.m.	Int'l Ballroom Center	Reception
12/12	12:20 p.m. - 2:00 p.m.	Int'l Ballroom West	Luncheon
12/12	8:00 p.m. - 10:00 p.m.	Int'l Ballroom East & Center	Panel Sessions

LUNCHEON PRESENTATION

Increasing Role of Government Investment in Civilian Technology: A presentation by Dr. Arati Prabhakar, Director of National Institute of Standards and Technology

IEDM CONFERENCE COMMITTEE 001570

Rick Sivan, General Chairman
Motorola
Austin, TX

Steve Hillenius
Technical Program Chairman
AT&T Bell Laboratories
Murray Hill, NJ

Ken Galloway
Technical Program Vice Chairman
University of Arizona
Tucson, AZ

Isik Kizilyalli
Publications Chairman
AT&T Bell Laboratories
Orlando, FL

Masafumi Kimata
Asian Arrangements Co-Chairman
Mitsubishi Electric Corp.
Hyogo, Japan

Shuji Ikeda
Asian Arrangements Co-Chairman
Hitachi
Tokyo, Japan

Pierre Woerlee
European Arrangements Co-Chairman
Philips Research Laboratory
Eindhoven, The Netherlands

Enrico Sangiorgi
European Arrangements Co-Chairman
University of Udine
Udine, Italy

Bijan Davari
Short Course Chairman
IBM, TJ Watson Research Center
Yorktown Heights, NY

Jesus del Alamo
Short Course Vice Chairman
Massachusetts Institute of Technology
Cambridge, MA

Genda Hu
Publicity Chairman
Information Storage Devices
San Jose, CA

Gary Bronner
Publicity Vice Chairman
IBM
Hopewell Junction, NY

Henry Baltes
Emerging Technologies Chairman
ETH Hoenggerberg
Zurich, Switzerland

Michael Gaitan
Treasurer
NIST
Gaithersburg, MD

Melissa Widerkehr
Phyllis Mahoney
Conference Managers
Widerkehr and Associates
Gaithersburg, MD



1995 Conference and Program Committee

Seated from left to right: Genda Hu, Publicity Chairman; Michael Brassington, Subcommittee Chairman, Integrated Circuits; Steve Hillenius, Technical Program Chairman; Rick Sivan, General Chairman; Ken Galloway, Technical Program Vice Chairman; Henry Baltes, Emerging Technologies Chairman; Lalita Manchanda, Subcommittee Chairman, Device Interconnect Technology. *First Row standing from left to right:* Phyllis Mahoney, Conference Manager; Stephen Chou, Subcommittee Chairman, Quantum Electronics and Compound Semiconductor Devices; Shuji Ikeda, Asian Arrangements Co-Chairman; Enrico Sangiorgi, European Arrangements Co-Chairman; Isik Kizilyalli, Publications Chairman; Masafumi Kimata, Asian Arrangements Co-Chairman; Gary Bronner, Publicity Vice Chairman; Bijan Davari, Short Course Chairman; Melissa Widerkehr, Conference Manager. *Second Row standing from left to right:* Wes Lawson, Subcommittee Chairman, Vacuum Electronics; Judy Hoyt, Subcommittee Chairman, Solid State Devices; Mark Law, Subcommittee Chairman, Modeling and Simulation; Pierre Woerlee, European Arrangements Co-Chairman; Denice Denton, Subcommittee Chairman, Detectors, Sensors and Displays; Hee-Gook Lee, Subcommittee Chairman, CMOS Devices and Reliability.

SUBCOMMITTEE ON CMOS DEVICES AND RELIABILITY

Hee-Gook Lee, *Chairman*
LG Semicon, Co. Ltd.
ChoongChungBuk-Do, Korea

Shahriar Ahmed
Intel Corporation
Hillsboro, OR

Ih-Chin Chen
Texas Instruments
Dallas, TX

John Chen
Taiwan Semiconductor Mfg. Co.
Taiwan, Rep. of China

Mark Gardner
Advanced Micro Devices
Austin, TX

Jacques Gautier
CENG/LETI
Grenoble, France

Jim Hayden
Motorola
Austin, TX

Masakazu Kakumu
Toshiba Corporation
Kawasaki, Japan

Jack Lee
University of Texas
Austin, TX

Bruno Ricco
University of Bologna
Bologna, Italy

Jack Y.-C. Sun
IBM Corporation
Hopewell Junction, NY

Eiji Takeda
Hitachi, Ltd.
Tokyo, Japan

Werner Weber
Siemens AG
Munich, Germany

Jason Woo
University of California
Los Angeles, CA

SUBCOMMITTEE ON DEVICE INTERCONNECT TECHNOLOGY

Lalita Manchanda, *Chairman*
AT&T Bell Laboratories
Holmdel, NJ

Sung Tae Ahn
Samsung Electronics Co., Ltd.
Kyungki-Do, Korea

Pierre Fazan
Micron Technology
Boise, ID

Carole Graas
Texas Instruments, Inc.
Dallas, TX

Michel Haond
CNET, France
Meylan Cedex, France

Seiichiro Kawamura
Fujitsu
Kawasaki-City, Japan

Takamoro Kikkawa
NEC Corporation
Sagamihara City, Japan

John Lowell
Advanced Micro Devices
Austin, TX

Karen Maex
IMEC
Leuven, Belgium

Mehrdad Moslehi
CVC Products, Inc.
Fremont, CA

S.C. Sun
National Chiao Tung University
Taiwan, Rep. of China

Shih-Wei Sun
United Microelectronics Corp.
Taiwan, Rep. of China

David Thomas
IBM Microelectronics
Essex Junction, VT

P.K. Vasudev
SEMATECH
Austin, TX

Simon Yang
Intel
Hillsboro, OR

SUBCOMMITTEE ON DETECTORS, SENSORS AND DISPLAYS

Denice Denton, *Chairman*
University of Wisconsin
Madison, WI

Savvas Chamberlain
DALSA, Inc.
Ontario, Canada

Anne Chiang
Xerox PARC
Palo Alto, CA

Leslie Field
Hewlett-Packard Laboratories
Palo Alto, CA

S. Gareth Ingram
GEC, Marconi Materials Technology
Hertfordshire, United Kingdom

Khalil Najafi
University of Michigan
Ann Arbor, MI

Arokia Nathan
University of Waterloo
Ontario, Canada

R. Popovic
Swiss Federal Institute of
Technology Lausanne
Lausanne, Switzerland

Nobukazu Teranishi
NEC Corporation
Kanagawa, Japan

A. Theuwsen
Philips Research Laboratories
Eindhoven, The Netherlands

Toshihisa Tsukada
Hitachi Ltd.
Tokyo, Japan

SUBCOMMITTEE ON INTEGRATED CIRCUITS

Michael Brassington, *Chairman*
Sun Microsystems
Mountain View, CA

Robert Bayruns
Anadigics
Warren, NJ

Larry Brigham
Intel Corporation
Hillsboro, OR

Sameer Haddad
Advanced Micro Devices
Sunnyvale, CA

Joel Hartman
CENG
Grenoble Cedex, France

Chang Gyu Hwang
Samsung
Kyungki-do, Korea

Tohru Mogami
NEC Corporation
Kanagawa, Japan

Andree Montree
Philips Research Laboratories
Eindhoven, The Netherlands

Seiichi Mori
Toshiba Corporation
Kawasaki, Japan

Lal Sood
Motorola
Austin, TX

Nobuo Tamba
Hitachi, Ltd.
Tokyo, Japan

Morgan Thoma
AT&T Bell Laboratories
Orlando, FL

Luan Tran
Micron Technology
Boise, ID

Kevin Yallup
National Semiconductor
Greenock, Scotland

SUBCOMMITTEE ON MODELING AND SIMULATION

Mark Law, *Chairman*
University of Florida
Gainesville, FL

Mohammed Darwish
Siliconix, Inc.
Santa Clara, CA

Michael Duane
Advanced Micro Devices
Austin, TX

Martin Giles
Intel Corporation
Santa Clara, CA

Hiroshi Iwai
Toshiba Corporation
Kawasaki, Japan

D.B.M. Klaassen
Philips Research Laboratories
Eindhoven, The Netherlands

Jean-Pierre Leburton
University of Illinois
Urbana, IL

Hiroshi Matsumoto
NEC Corporation
Kanagawa, Japan

Chris Maziar
The University of Texas
Austin, TX

Luca Selmi
DEIS
Bologna, Italy

Kenji Taniguchi
Osaka University
Osaka, Japan

Franco Venturi
University of Parma
Parma, Italy

Zhiping Yu
Stanford University
Stanford, CA

Hong-Ha Vuong
AT&T Bell Laboratories
Murray Hill, NJ

SUBCOMMITTEE ON QUANTUM ELECTRONICS AND COMPOUND SEMICONDUCTOR DEVICES

Stephen Chou, *Chairman*
University of Minnesota
Minneapolis, MN

Ilesanmi Adesida
University of Illinois
Urbana, IL

April Brown
Georgia Institute of Technology
Atlanta, GA

Young-Kai Chen
AT&T Bell Laboratories
Murray Hill, NJ

Deborah Crawford
National Science Foundation
Arlington, VA

Juergen Dickman
Daimler-Benz
Ulm (Donau), Germany

Darral Hill
Texas Instruments
Dallas, TX

Tadao Ishibashi
NTT LSI Laboratories
Atsugi-shi, Japan

S.J. Prasad
Maxim
Beaverton, OR

Bardia Pezeshki
IBM, T.J. Watson Research
Yorktown Heights, NY

William Stanchina
Hughes Research Labs
Malibu, CA

Mike Strosio
Army Research Office
Research Triangle Park, NC

Gerald Witt
AFORSR/NE
Bolling AFB, DC

Enrico Zanoni
Universita di Padova
Padova, Italy

SUBCOMMITTEE ON SOLID STATE DEVICES

Judy Hoyt, *Chairman*
Stanford University
Stanford, CA

Emmerich Bertagnolli
Siemens AG
Munich, Germany

T. Paul Chow
Rensselaer Polytechnic Institute
Troy, NY

Ronald Dekker
Philips Research Laboratories
Eindhoven, The Netherlands

John Derov
Rome Laboratory
Hanscom AFB, MA

Taylor Efland
Texas Instruments
Dallas, TX

Robert Hadaway
Northern Telecom Ltd.
Ottawa, Canada

Ted Kamins
Hewlett-Packard Laboratories
Palo Alto, CA

Nobuo Sasaki
Fujitsu Laboratories, Ltd.
Kanagawa, Japan

Ayman Shibib
AT&T Bell Laboratories
Reading, PA

Robert Trew
Case Western Reserve University
Cleveland, OH

Hak-Yam Tsoi
Motorola
Mesa, AZ

Sophie Verdonckt-Vandebroek
Xerox WCR&T
Webster, NY

K.L. Wang
University of California
Los Angeles, CA

Kazuo Yano
Hitachi, Ltd.
Tokyo, Japan

SUBCOMMITTEE ON VACUUM ELECTRONICS

Wes Lawson, *Chairman*
University of Maryland
College Park, MD

Monica Blank
Naval Research Lab
Washington, DC

Jennifer Butler
Hughes Research Lab
Malibu, CA

Kwo Ray Chu
National Tsing Hua University
Hsinchu, Taiwan

Michael Fazio
Los Alamos National Laboratory
Los Alamos, NM

Kevin Felch
Varian Associates
Palo Alto, CA

Gary Groshart
Northrup Grumman Corp.
Rolling Meadow, IL

Thomas Hargreaves
Litton Systems EDD
San Carlos, CA

Roy Heppinstall
EEV
Chalmsford Essex, England

James Hickey
Teledyne MEC
Rancho Cordova, CA

Ken Kreischer
Massachusetts Institute of
Technology
Cambridge, MA

John Nation
Cornell University
Ithaca, NY

John Pasour
MRC
Newington, VA

Francis Payen
Thomson
Velizy Cedex, France

Manfred Thumm
Universitaet Karlsruhe
Karlsruhe, Germany

STUDENTS: Join EDS (Electron Devices Society)

Our society has been involved in the progress of electronics and electrical engineering over the past 100 years with research and development in devices and technology.

EDS AREAS OF INTEREST

- Compound Semiconductor Devices
- Displays and Imaging Devices
- High Frequency Devices
- Micromechanics
- Optical Devices
- Photovoltaics
- Quantum Effect Devices
- Solid-State Sensors and Actuators
- Solid-State Power Devices
- Tubes and Other Vacuum Devices

ADVANTAGES OF IEEE/EDS MEMBERSHIP

- Monthly EDL Letters
- Student Magazine (U.S. only)
- Reduced Rates
- IEEE Spectrum
- Student Branches
- Local Chapters
- Notice of Meetings
- Awards
- Membership Pin and Card
- Professional Involvement
- Distinguished Lecturers
- Student Paper Contest

REQUEST STUDENT MEMBERSHIP APPLICATION FROM:

Professor Marvin H. White
Membership Chairperson
Electron Devices Society
Lehigh University
Sherman Fairchild Laboratory, #161
Bethlehem, PA 18015

TABLE OF CONTENTS

PLENARY SESSION

Monday, December 11, 9:00 a.m.
International Ballroom Center

Invited Papers

Chairman: Steve Hillenius

- 1.1 **Consumer Electronics as the Technology Driver**, Yoshitaka Hashimoto, Sony Corporation, Tokyo, Japan 3
- 1.2 **Smart Power Technology and the Evolution from Protective Umbrella to Complete System**, Bruno Murari, SGS-Thomson Microelectronics, Cornaredo, Italy 9
- 1.3 **CMOS Image Sensors: Electronic Camera on a Chip**, Eric Fossum, NASA Jet Propulsion Laboratory, Pasadena, CA 17

Session 2: CMOS Devices and Reliability—Hot Carriers and Device Reliability

Monday, December 11, 1:00 p.m.
International Ballroom East

Co-Chairmen: Masakazu Kakumu, Toshiba
Werner Weber, Siemens

- 1:00 p.m.
Introduction
- 1:05 p.m.
- 2.1 **Statistical Variation of NMOSFET Hot-Carrier Lifetime and its Impact on Digital Circuit Reliability**, J. Chen, B. McGaughy and C. Hu, University of California, Berkeley, CA 29
- 1:30 p.m.
- 2.2 **Hot-Carrier-Induced Gate Capacitance Variation and Its Impact on DRAM Circuit Functionality**, Y. Huh, H. Lee, J. Ahn, D. Yang and Y. Sung*, LG Semicon Co., Ltd., Cheongju, Korea, *Korea University, Seoul, Korea 33
- 1:55 p.m.
- 2.3 **Oxide-Field Dependence of the NMOS Hot-Carrier Degradation Rate and Its Impact on AC-Lifetime Prediction**, S. Kim, B. Menberu, T. Kopley and J. Chung, Massachusetts Institute of Technology, Cambridge, MA 37
- 2:20 p.m.
- 2.4 **Accurate Measurements for Lateral Distribution of Interface Traps by Charge Pumping and Capacitance Methods**, H. Uchida, K. Fukuda, H. Tanaka and N. Hirashita, Oki Electric Industry Co., Ltd., Tokyo, Japan 41
- 2:45 p.m.
- 2.5 **LDD Charge Pumping - Direct Measurement of Interface States in the Overlap Region**, V. Prabhakar, T. Brozek, Y. Chan* and C. Viswanathan, University of California, Los Angeles, CA and *Sematech, Austin, TX 45
- 3:10 p.m.
- 2.6 **A Comparative Study of Hot-Carrier Induced Light Emission and Degradation in Bulk and SOI MOSFETs**, L. Selmi, M. Pavesi*, H. Wong**, A. Acovic** and E. Sangiorgi***, University of Bologna, Bologna, Italy, *University of Parma, Italy, **IBM, Yorktown Heights, NY, ***University of Udine, Italy 49

Session 3: Integrated Circuits - Low Voltage/Low Power CMOS

Monday, December 11, 1:00 p.m.
International Ballroom Center

Co-Chairmen: Morgan Thoma, AT&T Bell Laboratories
Luan Tran, Micron

- 1:00 p.m.
Introduction
- 1:05 p.m.
- 3.1 **Reducing Operating Voltage from 3.2, to 1 Volt and Below—Challenges and Guidelines for Possible Solutions (Invited Paper)**, R. Yan, D. Monroe*, J. Weis, A. Mujtaba and E. Westwick, AT&T Bell Labs, Holmdel, NJ and AT&T Bell Labs, Murray Hill, NJ 55
- 1:30 p.m.
- 3.2 **TFSOI CMOS Technology for Sub-1V Microcontroller Circuits**, W. Huang, K. Papworth, M. Racanelli, J. John, J. Foerstner, H. C. Shin, H. Park, B. Hwang, S. Cheng, T. Wetteroth, S. Hong, H. Shin and S. Wilson, Motorola, Inc., Mesa, AZ 59
- 1:55 p.m.
- 3.3 **Optimization of Quarter Micron MOSFETs For Low Voltage/Low Power Applications**, Z. Chen, J. Burr, J. Shott and J. Plummer, Stanford University, Stanford, CA 63
- 2:20 p.m.
- 3.4 **Intra-Die Device Parameter Variations and Their Impact on Digital CMOS Gates at Low Supply Voltages**, M. Eisele*, J. Berthold, R. Thewes, E. Wohlrab, D. Schmitt-Landsiedel, W. Weber, Siemens Corporate Research, Munich Germany, *Technical University of Munich/Siemens Corporation, Munich, Germany 67
- 2:45 p.m.
- 3.5 **Reversal of Temperature Dependence of Integrated Circuits Operating at Very Low Voltages**, C. Park, J. John, K. Klein, J. Teplik, J. Caravella, J. Whitfield, K. Papworth and S. Cheng, Motorola, Inc., Mesa, AZ 71
- 3:10
- 3.6 **Discussion Session: Power/Voltage: How Low is Low?**
- Session 4: Modeling and Simulation—Process Modeling** 75
- Monday, December 11, 1:00 p.m.
International Ballroom West
- Co-Chairmen: Martin Giles, Intel
Hong-Ha Vuong, AT&T
- 1:00 p.m.
Introduction
- 1:05 p.m.
- 4.1 **Ion Implantation and Transient Enhanced Diffusion (Invited Paper)**, J. Poate, D. Eaglesham, G. Gilmer, H. Gossmann, M. Jaraiz*, C. Rafferty and P. Stolk, AT&T Bell Laboratories, Murray Hill, NJ and *University de Valladolid, Valladolid, Spain 77
- 1:30 p.m.
- 4.2 **Modeling Arsenic Activation and Diffusion During Furnace and Rapid Thermal Annealing**, E. Vandenbossche, H. Jaouen and B. Baccus*, SGS-Thomson Microelectronics, Crolles, France and *IEMN-ISEN, Lille, France 81
- 1:55 p.m.
- 4.3 **Unified Model of Boron Diffusion in Thin Gate Oxides: Effects of F, H₂, N, Oxide Thickness and Injected Si Interstitials**, R. Fair, Duke University, Durham, NC 85
- 2:20 p.m.
- 4.4 **3D Modeling of Sputter and Reflow Processes for Interconnect Metals**, F. Baumann, G. Gilmer*, AT&T Bell Laboratories, Holmdel, NJ, *Murray Hill, NJ 89

- 2:45 p.m.
4.5 A Sputter Equipment Simulation System Including Molecular Dynamical Target Atom Scattering Model, H. Yamada, T. Shinmura and T. Ohta, NEC Corporation, Kanagawa, Japan 93
- 3:10 p.m.
4.6 Three Dimensional PVD Virtual Reactor for VLSI Metallization, D. Bang, J. McVittie, K. Saraswat, Z. Krivokapic*, J. Iacoponi* and J. Gray*, Stanford University, Stanford, CA and *Advanced Micro Devices, Sunnyvale, CA 97
- 3:35 p.m.
4.7 Physical Etching/Deposition Simulation with Collision-Free Boundary Movement, Z. Hsiau, E. Kan, J. McVittie and R. Dutton, Stanford University, Stanford, CA 101
- 4:00 p.m.
4.8 Simulation Approach for Achieving Configuration Independent Poly-Silicon Gate Etching, K. Harafuji, M. Ohkuni, M. Kubota, H. Nakagawa, A. Misaka, Matsushita Electric Ind., Co., Ltd., Osaka, Japan 105

Session 5: Device Interconnect Technology—Advanced Memory Dielectrics 109

Monday, December 11, 1:00 p.m.
Jefferson Room

Co-Chairmen: S.C. Sun, National Nano Device Laboratory
P. Fazan, Micron Technology

- 1:00 p.m.
Introduction
- 1:05 p.m.
5.1 Ta₂O₅ Capacitors' Dielectric Material for Giga-Bit DRAMs(Invited Paper), Y. Ohji, Y. Matsui, T. Itoga, M. Hirayama, Y. Sugawara, K. Torii, H. Miki, M. Nakata, I. Asano, S. Iijima and Y. Kawamoto, Hitachi, Ltd., Tokyo, Japan 111
- 1:30 p.m.
5.2 Novel Stacked Capacitor Technology for 1Gbit DRAMS with CVD-(Ba,Sr)TiO₃ Thin Films on a Thick Storage Node of Ru, A. Yuuki, M. Yamamuka, T. Makita, T. Horikawa, T. Shibano, N. Hirano, H. Maeda, N. Mikami, K. Ono, H. Ogata and H. Abe, Mitsubishi Electric Corporation, Hyogo, Japan 115
- 1:55 p.m.
5.3 An ECR MOCVD (Ba,Sr)TiO₃ Based Stacked Capacitor Technology with RuO₂/Ru/TiN/TiSi_x Storage Nodes for Gbit-Scale DRAMs, S. Yamamichi, P. Lesaichere, H. Yamaguchi*, K. Takemura*, S. Sone*, H. Yabuta*, K. Sato, T. Tamura, K. Nakajima, S. Ohnishi, K. Tokashiki, Y. Hayashi, Y. Kato*, Y. Miyasaka*, M. Yoshida* and H. Ono, NEC Corp., Kanagawa, Japan and *Kawasaki, Japan 119
- 2:20 p.m.
5.4 Effects of Scaling Thickness and Niobium Doping Level on Ferroelectric Thin Film Capacitor Memory Operation, F. Chai, R. Schrimpf, J. Brews, D. Birnie, III, K. Galloway, R. Vogt, and M. Orr, University of Arizona, Tucson, AZ 123
- 2:45 p.m.
5.5 Characteristics of the PZT Thin Film Device Fabricated on the Single Grain, J. Joo and S. Joo, Seoul National University, Seoul, Korea 127
- 3:10 p.m.
5.6 Discussion Session

Session 6: Emerging Technologies 131

Monday, December 11, 1:00 p.m.
Lincoln Room

Co-Chairman: Henry Baltes, ETH Zurich

- 1:00 p.m.
Introduction
- 1:05 p.m.
6.1 New Generation MOS Controlled Power Devices and Their Applications (Invited Paper), W. Fichtner and H. Dettmer, ETH Zurich, Zurich, Switzerland 133
- 1:55 p.m.
6.2 Integrated Inductors for Low Cost Electronic Packages (Invited Paper), M. Allen, Georgia Institute of Technology 137
- 2:45 p.m.
6.3 Electronic Sensing of the Taste of Beer and Other Foodstuffs (Invited Paper), K. Toko, Kyushu University, Fukuoka, Japan 143

Session 7: Detectors, Sensors and Displays—Image Sensors 149

Monday, December 11, 1:00 p.m.
Georgetown Room

Co-Chairmen: Savvas Chamberlain, DALSA, Inc.
Nobukazu Teranishi, NEC

- 1:00 p.m.
Introduction
- 1:05 p.m.
7.1 High Resolution Tri-Linear Colour TDI CCD Image Sensor with Programmable Responsivity Gain, S. Agwani, J. Miller, S. Chamberlain, and V. Washkurak, DALSA, Inc. Waterloo, Canada 151
- 1:30 p.m.
7.2 An mK x nK Modular Image Sensor Design, G. Kreider, J. Bosiers, B. Dillen, J. van der Heijden, W. Hoekstra, A. Kleimann, P. Opmeer, J. Oppers, H. Peek, R. Pellens and A. Theuwissen, Philips Imaging Technology, Eindhoven, The Netherlands 155
- 1:55 p.m.
7.3 Optical Limitation to Cell Size Reduction in IT-CCD Image Sensors, T. Satoh, N. Mutoh, M. Furumiya, I. Murakami, S. Suwazono, C. Ogawa, K. Hatano, H. Utsumi, S. Kawai, K. Arai, M. Morimoto, K. Orihara, T. Tamura, N. Teranishi and Y. Hokari, NEC Corporation, Kanagawa, Japan 159
- 2:20 p.m.
7.4 Metal Contamination Characterization in CCD Image Sensors, W. Toren and J. Bisschop, Philips Imaging Technology, Eindhoven, The Netherlands 163
- 2:45 p.m.
7.5 CCD-based Sensor Array for Magnetic Pattern Recognition, N. O and A. Nathan, University of Waterloo, Waterloo, Ontario, Canada 167
- 3:10 p.m.
7.6 A Fingerprint Opto-Detector Using Lateral Bipolar Phototransistors in a Standard CMOS Process, R. Sandage and J. Connelly, Georgia Institute of Technology, Atlanta, GA 171
- 3:35 p.m.
7.7 A Solid-State Imager Joined to an Avalanche Multiplier Film with Micro-bump Electrodes, J. Yamazaki, H. Maruyama, F. Andoh, K. Tanioka, S. Araki*, K. Tsuji** and T. Kawamura, NHK Science and Technical Research Laboratories, Tokyo, Japan and *Olympus Optical Co., Ltd and **Hitachi, Ltd. 175

Session 8: Quantum Electronics and Compound Semiconductor Devices—Advanced Field Effect Transistors

179

Monday, December 11, 1:00 p.m.

Monroe Room

Co-Chairmen: April Brown, Georgia Tech
Enrico Zanoni, University of Padova

1:00 p.m.

Introduction

1:05 p.m.

- 8.1 **11.5V-Operation GaAs Spike-Gate Power FET with 65% Power-Added Efficiency**, T. Tanaka, H. Furukawa, H. Takenaka, T. Ueda, A. Noma, T. Fukui, K. Tateoka and D. Ueda, Matsushita Electronics Corp., Osaka, Japan 181

1:30 p.m.

- 8.2 **1.2V Operation 1.1W Heterojunction FET for Portable Radio Applications**, K. Inosako, N. Iwata and M. Kuzuhara, NEC Corporation, Shiga, Japan 185

1:55 p.m.

- 8.3 **High-Efficiency Dual-Gate InGaAs Pseudomorphic HEMTs for High Power Amplifiers Using Single-Voltage Supply**, I. Ohbu, T. Tanimoto, S. Tanaka, H. Matsumoto, A. Terano, M. Kudo, and T. Nakamura, Hitachi Ltd., Tokyo, Japan 189

2:20 p.m.

- 8.4 **Ultra-High-Speed InAlAs/InGaAs HEMT ICs Using pn-Level-Shift Diodes**, T. Enoki, Y. Umeda, K. Osafune, H. Ito and Y. Ishii, NTT LSI Laboratories, Kanagawa, Japan 193

2:45 p.m.

- 8.5 **0.1- μ p⁺-GaAs Gate HJFETs with $f_t=121$ GHz Fabricated using All Dry-etching and Selective MOMB Growth**, S. Wada, N. Furuhashi, M. Tokushima, M. Fukaishi, H. Hida, T. Maeda, NEC Corporation, Ibaraki, Japan 197

3:10 p.m.

- 8.6 **A New Physical Model for the Kink Effect on InAlAs/InGaAs HEMTs**, M. Somerville, J. del Alamo and W. Hoke*, Massachusetts Institute of Technology, Cambridge, MA and *Raytheon Company, Lexington, MA 201

3:35 p.m.

- 8.7 **High-Transconductance GaN MODFETs**, O. Aktas, W. Kim, Z. Fan, F. Stengel, A. Botchkarev, A. Salvador, S. Mohammad, B. Sverdlov and H. Morkoc, University of Illinois, Urbana, IL 205

4:00 p.m.

- 8.8 **Discussion Session**

Session 9: Vacuum Electronics—Microwave Tubes 209

Monday, December 11, 1:00 p.m.

Thoroughbred Room

Co Chairmen: F. Payen, Thomson Tubes Electroniques
G. Groshart, Northrop Grumman Corp.

1:00 p.m.

Introduction

1:05 p.m.

- 9.1 **Application of the "Kievafella" Permanent Magnet Focusing System to Linear Beam Microwave Tubes**, D. Furuno, D. Myers, K. Lancaster, H. Leupold*, E. Potenziari, II*, A. Nanji** and G. Sadakane**, Lockheed Martin Advanced Development Operations, San Diego, CA and *US Army Research Lab, Ft. Monmouth, NJ and Magnet Sales and Mfg. Inc., Culver City, CA 211

1:30 p.m.

- 9.2 **A CHI Wiggler Ubitron Amplifier Experiment: Wiggler Characterization**, J. Taccetti, R. Jackson, J. Freund, D. Pershing, M. Blank, V. Granatstein, Naval Research Laboratory, Washington, DC 215

1:55 p.m.

- 9.3 **The Development of High Frequency, Megawatt Gyrotrons for ITER**, K. Kreischer, B. Danly, J. Hogge, T. Kimura, R. Temkin and M. Read*, Massachusetts Institute of Technology, Cambridge, MA and *Physical Sciences, Inc., Alexandria, VA 219

2:20 p.m.

- 9.4 **Window-Temperature Measurements on a High-Power Gyrotron with an Internal, Quasi-Optical Converter**, T. Chu, P. Borchard, K. Felch, H. Jory, C. Loring, Jr., J. Neilson, J. Lorbeck*, G. Haldeman** and M. Blank**, Varian Associates, Inc., Palo Alto, CA and *University of Wisconsin, Madison, WI and **MIT Plasma Fusion Center, Cambridge, MA 223

2:45 p.m.

- 9.5 **Design of Two Low Voltage, Axially-Modulated, Cusp-Injected Gyrotron Amplifier Experiments**, W. Lawson, J. Rodgers, A. Grigoropoulos, A. Liu and W. Destler, University of Maryland, College Park, MD 227

3:10 p.m.

- 9.6 **Characteristics of a Stable 200 kW Second-Harmonic Gyro-TWT Amplifier**, Q. Wang, D. McDermott and N. Luhmann, Jr., University of California, Davis, CA 231

3:35 p.m.

- 9.7 **Initial Operation of a 100MW Fundamental Frequency Gyroklystron**, J. Cheng, W. Lawson, J. Calame, B. Hogan, M. Castle, P. Latham, M. Reiser and V. Granatstein, University of Maryland, College Park, MD 235

Session 10: Device Interconnect Technology—Evolutionary Interconnect Technology 239

Tuesday, December 12, 9:00 a.m.

International Ballroom East

Co-Chairmen: Carole Graas, Texas Instruments, Inc.
David Thomas, IBM

9:00 a.m.

Introduction

9:05 a.m.

- 10.1 **Interconnect Scaling—The Real Limiter to High Performance ULSI (Invited Paper)**, M. Bohr, Intel Corporation, Hillsboro, OR 241

9:30 a.m.

- 10.2 **A Scaling Scheme for Interconnect in Deep-Submicron Processes**, K. Rahmat, O. Nakagawa, S. Oh and J. Moll, Hewlett-Packard Co., Palo Alto, CA and W.T. Lynch, JRC, Research Triangle Park, NC 245

9:55 a.m.

- 10.3 **Interconnect Capacitances, Crosstalk, and Signal Delay in Vertically Integrated Circuits**, S. Kuhn*, M. Kleiner*, P. Ramm and W. Weber, Siemens AG, Munich, Germany, *Siemens AG, Munich, Germany and Technical University of Munich, Munich, Germany 249

10:20 a.m.

Discussion Session

10:45 a.m.

- 10.5 **Excellent Electro/Stress-Migration-Resistance Surface-Silicide Passivated Giant-Grain Cu-Mg Alloy Interconnect Technology for Giga Scale Integration (GSI)**, T. Takewaki, R. Kaihara, T. Ohmi and T. Nitta*, Tohoku University, Sendai, Japan, *Hitachi Ltd, Tokyo, Japan 253

11:10 a.m.

- 10.6 Low Temperature, Low Resistivity Sub-Half Micron Via/Interconnect Structure Using Reaction of Al-Alloys and Germane**, R. Joshi and M. Tejwani, IBM, Yorktown Heights, NY **257**

Session 11: Integrated Circuits—Flash Memory Technology

Tuesday, December 12, 9:00 a.m.
International Ballroom Center

Co-Chairmen: Seiichi Mori, Toshiba
Sameer Haddad, AMD

9:00 a.m.

Introduction

9:05 a.m.

- 11.1 A Novel Dual String NOR (DuSNOR) Memory Cell Technology Scalable to the 256Mbit and 1Gbit Flash Memories**, K. Kim, J. Kim, J. Yoo, Y. Choi, M. Kim, B. Nam, K. Park, S. Ahn and O. Kwon, Samsung Electronics Co., Ltd., Kyungki-Do, Korea **263**

9:30 a.m.

- 11.2 A New Cell Structure for Sub-Quarter Micron High Density Flash Memory**, Y. Yamauchi, M. Yoshimi, S. Sato, H. Tabuchi, N. Takenaka and K. Sakiyam, Sharp Corporation, Nara, Japan **267**

9:55 a.m.

- 11.3 Multi-Level Flash/EPROM Memories: New Self-Convergent Programming Methods for Low-Voltage Applications**, M. Chi and A. Bergemont, National Semiconductor, Santa Clara, CA **271**

10:20 a.m.

- 11.4 A Novel Side-Wall Transfer-Transistor Cell (SWATT Cell) for Multi-level NAND EEPROMs**, S. Aritome, Y. Takeuchi, S. Satoh, H. Watanabe, K. Shimizu, G. Hemink, R. Shiota, Toshiba R&D Center, Kawasaki, Japan **275**

10:45 a.m.

- 11.5 Novel Electron Injection Method Using Band-to-Band Tunneling Induced Hot Electron (BBHE) for Flash Memory with a P-Channel Cell**, T. Ohnakado, K. Mitsunaga, M. Nunoshita, H. Onoda, K. Sakakibara, N. Tsuji, N. Ajika, M. Hatanaka and H. Miyoshi, Mitsubishi Electric Corporation, Hyogo, Japan **279**

11:10 a.m.

- 11.6 Substrate-Current-Induced Hot Electron (SCIHE) Injection: A New Convergence Scheme for Flash Memory**, C.-Y. Hu, D. Kencke, S. Banerjee, R. Richart*, B. Bandyopadhyay*, B. Moore*, E. Ibok* and S. Garg*, University of Texas, Austin, TX and *Advanced Micro Devices, Inc., Austin, TX **283**

11:35 a.m.

- 11.7 Discussion Session: Flash Memory Cell Scaling Issues for 256Mbit Generation and Beyond**

Session 12: Modeling and Simulation—Hot Carrier Effects and Monte Carlo Simulation

Tuesday, December 12, 9:00 a.m.
Jefferson Room

Co-Chairmen: Zhiping Yu, Stanford University
Christine Maziar, University of Texas at Austin

9:00 a.m.

Introduction

9:05 a.m.

- 12.1 The Numerical Simulation of Substrate and Gate Currents in MOS and EPROMs**, A. Concannon, F. Piccinini*, A. Mathewson and C. Lombardi*, University College Cork, Cork, Ireland and *SGS-Thomson Microelectronics, Agrate, Italy **289**

9:30 a.m.

- 12.2 Characterization and Modeling of Hot-Carrier Luminescence in Silicon n/n/n Devices**, L. Selmi, M. Mastrapasqua*, D. Boulin**, J. Bude**, M. Manfredi***, E. Sangiorgi**** and M. Pinto**, Univ. of Bologna, Italy, *Univ. of Eindhoven, Netherlands, **AT&T Bell Labs., Murray Hill, NJ, ***Univ. of Parma, Italy, ****Univ. of Udine, Italy **293**

9:55 a.m.

- 12.3 New Monte Carlo Simulation for Polycrystalline Silicon Thin-Film Transistor**, T. Shimatani and M. Koyanagi, Tohoku University, Sendai, Japan **297**

10:20 a.m.

- 12.4 Hot Carrier Effects in Short MOSFETs at Low Applied Voltages**, A. Abramo, C. Fiegna* and F. Venturi**, University of Bologna, Bologna, Italy and *University of Ferrara, Italy and **University of Parma, Parma, Italy **301**

10:45 a.m.

- 12.5 Monte Carlo Study of Sub-Band-Gap Impact Ionization in Small Silicon Field-Effect Transistors**, M. Fischetti and S. Laux, IBM Research Division, Yorktown Heights, NY **305**

11:10 a.m.

Discussion Session

Session 13: CMOS Devices and Reliability—Plasma Damage and Gate Oxide Reliability

Tuesday, December 12, 9:00 a.m.
Lincoln Room

Co-Chairmen: Jack Y.-C. Sun, IBM
Ih-Chin Chen, Texas Instruments

9:00 a.m.

Introduction

9:05 a.m.

- 13.1 Role of Temperature in Process-Induced Charging Damage in Sub-micron CMOS Transistors**, T. Brozek, Y. Chan* and C. Viswanathan, University of California, Los Angeles, CA and *Sematech, Austin, TX **311**

9:30 a.m.

- 13.2 High Density Plasma Etch Induced Damage to Thin Gate Oxide**, S. Krishnan, S. Aur, G. Wilhite* and R. Rajgopal, Texas Instruments, Dallas, TX and *Prairie View A&M, TX, Prairie View, TX **315**

9:55 a.m.

- 13.3 Effects of Oxide Exposure, Photoresist and Dopant Activation on the Plasma Damage Immunity of Ultrathin Oxides and Oxynitrides**, K. Lai, K. Kumar, A. Chou and J. Lee, University of Texas, Austin, TX **319**

10:20 a.m.

- 13.4 A New Gate Oxide Lifetime Prediction Method Using Cumulative Damage Law and Its Applications to Plasma-Damaged Oxides**, K. Eriguchi, Y. Uraoka and S. Odanaka, Matsushita Electric Ind. Co., Ltd., Osaka, Japan **323**

10:45 a.m.

- 13.5 The Impact of Nitrogen Profile Engineering on Ultra-Thin Nitrided Oxide Films for Dual-Gate CMOS ULSI**, E. Hasegawa, M. Kawata, K. Ando, M. Makabe, M. Kitakata, A. Ishitani, L. Manchanda*, M. Green**, K. Krisch** and L. Feldman**, NEC Corporation, Kanagawa, Japan, *AT&T Bell Laboratories, Holmdel, NJ, **AT&T Bell Labs, Murray Hill, NJ **327**

- 11:10 a.m.
13.6 Short Channel Enhanced Degradation During Discharge of Flash EEPROM Memory Cell, J. Chen, J. Hsu, S. Luan, Y. Tang, D. Liu, S. Haddad, C. Chang, S. Longcor, J. Lien, Advanced Micro Devices, Sunnyvale, CA 331

Session 14: Solid State Devices—ESD Protection, Discrete Power and Bipolar Devices 335

Tuesday, December 12, 9:00 a.m.
Georgetown Room

Co-Chairmen: Sophie Verdonckt-Vandebroek, Xerox
 T. Paul Chow, Rensselaer Polytechnic Institute

- 9:00 a.m.
Introduction
- 9:05 a.m.
14.1 Bipolar SCR ESD Protection Circuit for High Speed Submicron Bipolar/BiCMOS Circuits, J. Chen, A. Amerasekera and T. Vrotsos, Texas Instruments, Dallas, TX 337
- 9:30 a.m.
14.2 A Hot-Carrier Triggered SCR for Smart Power Bus ESD Protection, J. Watt and A. Walker, Cypress Semiconductor Corp., San Jose, CA 341
- 9:55 a.m.
14.3 Efficient NPN Operation in High Voltage NMOSFET for ESD Robustness, C. Duvvury, D. Briggs, J. Rodriguez, F. Carvajal, A. Young, D. Redwine and M. Smayling, Texas Instruments, Inc., Dallas, TX 345
- 10:20 a.m.
14.4 A Planar MOS-Gated AC Switch Structure, M. Mehrotra and B. Baliga, North Carolina State University, Raleigh, NC 349
- 10:45 a.m.
14.5 High Power 4H-SiC Static Induction Transistors, R. Siergiej, R. Clarke, A. Agarwal, C. Brandt, A. Burk, Jr., A. Morse* and P. Orphanos, Westinghouse Science and Technology Center, Pittsburgh, PA and *Westinghouse Electric Corporation, Baltimore, MD 353
- 11:10 a.m.
14.6 Correlation of Low-Frequency Noise and Emitter-Base Reverse-Bias Stress in Epitaxial Si- and SiGe-base Bipolar Transistors, J. Babcock, J. Cressler, L. Vempati, A. Joseph and D. Hareme*, Auburn University, Auburn, AL and *IBM Microelectronics Division, Hopewell Junction, NY 357

Session 15: Quantum Electronics and Compound Semiconductor Devices—Quantum and Novel Devices 361

Tuesday, December 12, 9:00 a.m.
Monroe Room

Co-Chairmen: Ilesanmi Adesida, University of Illinois
 D. Crawford, National Science Foundation

- 9:00 a.m.
Introduction
- 9:05 a.m.
15.1 Comparison of Experimental and Theoretical Results of Room Temperature Operated Single Electron Transistor Made by STM/AFM Nano-Oxidation Process, K. Matsumoto, M. Ishii, J. Shirakashi, K. Segawa, Y. Oka, B. Vartanian* and J. Harris*, Electrotechnical Laboratory, Tsukuba, Japan and *Stanford University, Stanford, CA 363
- 9:30 a.m.
15.2 Silicon Single Hole Quantum Dot Transistors for Complementary Digital Circuits, E. Leobandung, L. Guo, Y. Wang and S. Chou, University of Minnesota, Minneapolis, MN 367

- 9:55 a.m.
15.3 Electron Transport Properties in InAs Self-Assembled Quantum Dot HEMTs, N. Horiguchi, T. Futatsugi, Y. Nakata and N. Yokoyama, Fujitsu Laboratories, Ltd., Atsugi, Japan 371
- 10:20 a.m.
15.4 A Novel Semimetallic Quantum Well FET, M. Yang, F.C. Wang*, C. Yang*, B. Bennett, and T.Q. Do**, Naval Research Laboratory, Washington, DC and *University of Maryland, College Park, MD, **SFA Inc., Landover, MD 375
- 10:45 a.m.
15.5 Novel Current-Voltage Characteristics of an InP-Based Resonant-Tunneling High Electron Mobility Transistor and Their Circuit Applications, K. Chen, K. Maezawa and M. Yamamoto, NTT LSI Laboratories, Kanagawa, Japan 379
- 11:10 a.m.
15.6 In-Situ Ga₂O₃ Process for GaAs Inversion/Accumulation Device and Surface Passivation Applications, M. Passlack, M. Hong, J. Mannaerts, S. Chu, N. Moriya and R. Opila, AT&T Bell Laboratories, Murray Hill, NJ 383

Session 16: Vacuum Electronics—Field Emitter Arrays and Photocathodes 387

Tuesday, December 12, 9:00 a.m.
Thoroughbred Room

Co-Chairmen: Thomas Hargreaves, Litton Systems EDD
 Kevin Jensen, NRL

- 9:00 a.m.
Introduction
- 9:05 a.m.
16.1 Field-Emitter-Array Development for Microwave Applications, C. Spindt, C. Holland, P. Schwoebel and I. Brodie, SRI International Menlo Park, CA 389
- 9:30 a.m.
16.2 Tower Structure Si Filled Emitter Arrays with Large Emission Current, Y. Hori, K. Koga, K. Sakiyama, Matsushita Electric Industrial Co. Ltd., Osaka, Japan, S. Kanemaru, J. Itoh, Electrotechnical Laboratory, Ibaraki, Japan 393
- 9:55 a.m.
16.3 A Robust Gated-Field-Emission Triode, S. Lu*, J. Huang, J. Tsai, D. Liu, J. Wang, J. Peng, W. Wang and C. Lee*, ERSO/ITRI, Taiwan, Rep. of China and *National Chiao-Tung University, Taiwan, Rep. of China 397
- 10:20 a.m.
16.4 Scaling-down of Cone-like Field Emitter Using LOCOS, C. Lee, H. Ahn and J. Lee, Seoul National University, Seoul, Korea 401
- 10:45 a.m.
16.5 Volcano-Shaped Field Emitters for Large Area Displays, H. Busta, G. Gammie, S. Skala, J. Pogemiller, R. Nowicki, J. Hubacek, D. Devine, R. Rao and W. Urbnek*, Coloray Display Corp., Fremont, CA and *Silicon Microstructures Inc., Fremont, CA 405
- 11:10 a.m.
16.6 High-Performance Negative Electron Affinity Photocathodes for High Resolution Electron Beam Lithography and Metrology, A. Baum, J. Schneider, and R. Pease, Stanford University, Stanford, CA 409

Session 17: CMOS Devices and Reliability— Advanced CMOS Devices and Reliability

413

Tuesday, December 12, 2:15 p.m.
International Ballroom East

Co-Chairmen: Jim Hayden, Motorola
Mark Gardner, Advanced Micro Devices

2:15 p.m.

Introduction

2:20 p.m.

- 17.1 **A Scaled 1.8V, 0.18 μ m Gate Length CMOS Technology: Device Design and Reliability Considerations**, M. Rodder, S. Aur and I. Chen, Texas Instruments, Dallas, TX 415

2:45 p.m.

- 17.2 **Device Drive Current Degradation Observed with Retrograde Channel Profiles**, S. Venkatesan, J. Lutze, C. Lage and W. Taylor, Motorola, Austin, TX 419

3:10 p.m.

- 17.3 **Reverse Short Channel Effect and Channel Length Dependence of Boron Penetration in PMOSFETs**, C. Subramanian, J. Hayden, W. Taylor, M. Orlowski and T. McNelly, Motorola, Austin, TX 423

3:35 p.m.

- 17.4 **The Effect of Source/Drain Processing on the Reverse Short Channel Effect of Deep Sub-Micron Bulk and SOI NMOSFETs**, S. Crowder, P. Rousseau, J. Snyder, J. Scott, P. Griffin and J. Plummer, Stanford University, Stanford, CA 427

4:00 p.m.

- 17.5 **A 0.1 μ m Inverted-Sidewall Recessed-Channel (ISRC) nMOSFET for High Performance and Reliability**, J. Lyu, B. Park, K. Chun and J. Lee, Seoul National University, Seoul, Korea 431

4:25 p.m.

- 17.6 **Performance and Reliability Optimization of Ultra Short Channel CMOS Device for Giga-bit DRAM Applications**, H. Hwang, K. Youn, J. Ahn, D. Yang, J. Ha, Y. Huh, J. Park, J. Kim and W. Kim, LG Semicon Co., Cheongju, Korea 435

4:50 p.m.

- 17.7 **A High Performance 0.1 μ m MOSFET with Asymmetric Channel Profile**, A. Hiroki, S. Odanaka, A. Hori, Matsushita Electric Industrial Co., Ltd., Osaka, Japan 439

Session 18: Device Interconnect Technology— Advanced Silicide and Metallization Technologies

443

Tuesday, December 12, 2:15 p.m.
International Ballroom Center

Co-Chairmen: Takamaro Kikkawa, NEC Corp.
Mehrdad Moslehi, CVC Products, Inc.

2:15 p.m.

Introduction

2:20 p.m.

- 18.1 **A New Cobalt Salicide Technology for 0.15 μ m CMOS Using High-Temperature Sputtering and In-Situ Vacuum Annealing**, K. Inoue, K. Mikagi, H. Abiko and T. Kikkawa, NEC Corporation, Kanagawa, Japan 445

2:45 p.m.

- 18.2 **Leakage Mechanism and Optimized Conditions of Co Salicide Process for Deep-submicron CMOS Devices**, K. Goto, A. Fushida*, J. Watanabe, T. Sukegawa*, K. Kawamura, T. Yamazaki*, T. Sugii, Fujitsu Laboratories Ltd., Atsugi, Japan, *Fujitsu Ltd., Kawasaki, Japan 449

3:10 p.m.

- 18.3 **Nitrogen-Doped Nickel Monosilicide Technique for Deep Submicron CMOS Salicide**, T. Ohguro, S. Nakamura, E. Morifuji, M. Ono, T. Yoshitomi, M. Saito, H. Momose and H. Iwai, Toshiba Corporation, Kawasaki, Japan 453

3:35 p.m.

- 18.4 **Novel Contamination Restrained Silicidation Processing Using Load-Lock LPCVD-Films and Lightly Doped Deep Drain (LD²) Structure for Deep Submicron Dual Gate CMOS**, H. Kotaki, M. Nakano, S. Hayashida, T. Matsuoka, S. Kakimoto, A. Nakano, K. Uda and Y. Sato, Sharp Corporation, Nara, Japan 457

4:00 p.m.

- 18.5 **A Comparative Study of CVD TiN and CVD TaN Diffusion Barriers for Copper Interconnection**, S. Sun, M. Tsai, H. Chiu, S. Chuang, C. Tsai, National Chiao Tung University, Taiwan, Republic of China 461

4:25 p.m.

- 18.6 **Completely Planarized W Plugs Using MnO₂ CMP**, S. Kishii, R. Suzuki, A. Ohishi, Y. Arimoto, Fujitsu Laboratories Ltd., Atsugi, Japan 465

4:50 p.m.

- 18.7 **In Situ CMP Monitoring Technique for Multi-layer Interconnection**, A. Fukuroda, K. Nakamura, Y. Arimoto, Fujitsu Laboratories Ltd., Atsugi, Japan 469

5:15 p.m.

- 18.8 **Fully Planarized Four-Level Interconnection with Stacked Vias Using CMP of Selective CVD-A1 and Insulator and its Application to Quarter Micron Gate Array LSIs**, T. Amazawa, E. Yamamoto, K. Sukuma, Y. Ito, K. Kamoshida, K. Ikeda, K. Saito, H. Ishii, S. Kato, S. Yagi, K. Hiraoka, T. Ueki, T. Takeda and Y. Arita, NTT LSI Laboratories, Kanagawa, Japan 473

Session 19: Modeling and Simulation—Back-End Process Modeling

477

Tuesday, December 12, 2:15 p.m.
Jefferson Room

Co-Chairmen: M. Duane, AMD
H. Matsumoto, NEC

2:15 p.m.

Introduction

2:20 p.m.

- 19.1 **CMOS Process Design for Minimization of IC Power Consumption Using TCAD (Invited Paper)**, A. Schwerin, D. Schumann and J. Berthold, Siemens, Munich, Germany 479

2:45 p.m.

- 19.2 **The Implications of Self-Consistent Current Density Design Guidelines Comprehending Electromigration and Joule Heating for Interconnect Technology Evolution**, W. Hunter, Texas Instruments, Dallas, TX 483

3:10 p.m.

- 19.3 **Thermal Analysis of Vertically Integrated Circuits**, M. Kleiner, S. Kuhn, P. Ramm*, W. Weber, Siemens AG, Munich, Germany, Technical University of Munich, Munich, Germany, *Fraunhofer Institute for Solid State Technology, Munich, Germany 487

3:35 p.m.

- 19.4 **Simulation and Modeling of the Effect of Substrate Conductivity on Coupling Inductance**, Y. Massoud and J. White, Massachusetts Institute of Technology, Cambridge, MA 491

4:00 p.m.

- 19.5 **"NET-AN" a Full Three-Dimensional Parasitic Interconnect Distributed RLC Extractor for Large Full Chip Scale Applications**, O. Akcasu, J. Lu, A. Dalal*, S. Mitra*, L. Lev*, N. Vasseggi**, A. Pance*, H. Hingarh*, H. Basit***, OEA International Inc., Santa Clara, CA, *Sun Microsystems, Inc., **Silicon Graphics, Inc., ***Rockwell International, Inc. 495

4:25 p.m.

- 19.6 **Using a Statistical Metrology Framework to Identify Systematic and Random Sources of Die and Wafer-level ILD Thickness Variation in CMP Processes**, E. Chang, B. Stine, T. Maung, R. Divecha, D. Boning, J. Chung, K. Chang*, G. Ray*, D. Bradbury*, O. Nakagawa, S. Oh*, and D. Bartelink*, Massachusetts Institute of Technology, Cambridge, MA and *Hewlett Packard Co., Palo Alto, CA 499

4:50 p.m.

- 19.7 **Finite Element Optimization of a MOSFET Structure: The Role of Interlayer Material for Residual Stress Reduction**, P. Ferreira, V. Senez, B. Baccus, J. Varon* and J. Lebaillly*, IEMN-ISEN, Villeneuve d'Ascq, France, *Philips Composants, Caen, France 503

Session 20: Solid State Devices—Novel Devices and Techniques 507

Tuesday, December 12, 2:15 p.m.
Lincoln Room

Co-Chairmen: R. J. Trew, Case Western Reserve University
N. Sasaki, Fujitsu

2:15 p.m.

Introduction

2:20 p.m.

- 20.1 **Si/SiGe High-Speed Field-Effect Transistors (Invited Paper)**, K. Ismail, IBM, T.J. Watson Research Center, Yorktown Heights, NY 509

2:45 p.m.

- 20.2 **A Novel Poly-Silicon-Capped Poly-Silicon-Germanium Thin-Film Transistor**, A. Tang, J. Tsai, R. Reif and T. King*, Massachusetts Institute of Technology, Cambridge, MA and *Xerox Palo Alto Research Center, Palo Alto, CA 513

3:10 p.m.

- 20.3 **Enhanced Hole Mobilities in Surface-Channel Strained-Si p-MOSFETs**, K. Rim, J. Welsner, J. Hoyt and J. Gibbons, Stanford University, Stanford, CA 517

3:35 p.m.

- 20.4 **Volatile and Non-Volatile Memories in Silicon with Nano-Crystal Storage**, S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan, and D. Buchanan, IBM Research Division, Yorktown Heights, NY 521

4:00 p.m.

- 20.5 **Impact of Coulomb Blockade on Low-Charge Limit of Memory Device**, K. Yano, T. Ishii, T. Sano, T. Mine, F. Murai and K. Seki, Hitachi, Ltd., Tokyo, Japan 525

4:25 p.m.

- 20.6 **Reference Voltages and Their Stress-Induced Changes in Thin Film Transistors as Determined by Charge Pumping**, A. Balasinski, J. Worley, M. Zamanian and F. Liou, Advanced Technology Development SGS-Thomson Microelectronics, Carrollton, TX 529

4:50 p.m.

- 20.7 **Silicon Film Thickness and Material Dependence of "Reverse Short Channel Effect" for SOI NMOSFETs**, R. Rajgopal, R. Schiebel, S. Iyer*, K. Joyner and T. Houston, Texas Instruments, Dallas, TX and *University of California, Berkeley, CA 533

Session 21: Integrated Circuits—ESD and Other Specialized Structures 537

Tuesday, December 12, 2:15 p.m.
Georgetown Room

Co-Chairmen: Lal Sood, Motorola
Tohru Mogami, NEC

2:15 p.m.

Introduction

2:20 p.m.

- 21.1 **A Novel On-Chip Electrostatic Discharge (ESD) Protection for Beyond 500MHz DRAM**, K. Narita, Y. Horiguchi, T. Fujii and K. Nakamura, NEC Corporation, Kanagawa, Japan 539

2:45 p.m.

- 21.2 **ESD Protection for Deep-Submicron CMOS Technology Using Gate-Couple CMOS-Trigger Lateral SCR Structure**, M. Ker, H. Chang and C-Y. Wu, National Chiao-Tung University, Taiwan, Republic of China 543

3:10 p.m.

- 21.3 **Substrate Triggering and Salicide Effects on ESD Performance and Protection Circuit Design in Deep Submicron CMOS Processes**, A. Amerasekera, C. Duvvury, V. Reddy and M. Rodder, Texas Instruments, Dallas, TX 547

3:35 p.m.

- 21.4 **On-State Reliability of Amorphous Silicon Antifuses**, G. Zhang, Y. King*, C. Hu, P. Yu, T. Jing, S. Eltoukhy* and E. Hamdy*, University of Berkeley, CA and *Actel Corp., Sunnyvale, CA 551

4:00 p.m.

- 21.5 **A Neuron MOS Transistor-Based Multiplier Cell**, W. Weber, S. Prange, R. Thewes and E. Wohlrab, Siemens Corporate Research, Munich, Germany 555

Session 22: Quantum Electronics and Compound Semiconductor Devices—Opto Electronics 559

Tuesday, December 12, 2:15 p.m.
Monroe Room

Co-Chairmen: Gerald Witt, AFOSR
Y.-K. Chen, AT&T Bell Laboratories

2:15 p.m.

Introduction

2:20 p.m.

- 22.1 **Novel Components for Wavelength Division Multiplexed Systems Based on Monolithic Multiplexer/Amplifier Integration (Invited Paper)**, M. Zirngibl, AT&T Bell Labs, Holmdel, NJ 561

2:45 p.m.

- 22.2 **Low-Noise 650nm-Band AlGaInP Visible Lasers with Highly-Doped Saturable Absorbing (HDSA) Layer**, I. Kidoguchi, H. Adachi, S. Kamiyama, T. Fukuhisa, M. Mannoh, A. Takamore and T. Uenoyama*, Matsushita Electric Industrial Co., Ltd, Osaka, Japan and *Matsushita Electric Industrial Co., Ltd, Kyoto, Japan 563

3:10 p.m.

- 22.3 **100mW High-Power Angled-Stripe Superluminescent Diodes with a New Real Refractive Index Guided Self-Aligned Structure**, T. Takayama, O. Imafuji, Y. Kouchi, M. Yuri, M. Kume, A. Yoshikawa and K. Itoh, Matsushita Electronics Corporation, Osaka, Japan 567

3:35 p.m.

- 22.4 **Device Modelling of Polymer Light-Emitting Diodes**, P. W. M. Blom, M.J.M. deJong and C.T.H.F. Liedenbaum, Philips Research Laboratories, Eindhoven, The Netherlands 571