COMPUTER-AIDED DESIGN AND VLSI DEVICE DEVELOPMENT

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KLUWER ACADEMIC PUBLISHERS
Boston/Dordrecht/Lancaster

Distributors for North America:
Kluwer Academic Publishers
190 Old Derby Street
Hingham, Massachusetts 02043, USA

Distributors for the UK and Ireland:
Kluwer Academic Publishers
MTP Press Limited
Falcon House, Queen Square
Lancaster LA1 1RN, UNITED KINGDOM

Distributors for all other countries:
Kluwer Academic Publishers Group
Distribution Centre
Post Office Box 322
3300 AH Dordrecht, THE NETHERLANDS

Library of Congress Cataloging-in-Publication Data
Main entry under title:

Computer-aided design and VLSI device development.

(The Kluwer international series in engineering and computer science ; SECS . VLSI, computer architecture, and digital signal processing)
Bibliography: p.
Includes index.
1. Integrated circuits—Very large scale integration—Design and construction—Data processing. 2. Computer-aided design. I. Cham, Kit Man. II. Series: Kluwer international series in engineering and computer science ; SECS . III. Series: Kluwer international series in engineering and computer science. VLSI, computer architecture, and digital signal processing.
TX7874.C6474 1986 621.395 85-19916
ISBN 0-89838-204-1

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Printed in the United States of America

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PREFACE

This book is concerned with the use of Computer-Aided Design (CAD) in the device and process development of Very-Large-Scale-Integrated Circuits (VLSI). The emphasis is in Metal-Oxide-Semiconductor (MOS) technology. State-of-the-art device and process development are presented.

This book is intended as a reference for engineers involved in VLSI development who have to solve many device and process problems. CAD specialists will also find this book useful since it discusses the organization of the simulation system, and also presents many case studies where the user applies the CAD tools in different situations. This book is also intended as a text or reference for graduate students in the field of integrated circuit fabrication. Major areas of device physics and processing are described and illustrated with simulations.

The material in this book is a result of several years of work on the implementation of the simulation system, the refinement of physical models in the simulation programs, and the application of the programs to many cases of device developments. The text began as publications in journals and conference proceedings, as well as lecture notes for a Hewlett-Packard internal CAD course.

This book consists of two parts. It begins with an overview of the status of CAD in VLSI, which points out why CAD is essential in VLSI development. Part A presents the organization of the two-dimensional simulation system. The process, device and parasitics simulation programs are described in some detail. The basic principles, input file format and application examples are presented. These chapters are intended to introduce the reader to the programs. Since these programs are in the public domain, the reader is referred to

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the manuals for more details. Part B of the book presents case studies, where the application of simulation tools to solve VLSI device design problems is described in detail. The physics of the problems are illustrated with the aid of numerical simulations. Solutions to these problems are presented. Issues in state-of-the-art device development such as drain-induced barrier lowering, trench isolation, hot electron effects, device scaling and interconnect parasitics are discussed.

For the book to be used as a textbook, we recommend that it be used for a semester course. If the course deals with device modeling and computer-aided design tools, then Part A of the book should be emphasized. The student will learn about the fundamentals of process and device simulation programs and simulation system organization. If the course deals with device physics and process development, then Part B of the book should be emphasized. The student will learn about current issues in VLSI device development. In either case, Part A and Part B of the book will complement each other.

We are grateful that Dr. John Chi-Hung Hui has contributed Chapter 11 on the issue of hot electron degradation effects in submicron n-channel MOSFETs. The optimization of the LDD structure for reducing the hot electron degradation is described in detail.

We are also grateful that Dr. Sukgi Choi has contributed Chapter 12 on the issue of device scaling. The scaling of n-channel enhancement and depletion mode devices are presented. Factors causing the device characteristics to deviate from classical scaling rules, as well as complications involved in short channel device scaling such as punchthrough are discussed.

We are indebted to Dr. P. Vande Voorde, Dr. D. Wenocur and Mr. M. Varon for proofreading the manuscripts. Mr. K. Ogasaki has been assisting us with the computer graphics which produced many of the figures in this book. Thanks are to Mr. T. Ekstedt who has kindly assisted the formatting of the text, and Dr. S.-L. Ng who has assisted in preparing many of the figures.

The manuscript was prepared by the TDP software on the HP3000 computer. Most of the simulations were performed on the HP1000 computer. We are grateful to the system managers for their support and assistance.

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We are indebted to many of our colleagues at Hewlett-Packard Laboratories for providing us with many ideas and suggestions, and to our management for providing an opportunity for us to complete this task.

Finally, we would like to thank our families for their spiritual support, patience and understanding during preparation of the manuscript.

Overview

In order to bring out the importance of Computer-Aided Design(CAD) in VLSI(Very-Large-Scale Integration) device design, it is necessary to discuss the evolution of the Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) and the issues involved in its scaling. MOSFETs, first proposed 50 years ago, are based on the principle of modulating longitudinal electrical conductance by varying a transverse electrical field. Since its conception, MOSFET technology has improved steadily and has become the primary technology for large-scale circuit integration on a monolithic chip, primarily because of the simple device structure. VLSI development for greater functional complexity and circuit performance on a single chip is strongly motivated by the reduced cost per device and has been achieved in part by larger chip areas, but predominantly by smaller device dimensions and the clever design of devices and circuits.

A general guide to the smaller devices in MOSFETs and associated benefits, has been proposed by Dennard et al [1] (MOSFET scaling). This proposed scheme assumes that the x and y dimensions (in the circuit plane) are large compared to the z-dimension for the active device. The scaling method is also restricted to MOS devices and circuits. The active portion of MOS devices is typically restricted to within one or two microns of the crystal surface and interconnection dielectrics and metals are less than one micron in thickness. Thus we should expect that the guidelines as proposed by Dennard should be reasonably valid for minimum circuit dimensions of two microns or greater. As the dimensions decrease below two microns, problems are introduced in both

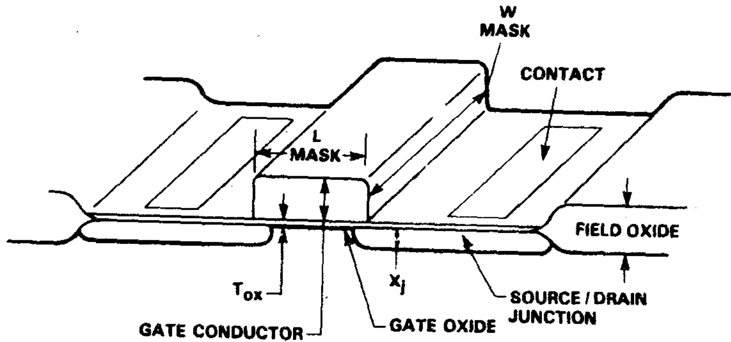

Fig. 1 Generic MOS Transistor.

fabrications and device operations that are not significant in larger long-channel devices. The 2-D aspects of the impurity profiles and oxidation process become important in determining the effective channel length and width. More processing steps are required, such as channel implantation and local oxidation, which make more stringent control of the process necessary. Secondary effects, such as oxidation-enhanced diffusion significantly affect the impurity profile. As a result, better understanding and accurate control of these phenomena are crucial to achieving the desired performance from the scaled devices.

For the device operation, we will examine many of the scaling assumptions as applied to the long channel, wide conductor circuits. Also, in each case, there have been practical departures from the scaling assumptions. The original rules proposed that physical dimensions were scaled so that all electric field patterns were kept constant. Fig. 1 shows a generic MOS transistor and the various dimensions. Table 1 gives Dennard's constant field scaling rule, even though these have not been the general practice. When a process is scaled to smaller dimensions, the x,y and z dimensions are all scaled by the same amount. In addition, the applied voltages are scaled in constant field scaling to maintain constant field pattern.

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W, L, T_{ox}, V, N_b		$\propto K^{-1}$
I_{DS}	$\propto (W/L)(V^2/T_{ox})$	$\propto K^{-1}$
C_g	$\propto W\,L\,C_{ox}$	$\propto K^{-1}$
t_d	$\propto C_g V / I$	$\propto K^{-1}$
P	$\propto V\,I$	$\propto K^{-2}$
P/A	$\propto V\,I / W\,L$	$\propto 1$
$P\,t_d$		$\propto K^{-3}$

Table 1 Dennard's constant field scaling.

Many scaling schemes have been proposed since the "constant field" proposal. It is useful to consider the actual scaling methods that have been followed. The desirability of electrical compatibility with bipolar TTL circuits and the five volt power supply standard has resulted in "constant voltage scaling" as far as circuit power supply is concerned. Sometimes the internal node voltages are changed as a result of scaling and re-design. If the source/drain junction is less than one micron and V_{DD} is retained at five volts, the electric field stress in the channel is too great and the MOS transistor characteristics drift with time because of the hot carrier charge trapping. It is possible, but not evident at this writing, that some modified structure such as a graded junction or a "low doped drain" (LDD) can allow five volt operation for sub-micron devices. This constant voltage scaling also makes the 2-D field coupling significant, which is negligible in the long-channel device. It is the major cause of all the short-channel effects. To model these short-channel effects, 2-D numerical simulations become necessary because 1-D analytical models are not adequate. We must, in any event, consider lower system voltage at some future time. Following examples illustrate several features of the scaling methods. The most evident is that whereas

most features of Dennard's constant field scaling are approximately retained from one generation of technology to the next, practical considerations have resulted in significant departures. Constant voltage scaling has in fact been the primary mode of scaling for most merchant suppliers. We can expect that a new power supply standard will be adopted and used until the dimensions are once more so small that device instability re-appears. Another departure from strict geometrical scaling has been in the vertical thickness of films. Conductor thickness has scaled very slowly in order to avoid electromigration effects in aluminum, or signal delay effects in polysilicon conductors. Table 2 shows the actual scaling done by most industrial suppliers. Either constant voltage or constant field scaling has resulted in improved circuits as measured by speed, and chip size and power for a given electronic function. As was mentioned earlier, circuit voltage, V_{DD}, will almost certainly be reduced for sub-micron devices. The tendency not to scale the interconnect or dielectric thickness (except gate oxide) will continue.

The future reduction of minimum features to less than one micron will undoubtedly bring further changes in actual scaling effects. The minimum practical conduction threshold for switches to turn off in dynamic circuits is approximately 0.6 volts. The desirability of dynamic operation in many electrical functions will keep CMOS circuit operation at about two volts. There will be exceptions such as the watch circuit that operates from a single battery cell. The peak current ($V_{GS} = V_{DS}/2$) per unit width scales as K^{-2} for long channel devices and constant voltage scaling. The effect of velocity saturation is to reduce this scaling factor to approximately K^{-1}. If width is also reduced by the same scaling factor of K, then peak current per unit width scales as K^{-1} for long channel and is almost constant for short channel. The transconductance follows the same behavior as current. Some switches such as the transistors in a static RAM cell are not required to switch particularly fast and have a small capacitive load. Hence the relative lack of increased performance from scaling, the smallest geometry device does not result in a performance problem inside the static RAM cell. On

PROCESS (COMPANY)	Leff (um)	Vt (volt)	VDD (volt)	Tox (nm)	Xj (um)
NMOS(Intel)	4.6		5.0	120	2.00
NMOS(HP)	3.0	0.8	5.0	100	
HMOSI(Intel)	2.9	0.7	5.0	70	0.80
NMOS(Xerox)	2.5		5.0	70	0.46
NMOS(HP)	2.0	0.8	5.0	50	0.20
HMOSII(Intel)	1.6	0.7	5.0	40	0.80
NMOS(HP)	1.4	0.6	3.0	40	0.30
HMOSIII(Intel)	1.1	0.7	5.0	25	0.30
NMOS(NTT)	1.0	0.5	5.0	30	0.25
NMOS(IBM)	0.8	0.6	2.5	25	0.35
NMOS(Toshiba)	0.5	0.5	3.0	15	0.23
NMOS(AT&T)	0.3		1.5	25	0.26

Table 2 Actual scaling done by the most industrial suppliers.

the other hand, devices that must drive long signal lines, clock lines, or word lines may require width-scaling that is not at all the same as length-scaling.

The scaling for commercial devices then will be to a new voltage standard of less than five volts as dimensions become sub-micron. The tendency in node capacitance is such that average wire length is a fraction of chip size. As more electronic functions are included on a chip, the chip size will continue to increase, and wire length also increases. In future scaling, the capacitance per unit length of wire for minimum pitch will stay almost constant since a large part of capacitance is fringing field or else inter-line. A new circuit design problem will be wire placement to minimize capacitance effects. To evaluate the actual capacitance values, the circuit extraction program coupled with the 2-D or 3-D parasitics simulator is indispensable.

An additional feature of scaling will be that the logic device width will be reduced by a smaller factor than the scaling factor. This feature is a result of the fact that the driving current per unit width only scales at best as $C_O \sim K^{-1}$. If the width is scaled by a factor of K, then the driving current per device at constant voltage will decrease somewhat as a result of various parasitic effects. The examples of minimum operating voltage and deleterious effects on performance are given to help illustrate the practical approach to sub-micron scaling.

The ability to calculate the effect of a process change on circuit or device electrical parameters has been an indispensable part of the rapid advances that have been made in semiconductor circuits ever since the beginning of the solid state micro-electronic industry. Experiments tend to establish the validity of theoretical concepts, establish empirical laws, as well as help discover new physical effects. A symbiontic relation has developed between experiment and associated theory (modeling) in which the modeling helps to guide the direction of experiments, and experiments establish the validity of models as well as produce devices and circuits with optimized performance.

The conventional process and device designs for integrated-circuit technologies have been based on a trial-and-error approach using

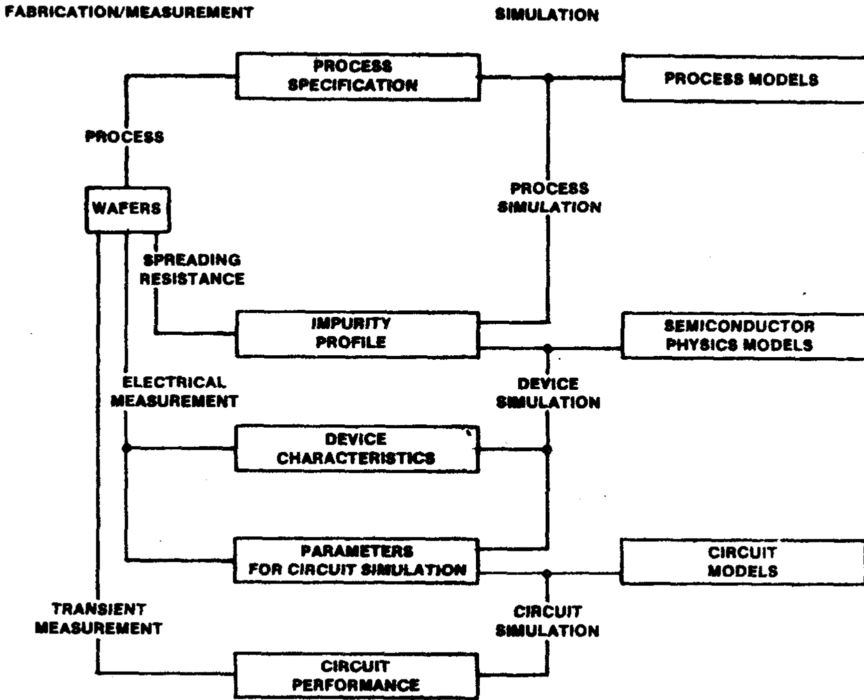

Fig. 2 Block diagram of the process development

fabrications and measurements plus simple 1-D analytical modeling to achieve the desired terminal electrical characteristics and circuit performances. The left half of Fig. 2 outlines a process, device, and circuit design using the fabrications and simple models. This approach is not, however, adequate for the small geometry devices. As mentioned in the review of scaling, the constant voltage scaling and the lack of vertical scaling make the 2-D field coupling more dominant in the device performance. Especially, the threshold voltage becomes a sensitive function of the channel length and the drain bias. The fringing and inter-line capacitances become significant in the wiring capacitance. The

velocity saturation also prohibits the simple 1-D model from accurately predicting the saturation currents. These factors force the engineers to resort more to the experiments. Thus, it drastically increases the cost and time to develop a scaled geometry process. Even with the experiments, complicated processes and structures make it difficult to get physical insight and quantitative analysis of the factors governing device operation.

A complementary analysis and design path through process, device, and circuit simulations has been proposed and is now widely accepted. In the process simulation, process-specification information is used to simulate the device structure and impurity distribution using the process models. Device simulation yields the terminal characteristics based on the device structure and the impurity profile from the process simulation and physical models. The SPICE parameters are extracted from the terminal characteristics and the layouts. Based on these parameters and circuit connectivity, circuit simulations yield the switching characteristics and provides the means to evaluate the circuit performances. Compared to laboratory experiment, the design path via simulation is less costly and faster; more important, it produces detailed information concerning device operation in a well-controlled environment.

A complete 2-D numerical simulation system has been implemented in Hewlett-Packard Laboratories since 1982. In part A, this numerical simulation system and its individual tools will be explained in detail so that the reader can get acquainted with these tools and learn how to use them. Most of these tools are in the public domain. Thus we also give the information of these programs in the appendix so that it will help the reader implement these tools. In part B, the applications of the system in modeling small geometry processes will be presented. These simulation tools are different with the simple analytical models. First, we try to develop a methodology to use these tools effectively in process development. Next, real examples which are typical in important topics of scaled process development will be given in detail to help the reader attack their real problems.

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