Programmable Logic Handbook

Geoff Bostock

Programmable Logic Handbook

Geoff Bostock

Collins Professional Books

8 Grafton Street London W1X 3LA

Collins Professional Books
William Collins Sons & Co. Ltd
8 Grafton Street, London W1X 3LA

First published in Great Britain by
Collins Professional Books 1987

British Library Cataloguing in Publication Data
Bostock, Geoff
Programmable logic handbook
1. Electronic digital computers 2 Logic design
I. Title
621.395 TK7888.3

ISBN 0–00–383213–9

Typeset by V & M Graphics Ltd, Aylesbury, Bucks
Printed and bound in Great Britain by
Mackays of Chatham, Kent

Preface

Programmable logic devices have been available for over 15 years yet, until now, there has been no comprehensive reference work covering the subject. This is because it has been possible, until recently, for the design engineer to choose from a fairly restricted range of devices; restricted both in the sense of being small in number and simple to understand. In the last few years, however, the choice of architecture has become wider and more powerful in its application possibilities.

In compiling the data for this book it was clear that the starting point was hard to define; how much previous knowledge of semiconductors and electronics could I assume that the reader has? The easy way out was to assume that the answer was none. The early chapters are a summary of the basics of semiconductor devices and the principles of logic but, because this is intended as a reference work, there are no formal proofs of the results obtained. The references at the end of the book contain any formal working required by the reader. However tempting it is to miss out these early chapters, which may appear trivial to readers well versed in electronics, some of the later points have their origins in these basic teachings.

To put programmable logic into perspective let us take a brief historical look at the subject. PROMs were the first devices to come to the market in about 1970, although whether they were intended as memories or logic is a moot point. The first true logic device was Signetics FPLA, introduced in 1974. Initially this was a limited success for a number of reasons; high complexity (for that time), inflexible architecture, large package and high price (compared with standard logic) being the chief ones. PALs, introduced by MMI in 1977, overcame many of the drawbacks of PLAs and took a lead in market share which they have never relinquished. The total market size is now over a billion dollars, shared between more than 100 device types.

Programmable logic has become a real competitor to standard logic on the one hand, and to masked ASICs on the other, but it still represents only a small fraction of their market size. There is thus a huge potential for growth with consequent benefits to designers, provided that they are in a position to take advantage of those benefits. This book is intended to help them take fullest advantage. All the currently available architectures are described in detail; the design methods are also covered. These range from manual techniques to high-powered CAE systems, showing that programmable logic is suitable for both low budget projects and highly equipped design centres.

One of the largest sections of the book is devoted to applications. These

include simple logic functions which can be used to build more complex functions and some ideas for the more complex functions themselves. The applications are intended to be diverse enough to show how most logic requirements can be fitted into programmable logic devices. Even if the application is not covered exactly, enough information is provided to enable the designer to make the best choice of device and be guided as to how to complete the design.

The student with no prior knowledge of programmable devices should find this work a useful primer, particularly when used in conjunction with standard text-books covering the formal aspects of logic design. I hope that established designers will also find it helpful as a reference work to keep by their benches. If it helps to breed a generation of logic designers who turn to programmable devices before looking at lists of TTL and CMOS standard functions, then it will have achieved its goal.

Geoff Bostock

Contents

Preface		ix
1	Introduction to Logic Devices	1
2	Programmable Device Techniques	14
3	Basic Logic Structures	32
4	Combinational PLDs	65
5	Sequential PLDs	93
6	Using Programmable Logic	138
7	Design Support for PLDs	158
8	Programmable Logic Applications	169
Conclusion		224
Appendix 1: PLD Manufacturer Details		226
Appendix 2: CAE Manufacturer Details		231
Appendix 3: Suggested Reading		236
Index		239

Chapter 1

Introduction to Logic Devices

1.1 BASIC PRINCIPLES

1.1.1 The idea of logic

In order to understand any discussion of what comprises a logic device it is necessary to be aware of what is meant by logic. In any system of logic, be it electrical or philosophical, the fundamental concept is that statements may be *true* or *false*. Conclusions about the state of the system being described are drawn from an analysis of which components of that system are true and which are false. For example, a simple combination lock might be devised in which two-way switches are placed in series with a relay. The relay would operate the lock mechanism; the system circuit is shown in Figure 1.1.

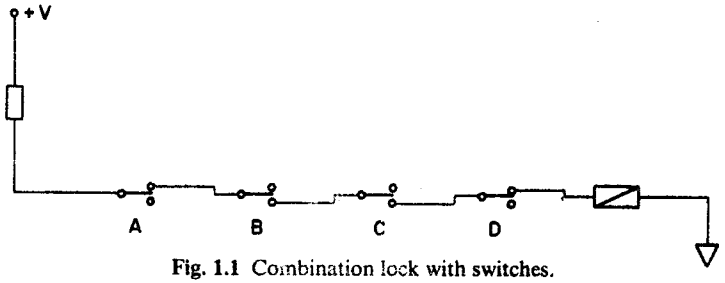

Fig. 1.1 Combination lock with switches.

Each switch is given a letter and only one combination of ups and downs will allow the lock to operate. In the system illustrated, with only four switches, it would not be very difficult to break the combination for there are only sixteen possibilities, but we will see in later chapters how the number can be extended to make a practical circuit. In our simple system it can be seen that the combination of A-up B-down C-down and D-up will open the lock. If up is equivalent to the *true* state and down is the *false* state, then a *logic equation* may be written to describe the circuit:

OPEN = A AND NOT B AND NOT C AND D

AND and NOT are the *logic operators* which define the relationships between the variables. In this example A and D must both be true and B and C false for the equation to be satisfied.

A similar system may be employed to make decisions about almost any

situation. While the human brain is quite capable of making these decisions it usually needs the data to be converted to a visual form. Electronic logic devices take the data in the form of electrical signals and use electronic switches to implement the logic equations. In our example we used mechanical switches as the logic elements as well as the interface between the outside world and the electrical system. Usually the interface is separated from the logic elements and from now on we will concentrate on the electronic devices used to perform the logic. The most common electronic switch is the transistor and the next section describes the two types used in practical circuits.

1.1.2 Transistor switches

1.1.2.1 Semiconductors

Before describing transistor operation it is necessary to appreciate the materials from which they are made. Matter under normal conditions is composed of atoms. In solid matter the atoms are bonded together and held in relatively fixed positions by the interaction of the electrons in their outer layers. Conducting materials, such as metals, do not use all their electrons for bonding so the spares are free to move within the solid boundary and will conduct electricity. Other substances, particularly those with complex molecules, have no spare electrons and are therefore insulators. The effect of temperature is also relevant.

When heated a solid absorbs energy; internally this energy is stored as vibration energy by the atoms or molecules. In a conductor this has the effect of reducing the available space for the electrons to move around in, so the bulk resistivity of the material is increased. The effect on insulators is different. Some of the energy is transferred to the electrons, which are then able to escape from their bonding duties and become free to conduct electricity. Those materials in which this property is noticeable at room temperature, particularly monatomic crystalline solids such as silicon and germanium, are called semiconductors.

There is a more controllable mechanism by which semiconductors may be made to conduct electricity. A small amount of an impurity may be added to a crystal without disturbing the lattice too greatly, provided that the atoms of the impurity are similar in size to the parent atoms. If the impurity has more electrons than the parent available for bonding the spare electrons become available for conduction. This is called an *n-type* semiconductor because the current is carried by negative charges. Conversely, it is possible that an impurity will have fewer electrons available for bonding than the parent, in which case there will be *holes* formed in the bonding layer. Under the influence of an electric field, electrons will move to fill adjacent holes leaving a hole where they were; this makes it appear as if the holes themselves are moving through the crystal. Such material is called a *p-type* semiconductor as the current is carried by positive charges.

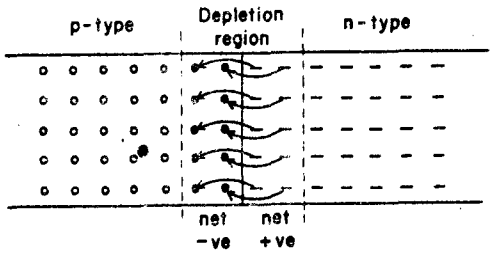

Fig. 1.2 p–n junction.

1.1.2.2 Diode junctions

While the current-carrying potential of a simple semiconductor depends simply on whether there is an excess of electrons or holes, a quite different situation exists when there is a junction between p-type and n-type material. At the junction itself there is a thin layer called the ***depletion region*** where the material is *intrinsic* and there are no free charge carriers. Figure 1.2 shows how the free electrons from the n-type side can diffuse to the other side and fill the holes, creating a potential barrier.

Applying a positive voltage to the n-type side pulls electrons away from the depletion region and increases the height of the barrier. In this case no current can flow through the junction. In the reverse case, when a negative voltage is applied to the n-type material, electrons are repelled towards the depletion region and cause the potential barrier to be lowered. When the barrier has been eliminated they meet holes which have been attracted from the p-type side of the junction. The electrons combine with the holes allowing a continuous flow of electrons in one direction and holes in the other. The net result is that there is a constant current flowing through the junction.

This property of the p–n junction, allowing current to flow in one direction but not the other, forms the basis of most electronic components from the diode to the VLSI integrated circuit.

1.1.2.3 MOS transistors

The MOS transistor is shown in cross-section in Figure 1.3. MOS is an acronym for Metal–Oxide–Silicon which describes the basic structure. The transistor is fabricated from a crystal of p-type silicon, into which impurities are diffused to form n-type regions called *sources* and *drains*. A thin layer of silicon dioxide is grown above the gap between each source and drain and a layer of metal or silicon deposited on the top. This top layer is called the *gate* and controls the current flow between the source and drain.

If the source and bulk silicon are held at the same voltage and the drain is taken to a more positive voltage then no current can flow between source and drain, because the drain-substrate junction is reverse-biased. If a positive voltage is now applied to the gate, electrons will be attracted into the region immediately

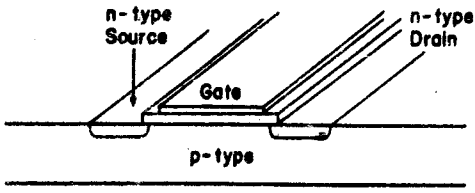

Fig. 1.3 MOS transistor structure.

below the oxide. This has the effect of making an n-type *channel*, which allows electrons to flow from source to drain. The voltage on the gate thus controls the flow of current through the transistor. A transistor of this type is called an *n-channel* device. A similar transistor made on an n-type substrate would be a *p-channel* device.

A MOS transistor can be used as a switch by connecting the current to be switched to source and drain, and connecting the controlling voltage to the gate. Because silicon dioxide is a good insulator, very little current has to be supplied by the control voltage; however, because the gate is acting as a capacitor there may be loading effects at high frequency. The channel is confined to a shallow region just below the surface and will therefore not permit very high currents to flow. The full consequences of these properties will be examined in a later chapter.

1.1.2.4 Bipolar transistors

If the n-type side of a p–n junction is doped more heavily with impurities than the p-type side, then many more electrons than holes will be attracted to the depletion region when the junction is *forward-biased*. Most of the electrons will then pass into the p-type material, where they will be 'eaten' gradually by holes. The electrons are said to be injected into the p-region. In a bipolar transistor, (Figure 1.4), the n-type region is called the *emitter* and the p-type region the *base*. The base is made very narrow and bordered by a second n-type region, the *collector*, which is usually made more positive than the base. Most of the electrons injected into the base will be attracted into the collector thus establishing a current flow between collector and emitter.

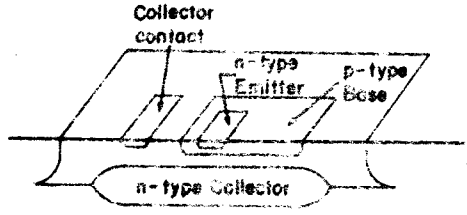

Fig. 1.4 Bipolar transistor structure.

The base controls the collector current as the voltage between base and emitter determines how much electron current is injected by the emitter. If the base voltage is too low to allow injection, then no current will flow in the transistor; thus the base acts as a control terminal for the bipolar transistor just as the gate does for the MOS device. Unlike the gate, the base must supply a small current to account for those electrons which are injected by the emitter but combine with holes before they reach the collector. However, because the area of the emitter can be made relatively large, a bipolar transistor can carry a larger current than an MOS.

The transistor described above is called an *npn* transistor to show the doping types of the three regions making up the device. It is also possible to make a *pnp* transistor where the dopings and voltages are reversed.

1.2 PRACTICAL LOGIC DEVICES

1.2.1 Planar technology

1.2.1.1 Masking and diffusion

Before embarking on a study of both standard logic families and programmable devices it is instructive to examine the technology used to fabricate integrated circuits. This is still based on the *planar process* developed in the late 1950s by the Fairchild Camera and Instrument Corporation. Figure 1.5 illustrates the steps required to create a p-type region in an n-type crystal of silicon. Slices, or wafers, about 1 mm thick are cut from a silicon crystal which has been grown by the *Czochralski* method. Current production uses wafers up to 150 mm in diameter. The wafers are chemically polished to remove mechanical damage incurred in the cutting process.

The first step is to grow a layer of silicon dioxide on the surface of the wafer. This is achieved by passing oxygen over the wafer in a furnace at a temperature of up to 1200° C. As many as fifty wafers may be processed at one time and furnace temperatures are controlled to better than 1° C. A thin layer of sensitive material is then applied to the surface of the wafer and the areas where p-type regions are required are defined. This may be achieved by exposure to ultraviolet light or an electron beam which polymerise the layer in areas which are to remain n-type. A photo-mask is used with ultraviolet light; the electron beam, which gives much finer definition, is electrically scanned over the wafer. The unpolymerised areas are dissolved in solvent to reveal the silicon dioxide surface, which is then chemically etched by hydrofluoric acid to expose the underlying silicon.

The next step involves another high-temperature furnace operation; in this case a gas containing the required impurity is passed over the wafers and forms a solid solution at the surface of the silicon. Prolonged exposure to temperature causes the impurity to diffuse into the silicon to a depth of a micrometre or more. The net result is a tub of p-type material in the n-type; the boundary between the

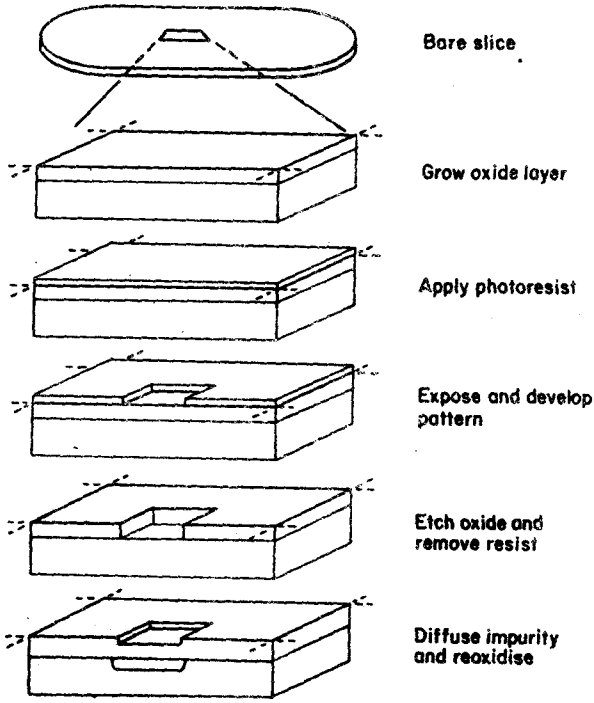

Fig. 1.5 Masking and diffusion steps (planar process).

two being a p–n junction. Successive diffusion steps are required to build up the transistor structures described in the previous section.

1.2.1.2 Metallisation

Having fabricated silicon-based components a way has to be found to enable them to be used. This involves connecting some kind of rigid metallic structure to the silicon to enable the device to be mounted, for example, on to a printed circuit board. The size of transistor features, usually a few micrometres, means that direct connection of wires is virtually impossible for reliable permanent joints. In practice, photolithography has to be used again. A metal, such as aluminium, is evaporated over the silicon surface to form a thin film. Windows previously etched in the silicon dioxide allow the aluminium to make contact to the silicon where connection is required. The aluminium itself is then etched to form conductive tracks from the silicon windows to metallic areas which are large enough to allow direct connection of wires.

Where the aluminium contacts the silicon an alloy is formed to ensure reliable connection. Aluminium is a p-type impurity in silicon so some care has to be taken when connecting to n-type areas. If the n-type area is heavily doped the depletion region will be extremely thin and holes and electrons will cross it very

easily even when it is reverse-biased. There will be no problem in connecting aluminum to p-type silicon as no junction is formed in this case.

1.2.1.3 Integrated circuits

As well as providing a conducting path from the silicon to the connecting wires, aluminium tracks can be used to connect diffused components in the same silicon wafer. Circuits containing several transistors, diodes, resistors and even capacitors can be connected-up on the silicon wafer surface, just as the discrete components can be connected on a printed circuit board. In principle, there is no limit, within the ingenuity of the designer, to the number of components which can be connected on a wafer. In practice, the planar process is subject to random faults caused by dirt particles or material defects. If a component has a fault it will not function correctly, so the circuit containing it will also be defective.

The potential number of circuits on a wafer depends on the area of the wafer and the area of a circuit. Probability theory can predict what proportion of these circuits will be faulty for a given level of fault densities. This enables manufacturers to calculate the largest circuit which they can make economically. Improvements in processing and materials technology cause a steady reduction in the fault density allowing larger circuits to be designed and manufactured.

1.2.1.4 Packaging

The final stage in integrated circuit manufacture is packaging. Most electronic assemblies are based on printed circuit technology so the integrated circuits have to be packaged into a form which is robust enough to withstand the handling they will receive, while allowing the connecting pins to be soldered into the *Printed Circuit Board* (PCB). The standard package is the ***dual-in-line*** which has two rows of pins fitting into a 0.1 in. grid. The pins are 0.1 in. apart; the row separation depends on the number of pins, usually 0.3 in., 0.6 in. or 0.9 in.

The packages are constructed on a frame, called the ***lead frame***; the circuit itself is alloyed to a central bar and fine wires, about 25 μm thick, bonded from the circuit to the pins. The whole frame is either sandwiched between two ceramic plates in an inert atmosphere, or moulded into solid plastic. The circuit is cropped out of the supporting frame and the leads formed into the conventional inverted 'U' to allow easy insertion into holes in the printed circuit board. Package sizes from eight to sixty-four pins are found in this form; the number of pins and package width are related by the mechanical problems of fitting the leads round the circuit. Reducing package size for a given pin-count is a major task, which has received the attention of most integrated circuits manufacturers.

A recent development is the *SO package* which has leads on a 0.05 in. spacing formed into an 'L' shape, which allows the circuit to sit on the board, instead of the pins passing through holes. The package may be stuck to the board and connection made by means of a solder paste laid down previously by a screen printing process. The smaller spacing means smaller packages, and other components are available in similar styles. Component placing may be

mechanised so the production process becomes cheaper, and the size reduction also means cheaper mechanical components. The whole process is called *surface mounting* and is probably the way that most production will be done in the future.

As logic functions become more complex they often need more connections, and the DIL and SO packages cannot cope with the pin numbers required. Another type of surface mounting package has been developed, based on having leads on all four sides. The first packages of this kind had a ceramic base with printed connections leading to plated areas at the edge of the package. These were intended for direct soldering to a ceramic substrate, as found in thin and thick film circuits. Special sockets were developed to enable these packages to be used on printed circuit boards; their lack of leads led to them being called *leadless chip carriers*, LLCCs for short. Plastic versions in the same style use leads bent into a 'J' and located in notches at the edge of the package; they are called *Plastic Leaded Chip Carriers*, or PLCCs. PLCCs and LLCCs have been developed for packages as small as twenty leads, but they are more useful for circuits with much larger counts, from forty-four to over 150 now possible.

1.2.2 Standard integrated circuit families

1.2.2.1 Bipolar logic circuits

Bipolar transistor action depends on the properties of p–n junctions which are below the silicon surface, albeit by only 1 or 2 μm. The active region of a MOS transistor is at the surface itself. The surface properties of silicon, and the ways to control them, were understood at a later time than the bulk properties, so bipolar logic circuits evolved before MOS. Figure 1.6 shows how bipolar silicon components can be connected to form an AND circuit.

If all three switches are open then no current will flow in any of the three input diodes. The base of the output transistor is thus connected to a positive voltage, so the transistor is switched on, current flows in the output resistor and the lamp will be turned on. If any of the switches is closed current will flow through the diode connected to it, so the voltage on the transistor base will be insufficient to

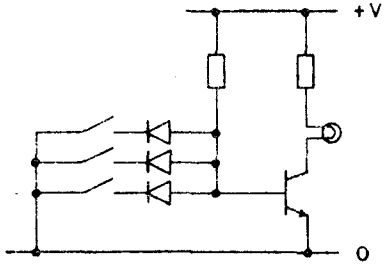

Fig. 1.6 AND function – bipolar.

allow it to conduct appreciably, and the lamp will not be lit. The lamp turns on only when all three switches are open so the circuit implements the AND function.

This circuit as it stands is not quite suitable to form the basis of a logic family. By amalgamating the input diodes into a single multi-emitter transistor and adding an output stage which will drive succeeding circuits the basic *transistor–transistor–logic*, or TTL, circuit of Figure 1.7, is formed. A whole family of logic functions based on the simple circuit described above has been designed over the past twenty years and now forms a major part of the circuit designer's armoury.

1.2.2.2 MOS logic circuits

Once the properties of silicon surfaces were understood, and the techniques for controlling them had been perfected, it became possible to construct logic

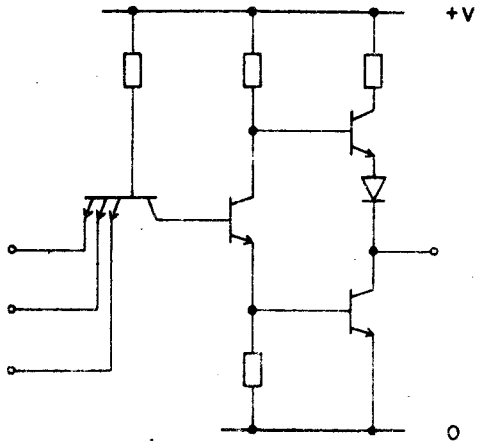

Fig. 1.7 TTL NAND gate.

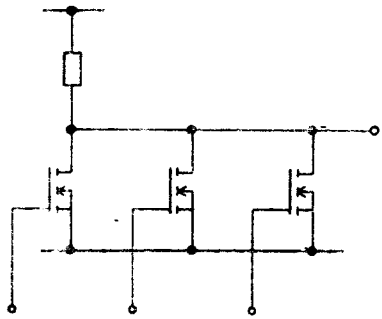

Fig. 1.8 NOR function-n-channel MOS.

circuits using MOS switches. The circuit in Figure 1.8 shows how a simple NOR gate can be built from MOS transistors. The transistors are *n-channel* type so any gate taken to a positive voltage will open a conductive path from the load resistor to ground. This structure will, however, provide no particular advantage over bipolar transistor circuits; indeed, the performance is likely to be worse because of the lower current capability and higher capacitance of MOS.

The identical function can be constructed from *p-channel* transistors, as shown in Figure 1.9, by connecting them in series. Any gate taken to a positive voltage will turn its channel off and prevent current from flowing in the chain. Again, no advantage is obtained from this structure, but consider what is achieved by combining the two, as in Figure 1.10. If any inputs are taken positive the *p-channel* transistors are switched off, while if all the inputs are negative the *n-channel* transistors do not conduct. Thus, no current flows in any steady state condition. The result is a logic circuit taking very little current; there is now a decided advantage over bipolar transistors.

1.2.2.3 Technology comparison

Some of the advantages of bipolar against MOS and vice versa have already been mentioned above. The choice between the two technologies is essentially dictated by practical considerations which are worth summarising here. The two chief performance criteria under consideration are usually speed and power. That is how fast the circuit will perform the function contained in it, and how much power must be supplied to it in operation. Usually, the faster the circuit the higher the power consumption, because speed is achieved by charging circuit capacitance quickly which involves the use of higher electrical currents.

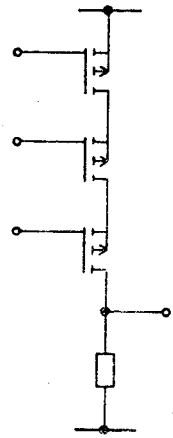

Fig. 1.9 NOR function – p-channel MOS.

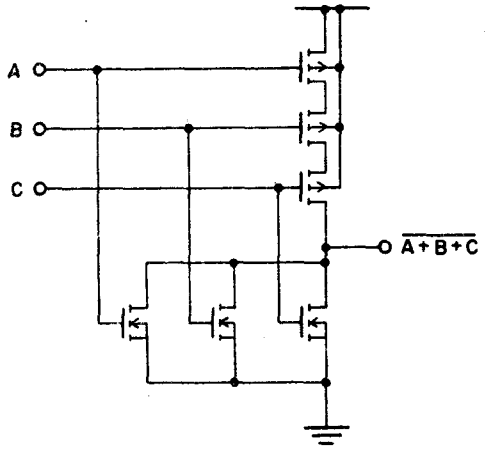

Fig. 1.10 NOR function – CMOS.

As already noted, bipolar transistors are better at handling high currents and so bipolar technologies usually offer higher speed. Examination of the technology shows, however, that MOS components can be diffused closer together and intrinsically smaller. This is because bipolar transistors need to be isolated from each other while groups of MOS can be diffused together. Also the diffusion windows in bipolars need aligning with each other while many of the MOS processes are self-aligning. MOS structures therefore have lower capacitance, and can operate at lower currents for a given speed. This is no real advantage where simple circuits are concerned because the major component of capacitance is in the external circuit which is connected to it. As circuits become more complex the internal capacitance becomes more important and MOS becomes a better choice for high speed.

The MOS circuit described above using both p- and n-channel transistors is termed *Complementary MOS*, or CMOS for short. The other main advantages of CMOS are the higher noise immunity inherent in the gate design – CMOS switches virtually between the two power rail voltage levels – and more complex functions can be built into the same area of silicon because of the higher packing density of MOS transistors. On the bipolar side are the capacity to make the absolutely fastest circuits, at the cost of high power consumption, and greater robustness, because MOS transistors are susceptible to relatively low static electricity voltages on their input gate oxide.

1.3 CUSTOM LOGIC CIRCUITS

1.3.1 Microprocessors

The first integrated circuits were only simple functions capable of containing a single logic equation. Attempts to make larger circuits failed because the silicon