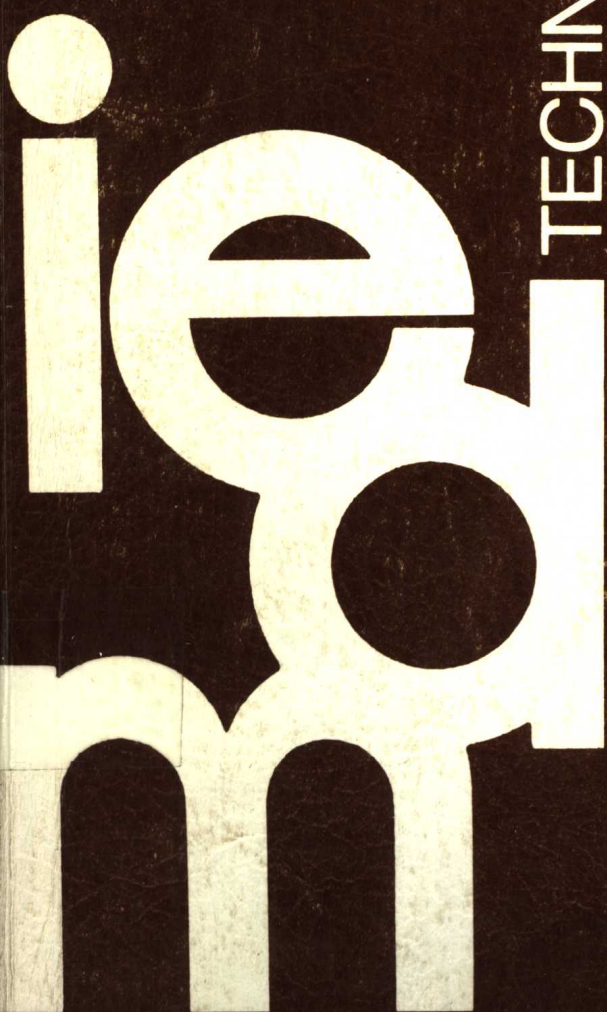


international
**ELECTRON
DEVICES**
meeting

1998

SAN FRANCISCO, CA
DECEMBER 6–9, 1998

TECHNICAL DIGEST



1998 International Electron Devices Meeting TECHNICAL DIGEST

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WELCOME FROM THE GENERAL CHAIR

The Conference Committee and I welcome you to the 1998 IEEE International Electron Devices Meeting. This year the conference returns to San Francisco and continues a 44-year tradition as the premier forum for the presentation of the latest research and development in the area of electron devices and their applications. The strong international nature of our industry and the broad range of topics are evident with invited speakers and contributed papers from major semiconductor centers from around the world. Over 660 abstracts were submitted from 30 countries. The total number of accepted abstracts was 240.

This year we are introducing a new feature to the IEDM. Two special sessions will feature invited speakers and regular papers on device manufacturing issues. We are continuing two features to improve accessibility to the information in the IEDM abstracts. We have included 50 word abstracts on the IEDM home page which are available now (please visit our site at <http://www.ieee.org/conference/iedm>). We are also providing the digest in a CD-ROM version that will be distributed along with the technical digest.

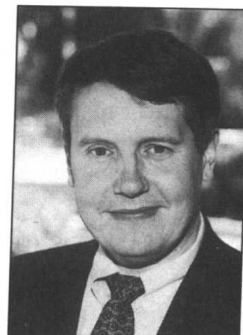
Two short courses are scheduled for Sunday. These are designed for broad appeal to the IEDM participants including those unfamiliar with the topics. The courses are entitled "Reliability for Logic and Memory Technologies" and "Next Generation TCAD: Models and Methods." These courses have been organized and will be presented by active researchers who are experts in these fields.

The plenary talks on Monday will feature presentations on semiconductor process equipment, system on a chip and electronics for communications. Speakers from North America, Europe and Asia will be featured.

The IEDM Luncheon speaker this year will be Dr. Yoshio Nishi, senior vice-president and director of research and development of Texas Instruments. He will be speaking on "Technology Development Trends in the Next Millennium." This talk will address the trends in semiconductor technology development. I recommend that you not miss it.

On Tuesday night, panel sessions are planned on two important and potentially controversial topics: "Do Copper and Low-K Solve All of Our Interconnect Related Problems?" and "Front-End Processing: Scaling Challenges for Nanometer Transistors."

On behalf of the IEEE Electron Devices Society, which sponsors the IEDM, Gary Bronner, Technical Program Chair and Mark Law, Technical Program Vice Chair, I wish to express my sincere appreciation and congratulations to the members of the IEDM committee for the outstanding job they have done in planning and organizing the 1998 meeting. The authors are to be commended for their efforts in preparing and presenting the high-quality papers that form the foundation of the IEDM. It is with great pleasure that I extend a warm welcome to them and to all the attendees of the 1998 IEEE International Electron Devices Meeting.



Pierre Woerlee
General Chair



Gary Bronner
Technical Program
Chair



Mark Law
Technical Program
Vice Chair

001676

AWARD PRESENTATIONS

PLENARY SESSION

Monday, December 7

1997 Roger A. Haken Best Student Paper Award

To: Felix Mayer, ETH Hoenggerberg, Zurich, Switzerland
For the paper entitled: Single-Chip CMOS Anemometer

Paul Rappaport Award

To: Isabel Y. Yang, Carlin J. Vieri, Anantha P. Chandrakasan and Dimitri A. Antoniadis
For the paper entitled: Back-Gated CMOS on SOIAS for Dynamic Threshold Voltage Control

EDS Chapter of the Year Award

To: ED/MTT India Chapter
ED/CPMT/R Singapore Chapter
"To an EDS chapter based on the quantity and quality of the activities and programs implemented by the chapter."

EDS Distinguished Service Award

To: W. Dexter Johnston, Jr.
"To recognize and honor outstanding service to the Electron Devices Society"

J. J. Ebers Award

To: B. Jayant Baliga
"For fundamental and sustained contributions to power semiconductors"

1998 IEEE Jack A. Morton Award

To: Isamu Akasaki, Meijo University, Nagoya, Japan and Shuji Nakamura, Nichia Chemical Industries, Ltd., Tokushima, Japan
"For contributions in the field of group-III nitride materials and devices"

IEDM LUNCHEON

Tuesday, December 8

1998 IEEE Clelio Brunetti Award

To: Roger T. Howe, University of California, Berkeley, CA and Richard S. Muller, University of California, Berkeley, CA
"For leadership and pioneering contributions to the field of microelectromechanical systems"

1998 IEEE David Sarnoff Award

To: Dr. Tatsuo Izawa, Nippon Telegraph and Telephone Corporation, Kanagawa, Japan
"For contributions to vapor phase axial deposition for optical fiber fabrication"

LUNCHEON PRESENTATION

"Technology Development Trends in the Next Millennium", a presentation by Dr. Yoshio Nishi, Texas Instruments

CONFERENCE HIGHLIGHTS

<u>Date</u>	<u>Time</u>	<u>Room</u>	<u>Event</u>
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12/7	9:00 a.m. – 12:00 p.m.	Cont'l Ballroom 1-9	Plenary Session
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12/8	12:20 p.m. – 2:00 p.m.	Grand Ballroom B	Luncheon
12/9	8:00 p.m. – 10:00 p.m.	Continental Ballroom 1-4 and 6-9	Panel Sessions

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Fumio Ootsuka, Hitachi, Ltd.

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- 8.1 A High Performance 180 nm Generation, Logic Technology**, S. Yang, S. Ahmed, B. Arcot, R. Arghavani, P. Bai, S. Chambers, P. Charvat, R. Cotner, R. Gasser, T. Ghani, M. Hussein, C. Jan, C. Kardis, J. Maiz, P. McGregor, B. McIntyre, P. Nguyen, P. Packan, I. Post, S. Sivakumar, J. Steigerwald, M. Taylor, B. Tufts, S. Tyagi and M. Bohr, Intel Corporation, Hillsboro, OR **197**

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Paul Heremans, IMEC

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- 9.1 30-nm-Gate InAlAs/InGaAs HEMTs Lattice-Matched to InP Substrates**, T. Suemitsu, T. Ishii, H. Yokoyama, Y. Umeda, T. Enoki, Y. Ishii and T. Tamamura, NTT Laboratories, Kanagawa, Japan **223**

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- 9.2 Improvement of DC, Low Frequency and Reliability Properties of InAlAs/InGaAs InP-Based HEMTs by Means of an InP Etch Stop Layer**, G. Meneghesso, D. Buttari, E. Perin, C. Canali* and E. Zanoni, University of Padova, Padova, Italy and *University of Modena, Modena, Italy **227**

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Tsu Jae King, University of California

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- 10.5 Improved Stability of Polysilicon Thin-Film Transistors Under Self-Heating and High Endurance EEPROM Cells for Systems-On-Panel**, J. Lee, N. Lee, H. Chung and C. Han, KAIST, Taejeon, Korea **265**

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Anthony Walton, University of Edinburgh

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- 11.5 A Fast 3D Modeling Approach to Parasitics Extraction of Bonding Wires for RF Circuits**, X. Qi, C. Yue, T. Arnborg*, H. Soh, Z. Yu, R. Dutton and H. Sakai, Stanford University, Stanford, CA and *Ericsson Components AB, Kista, Sweden 299

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Johann Alsmeyer, Siemens

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Michel Le Contellec, CNET/France Telecom

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Simon Deleonibus, LETI

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Co-Chairs: Olof Engstrom, Chalmers University of Technology
Gary Fedder, Carnegie Mellon University

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- 17.6 In-Plane Sensitive Vertical Trench-Hall Device**, R. Steiner, F. Kroener, Th. Olbrich*, R. Baresch* and H. Baltes, ETH Zurich, Zurich, Switzerland and *Austria Mikro Systeme International AG, Unterpremstaetten, Austria 479

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Co-Chairs: Paul Packan, Intel Corp.
Scott Dunham, Boston University

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- 18.2 Predictive Simulation of Transient Activation Processes in Boron-Doped Silicon Structures**, A. Lilak, M. Law, K. Jones, M. Giles*, E. Andideh*, M. Caturla**, T. Diaz de la Rubia**, J. Zhu** and S. Theiss**, University of Florida, Gainesville, FL and *Intel Corp., Santa Clara, CA and **Lawrence Livermore Nat'l Labs, Livermore, CA 493

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- 18.5 Modeling Solid Source Boron Diffusion for Advanced Transistor Applications**, P. Packan, S. Thompson, E. Andideh, S. Yu, T. Ghani, M. Giles, J. Sandford and M. Bohr, Intel Co., Hillsboro, OR 505

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- 18.6 A Calibrated Model for Trapping of Implanted Dopants at Material Interface During Thermal Annealing**, Y. Oh and D. Ward, Avant! Corp., Fremont, CA 509

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Co-Chairs: Robert Pezzani, SGS Thomson Microelectronics
Dietrich Vook, Hewlett Packard

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- 19.1 Progress in RF Inductors on Silicon—Understanding Substrate Losses (Invited)**, J. Burghartz, IBM Research Division, Yorktown Heights, NY 523

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- 19.2 Application of a New Circuit Design Oriented Q Extraction Technique to Inductors in Silicon ICs**, T. Chen, K. Kim and K. O., University of Florida, Gainesville, FL 527

3:10 p.m.

- 19.3 Modeling and Characterization of On-Chip Transformers**, S. Mohan, C. Yue, M. Hershenson, S. Wong and T. Lee, Stanford University, Stanford, CA 531

3:35 p.m.

- 19.4 A Novel Buried Oxide Isolation for Monolithic RF Inductors on Silicon**, H. Erzgräber, T. Grabolla, H. Richter, P. Schley and A. Wolff, Institute for Semiconductor Physics, Frankfurt, Germany 535

4:00 p.m.

- 19.5 On-Chip Spiral Inductors with Diffused Shields Using Channel-Stop Implant**, T. Yoshitomi, Y. Sugawara, E. Morifuji, T. Ohguro, H. Kimijima, T. Morimoto, H. Momose, Y. Katsumata and H. Iwai, Toshiba Corp., Kawasaki, Japan 540

4:25 p.m.

- 19.6 High-Performance Electroplated Solenoid-Type Integrated Inductor (SI²) for RF Applications Using Simple 3D Surface Micromachining Technology**, J. Yoon, B. Kim, C. Han, E. Yoon, K. Lee and C. Kim, KAIST, Taejeon, Korea 544

4:50 p.m.

- 19.7 Novel High-Q Bondwire Inductor for MMIC**, Y. Lee, S. Yun and H. Lee, Ajou University, Suwon, Korea 548

Session 20: CMOS Devices and Reliability—MOS Physics and Characterization 553

Tuesday, December 8, 2:15 p.m.

Continental Ballroom 6–9

Co-Chairs: Jurriaan Schmitz, Philips Research Labs
Kaizad Mistry, Intel Corp.

2:20 p.m.

- 20.1 Two-Dimensional Dopant Profiling of a 60nm Gate Length nMOSFET using Scanning Capacitance Microscopy**, W. Timp, M. O'Malley, R. Kleiman and J. Garino, Bell Labs, Lucent Technologies, Murray Hill, NJ 555

2:45 p.m.

- 20.2 Direct Measurement of L_{eff} and Channel Profile in MOSFETs Using 2-D Carrier Profiling Techniques**, P. DeWolf, R. Stephenson, S. Biesemans, P. Jansen, G. Badenes, K. DeMeyer* and W. Vandervorst*, IMEC, Leuven, Belgium 559

3:10 p.m.

- 20.3 A New Evaluation Method of Plasma Process-Induced Si Substrate Damage by the Voltage Shift Under Constant Current Injection at Metal/Si Interface**, K. Egashira, K. Eriguchi and S. Hashimoto, Matsushita Electronics Corp., Kyoto, Japan 563

3:35 p.m.

- 20.4 Direct Detecting of Dynamic Floating-Body Effects in SOI Circuits by Backside Electron Beam Testing**, E. Yoshida, T. Koyama, S. Maeda, Y. Yamaguchi, J. Komori and Y. Mashiko, Mitsubishi Electric Corp., Hyogo, Japan 567

4:00 p.m.

- 20.5 Remote Charge Scattering in MOSFETs with Ultra-Thin Gate Dielectrics**, M. Krishnan, Y. Yeo, Q. Lu, T. King, J. Bokor and C. Hu, University of California, Berkeley, CA 571

4:25 p.m.

- 20.6 Importance of Si-N Atomic Configuration at the Si/Oxynitride Interfaces on the Performance of Scaled MOSFETs**, M. Takayanagi-Takagi and Y. Toyoshima, Toshiba Corp., Yokohama, Japan 575

4:50 p.m.

- 20.7 Experimental Signature and Physical Mechanisms of Substrate Enhanced Gate Current in MOS Devices**, D. Esseni and L. Selmi, University of Bologna, Bologna, Italy 579

Session 21: Device Interconnect Technology—Gate Dielectrics 583

Tuesday, December 8, 2:15 p.m.

Imperial Room

Co-Chairs: Goncal Badenes, IMEC
Akihiko Ishitani, ASET

2:20 p.m.

- 21.1 Sub-5nm Multiple-Thickness Gate Oxide Technology Using Oxygen Implantation**, Y. King, C. Kuo, T. King and C. Hu, University of California at Berkeley, Berkeley, CA 585

2:45 p.m.

- 21.2 Multiple Gate Oxide Thickness for 2GHz System-On-A-Chip Technologies**, C.T. Liu, Y. Ma*, M. Oh*, P. W. Diodato, K. R. Stiles*, J. R. McMacken*, F. Li*, C. Chang, K. Cheung, J. Colonell, Y. Lai, R. Liu, E. Lloyd, J. Miner, C. Pai, H. Vaidya, J. Frackoviak, A. Timko, F. Klemens, H. Maynard and J. Clemens, Bell Labs, Lucent Technologies, Murray Hill, NJ and *Orlando, FL 589

3:10 p.m.

- 21.3 Radical Oxygen (O*) Process for Highly-Reliable SiO₂ with Higher Film-Density and Smoother SiO₂/Si Interface**, M. Nagamine, H. Itoh, H. Satake and A. Toriumi, Toshiba Corp., Yokohama, Japan 593

3:35 p.m.

- 21.4 Impact of Nitridation Engineering on Microscopic SILC Characteristics of Sub-10-nm Tunnel Dielectrics**, T. Ogata, M. Inoue, T. Nakamura*, N. Tsuji, K. Kobayashi, K. Kawase, H. Kurokawa, T. Kaneoka, Y. Ohno and H. Miyoshi, Mitsubishi Electric Corp., Hyogo, Japan and *Ryoden Semiconductor System Engineering Corp., Hyogo, Japan 597

4:00 p.m.

- 21.5 Antenna Device Reliability for ULSI Processing**, S. Krishnan, A. Amerasekera, S. Rangan and S. Aur, Texas Instruments, Dallas, TX 601

4:25 p.m.

- 21.6 Gate Quality Doped High K Films for CMOS Beyond 100nm: 3-10nm Al₂O₃ with Low Leakage and Low Interface States**, L. Manchanda, W. Lee, J. Bower, F. Baumann, W. Brown, C. Case, R. Keller, Y. Kim, E. Laskowski, M. Morris, R. Opila, P. Silverman, T. Sorsch and G. Weber, Bell Laboratories, Lucent Technologies, Murray Hill, NJ 605

4:50 p.m.

- 21.7 Ultra Thin High Quality Ta₂O₅ Gate Dielectric Prepared by In-situ Rapid Thermal Processing**, B. Wu, H. Luan, L. Kang, B. Kim, R. Vrtis*, D. Roberts* and D. Kwong, University of Texas, Austin, TX and *Schumacher, Carlsbad, CA 609

Session 22: CMOS Devices and Reliability—Advanced CMOS Devices and Technology 613

Tuesday, December 8, 2:15 p.m.

Grand Ballroom A

Co-Chairs: Suresh Venkatesan, Motorola
Tahir Ghani, Intel Corp.

2:20 p.m.

- 22.1 Progress Toward 10nm CMOS Devices**, G. Timp, K. Bourdelle, J. Bower, F. Baumann, T. Boone, R. Cirelli, K. Evans-Lutterodt, J. Garino, A. Ghetti, M. Green, H. Gossmann, D. Jacobson, Y. Kim, R. Kleiman, A. Kornblit, F. Klemens, C. Lochstampf, W. Mansfield, S. Moccio, D. Muller, M. O'Malley, L. Ocola, J. Rosamilia, J. Sapjeta, P. Silverman, T. Sorsch, W. Timp, D. Tennant and B. Weir, Bell Labs, Lucent Technologies, Murray Hill, NJ 615

2:45 p.m.

- 22.2 Accurate Characterization of Electron and Hole Inversion-Layer Capacitance and Its Impact on Low Voltage Operation of Scaled MOSFETs**, S. Takagi, M. Takayanagi-Takagi and A. Toriumi, Toshiba Corp., Yokohama, Japan 619

3:10 p.m.

- 22.3 A 1.2V, 0.1μm Gate Length CMOS Technology: Design and Process Issues**, M. Rodder, S. Hattangady, N. Yu, W. Shiau, P. Nicollian, T. Laaksonen, C. Chao, M. Mehrotra, C. Lee, S. Murtaza and S. Aur, Texas Instruments, Dallas, TX 623

3:35 p.m.

- 22.4 High-Performance Sub-0.08μm CMOS with Dual Gate Oxide and 9.7ps Inverter Delay**, M. Hargrove, S. Crowder, E. Nowak, R. Logan, L. Han, H. Ng, A. Ray, D. Sinitsky, P. Smeys, F. Guarin, J. Oberschmidt, E. Crabbé, D. Yee and L. Su, IBM SRDC, Hopewell Junction, NY 627

- 4:00 p.m.
22.5 A Study of Ultra Shallow Junction and Tilted Channel Implantation for High Performance 0.1 μ m PMOSFETs, K. Goto, M. Kase*, Y. Momiyama, H. Kurata, T. Tanaka, M. Deura, Y. Sanbonsugi and T. Sugii, Fujitsu Labs Ltd., Atsugi, Japan and *Fujitsu Ltd., Mie, Japan 631

- 4:25 p.m.
22.6 Channel Profile Engineering of 0.1 μ m-Si MOSFETs by Through-the-Gate Implantation, Y. Ponomarev, P. Stolk, A. van Brandenburg, R. Roes, A. Montree, J. Schmitz and P. Woerlee*, Philips Research Labs, Eindhoven, The Netherlands and *Philips Research Labs and University of Twente, Enschede, The Netherlands 635

- 4:50 p.m.
22.7 High Performance pMOSFET with BF₃ Plasma Doped Gate/Source/Drain and S/D Extension, J. Ha, J. Park, W. Kim, S. Kim, W. Song, H. Kim, H. Song, K. Fujihara, H. Kang, M. Lee, S. Felch*, U. Jeong*, M. Goeckner*, K. Shim***, H. Kim***, H. Cho***, Y. Kim***, D. Ko** and G. Lee**, Samsung Electronics Co., Ltd., Kyunggi-Do, Korea and *Varian Associates, Inc., Palo Alto, CA and **Yonsei University, Seoul, Korea and ***Varion Korea, Ltd., Kyumgki-Do, Korea 639

- 5:15 p.m.
22.8 A 1.9 μ m² Loadless CMOS Four-Transistor SRAM Cell in a 0.18 μ m Logic Technology, K. Noda, K. Matsui, K. Imai, K. Inoue, K. Tokashiki, H. Kawamoto, K. Yoshida, T. Takeda, N. Nakamura, T. Kimura, H. Toyoshima, Y. Koishikawa, S. Maruyama, T. Saitoh and T. Tanigawa, NEC Corp., Kanagawa, Japan 643

Session 23: 1998 IEDM Evening Panel Discussion 647

Tuesday, December 8, 8:00 P.M.
 Continental Ballroom 2-4

Front End Processing: Scaling Challenges for Nanometer Transistors

Panel Moderator: Steve Hillenius, Bell Labs, Lucent Technology

Session 24: 1998 IEDM Evening Panel Discussion 649

Tuesday, December 8, 8:00 p.m.
 Continental Ballroom 6-9

Do Copper And Low-K Solve All Of Our Interconnect Related Problems?

Panel Moderator: Shyam Murarka, RPI

Session 25: Quantum Electronics and Compound Semiconductors—Heterojunction Bipolar Transistors and Photodetectors 651

Wednesday, December 9, 9:00 a.m.
 Continental Ballroom 1

Co-Chairs: Hiroshi Ito, NTT
 Augusto Gutierrez-Aitken, TRW

- 9:05 a.m.
25.1 Advanced Performance of Small-Scaled InGaP/GaAs HBTs with f_T Over 150 GHz and f_{max} over 250 GHz, T. Oka, K. Hirata*, K. Ouchi, H. Uchiyama, T. Taniguchi, K. Mochizuki and T. Nakamura, Hitachi, Ltd., Tokyo, Japan and **Hitachi ULSI Systems, Tokyo, Japan 653

- 9:30 a.m.
25.2 Transferred-Substrate HBTs with 250 GHz Current-Gain Cutoff Frequency, D. Mensa, Q. Lee, J. Guthrie, S. Jaganathan and M. Rodwell, University of California, Santa Barbara, CA 657

- 9:55 a.m.
25.3 High-Gain GaInP/GaAs HBT Monolithic Transimpedance Amplifier for High-Speed Optoelectronic Receivers, S. Mohammadi, J. Park, D. Pavlidis, C. Dua*, J. Guyaux* and J. Garcia*, The University of Michigan, Ann Arbor, MI and *Thomson-CSF, Orsay, France 661

- 10:20 a.m.
25.4 Broadly-Tunable Narrow-Linewidth Micromachined Laser/Photodetector and Phototransistor, F. Sugihwo, C. Lin, L. Eyres, M. Fejer and J. Harris, Stanford University, Stanford, CA 665

- 10:45 a.m.
25.5 Failure Analysis of Travelling Wave MSM Distributed Photodetectors, A. Nespola, T. Chau*, M. Wu*, G. Ghione and C. Naldi, Politecnico di Torino, Torino, Italy and *University of California, Los Angeles, CA 669

- 11:10 a.m.
25.6 Investigation of the Space Charge Effect in the Quantum Well Infrared Photodetector, C. Kuan, Y. Hsu and M. Hsu, National Taiwan University, Taiwan, Rep. of China 673

Session 26: Solid State Devices—SiGe and High Power Devices 677

Wednesday, December 9, 9:00 a.m.
 Continental Ballroom 2-3

Co-Chairs: Akio Nakagawa, Toshiba
 Oh-Kyong Kwon, Hanyang University

- 9:05 a.m.
26.1 Lateral Thinking About Power Devices (LDMOS) (Invited), T. Efland, C. Tsai and S. Pendharkar, Texas Instruments, Dallas, TX 679

- 9:30 a.m.
26.2 A New Generation of High Voltage MOSFETs Breaks the Limit Line of Silicon, G. Deboy, M. März, J. Stengl, H. Strack, J. Tihanyi and H. Weber, Siemens AG, Munich, Germany 683

- 9:55 a.m.
26.3 A Lateral Insulated Gate Bipolar Transistor Employing the Self-Align Sidewall Implanted N⁺ Source, D. Byeon, B. Lee, D. Kim, M. Han, Y. Choi* and C. Yun, Seoul National University, Seoul, Korea and *Ajou University, Suwon, Korea 687

- 10:20 a.m.
26.4 Backside Laserprober Characterization of Thermal Effects During High Current Stress in Smart Power ESD Protection Devices, C. Fürbock, N. Seliger, D. Pogany, M. Litzenberger, E. Gornik, M. Stecher*, H. Gossner* and W. Werner*, TU Vienna, Vienna, Austria and *Siemens AG, Munich, Germany 691

- 10:45 a.m.
26.5 Breakdown and Low-Temperature Anomalous Effects in 6H SiC JFETs, G. Meneghesso, A. Bartolini, G. Verzellesi*, A. Cavallini**, A. Castaldini**, C. Canali*** and E. Zanoni, University of Padova, Padova, Italy and *University of Trento, Trento, Italy and **Univ. of Bologna, Bologna, Italy and ***Univ. of Modena, Modena, Italy 695

- 11:10 a.m.
26.6 SiGe Fast-Switching Power Diodes, A. Brown, G. Hurkx, H. Huizing, M. Peter, W. de Boer, J. van Berkum, P. Zalm, E. Huang* and N. Koper**, Philips Research Labs, Eindhoven, The Netherlands and *Philips Semiconductors, Stockport, United Kingdom and **Stadskanaal, The Netherlands 699

- 11:35 a.m.
26.7 Si/SiGe:C Heterojunction Bipolar Transistors in an Epi-Free Well, Single-Polysilicon Technology, D. Knoll, B. Heinemann, H. Osten, K. Ehwald, B. Tillack, P. Schley, R. Barth, M. Matthes, K. Park*, Y. Kim** and W. Winkler, Insitute. for Semiconductor Physics, Frankfurt, Germany and *Lucent Technology, Nurnberg, Germany and **Bell Labs, Lucent Tech, Murray Hill, NJ 703