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ICCC 82

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Foreword

On behalf of the Conference Committee we would like to extend a special welcome to the Second International Conference on Circuits and Computers—ICCC-82. The first conference, organized by Guy Rabbat and held at the Rye Town Hilton Inn in Port Chester, New York, was very successful. Several suggestions from that meeting have been incorporated into this year's conference.

History has shown that the complexity of ICs has doubled every 1½ to 2 years. This increase in complexity to include very large scale integrated (VLSI) and very high-speed integrated (VHSI) circuits supported by improved fabrication techniques has emphasized the need for new circuit architectures and revolutionary design and testing methods. In addition, the availability of these complex ICs has presented new challenges to system designers to efficiently utilize the expanded signal processing capability.

ICCC-82 highlights topics associated with development and application of VLSI circuits to large-scale systems. While several workshops and conferences emphasize many different aspects of VLSI circuits, this conference is the only conference sponsored jointly by the IEEE Computer Society and Circuits and Systems Society and emphasizes three interdependent areas that characterize emerging VLSI technology: semiconductor technology, CAD design systems, and computing technology.

We would like to express our appreciation to the Technical Program Committee for the outstanding conference program. The response to the call for papers was overwhelming. The committee had a monumental task in reducing the approximately five hundred abstracts submitted for consideration by about two-thirds. Although many good papers could not be included, the 140 papers contained in the program are intended to describe some of the latest and most important accomplishments in the field. The international character of the conference is emphasized by the fact that one-third of the papers in the technical program are from overseas.

Special thanks are also extended to the Mid-Hudson and New York Sections of IEEE for publicity, local arrangements and assistance with the visual aids presentations.

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Moderator

P. Losleben

DARPA/IPTO

"THE KEY TO HIGH PERFORMANCE PROCESSORS - PACKAGING"

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ABSTRACT

This paper reviews technology factors limiting performance in high end commercial processors. The discussion will include implications of GaAs and Josephson technologies as well as critical packaging parameters. The key factor will be shown to be packaging where the acceptable package must not only provide short time of flight delays but also adequate power distribution and cooling. The multi-level ceramic technology used in the IBM 3081 will be reviewed to illustrate how these requirements are satisfied with this technology.

INTRODUCTION

During the past 20 years we have seen rapid advances in the area of silicon technology. This has lead to the advent of significant "computer on a chip" products which have revolutionized the data processing industry [1]. This progress has also made possible the increase in high performance computer capability from clock cycles of 200 nanoseconds in the IBM 360/65 announced in April 1965 to a clock rate of 26 nanoseconds and more than a 20 times performance improvement (Figure 1) as announced in the IBM 3081 Model K in October of 1981.

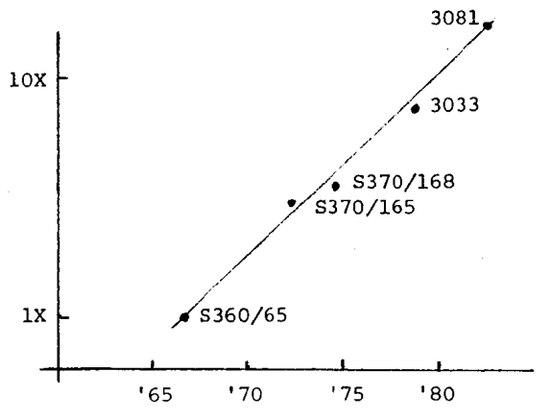

FIGURE 1 Relative Performance Trend

As we look to the future it's difficult to envision high end processors not being made up of large collections of individual chips which must be interconnected efficiently [2] so as to minimize time of flight delays while at the same time providing adequate power distribution and power dissipation capabilities [3]. The challenge will be primarily one of packaging technology rather than integrated circuit technology.

THE CHALLENGE

As a discussion reference, we shall use the IBM 3081 Model K which utilizes advanced silicon chip and packaging technologies. An analysis of the system delays based upon critical path analysis is given in Figure 2.

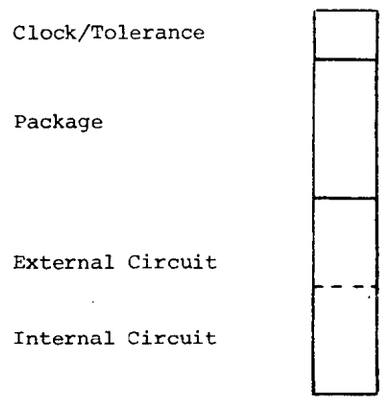

FIGURE 2 Path Delay Analysis

One way to increase MIPS is to reduce cycle time through improved technology. The second way is through system architectural improvements which reduce the effective number of machine cycles required for an average instruction to be executed - typically requiring more system hardware made possible by technology advances. In practice a combination of both approaches is used. For this paper dealing with technology, we will assume that the 50-100 MIP processor will require a cycle time reduction by a factor of 3-5 (i.e., less than a 10 nanosecond clock), and the challenge will be one of the package providing the adequate delay propagation, noise tolerances, voltage distribu-

tion and cooling.

INTERNAL CHIP DELAYS

The internal TTL chip circuits used in the 3081 have a worse case delay of 1.55 nanoseconds. Recently, ECL silicon circuits with quoted delays of 250 picoseconds [4] and LVI circuits with delays of 160 picoseconds have been reported [5]. Looking ahead to further silicon technology advances enables us to predict with confidence the availability of high performance silicon circuits with delays less than 100 picosecond and chips containing several thousand gates. With some 12 to 16 levels of logic this would represent less then a 3 nanosecond contribution to the clock cycle.

Data paths containing cache accesses are frequently "critical" paths for high performance processors. There is a great deal of attention given to designing fast access cache chips. In the 3081 Model K the chip used is a 1K x 3 chip with an access time of less than 12 nanoseconds and a power dissipation of approximately 3 watts. Unlike main memory where technology advances have been used to drive density but not performance, in the cache chip area technology advances are used to better performance. Chip densities will be rather modest by today's FET standards (1 to 4 Kb vs 16 to 64 Kb). Thus tomorrow's individual chips will be adequately fast but not very dense (16 Kb or less), and many chips will be required for a suitably large cache (64 KB or larger). Furthermore, these chips with their overall increased power dissipation must be adequately cooled and yet packaged sufficiently close together so as not to affect the total cache access time adversely.

What about Gallium Arsenide [6,7] and Josephson [8] technology with their very fast internal circuits? The key lies in figure 2 where one sees that reducing the internal chip delays has limited leverage at the system level. With the large R&D resources being devoted to silicon (and the resultant advances), the entry barrier for these technologies becomes higher each year. Furthermore, if the new technology is unable to offer a comparable level of integration to that of silicon, then additional chip to chip crossing delays will rapidly negate at the system level any improvement due to a faster technology at the chip level. If a non-silicon technology emerges, it will be for reasons other than fast internal circuit delays (e.g., packaging for Josephson [9]).

OFF CHIP DRIVER DELAYS

A serious problem with high end processors is the data paths within the processor are wide in order to optimize performance. This means that even at relatively high levels of integration (several thousand circuits per chip) one faces the requirement that each of these chips must have the capability to simultaneously drive wide data buses. The difficulty this poses is that simultaneous switching of these drivers can cause significant $L\Delta i/\Delta t$ voltage drop on the chip (where L is the inductance of the power distribution net, the Δi is the total driver current change, and Δt is the rise time of the driver output pulses). In the design of any high performance system, it is imperative that these "delta I" problems be accurately assessed; for example, even today in the 3081, this poses a serious design limitation - a limitation even with low inductance "C4" (Controlled Collapse Chip Connection [10]) solder interconnection pads (96 signal I/O and 25 power I/O on a 704 circuit logic chip in the 3081). This design constraint limited simultaneous switching from 18 to 22 driven in critical system nets as a result of the "delta I" problem.

The criticality of voltage drops (DC design parameters) and simultaneous switching noise (AC design parameters) must also be considered with the presence of reflection and coupled noise. The package must provide an effective medium for propagation of signals between two chips while guaranteeing sufficent tolerances (Figure 3) between quiet and active circuits. While wiring rules can manage reflective noise and simultaneous switching noise, since they do not occur at the same time, the package must provide the remaining tolerances [11].

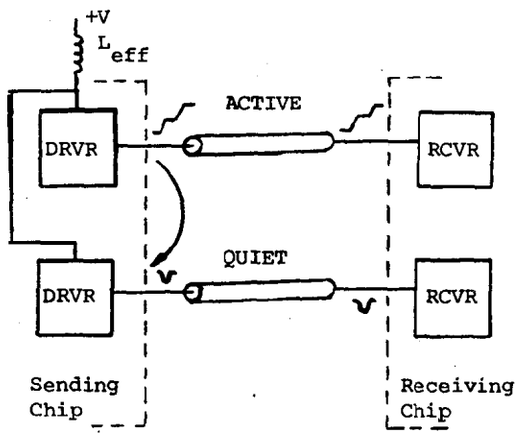

FIGURE 3 Signal Line Noise Sources

In looking ahead, the "delta I" problem becomes very severe. As the level of integration increases, the I/O requirement increases roughly as the 2/3 power of the number of circuits and the need for simultaneous switching increases proportionately. As pulse rise times decrease, the problem becomes more acute. In net, one can argue that there is a requirement for a 3-fold improvement at the package level associated with any VLSI performance improvement.

Referring back to Figure 2, reducing the external circuit delay proportionately with the other delay elements is perhaps the key problem to be addressed in advanced processors.

The classical answer to this problem is decoupling capacitors, and this solution has been proposed for the 3081 TCM package [12]. The difficulty with this answer lies in being able to place adequate capacitance sufficiently close to the switching circuits so they are not inductively decoupled at these frequencies.

PACKAGING

The Thermal Conduction Module (TCM) used in the 3081 provides a package which enables some 45,000 logic circuits (or equivalent cache bits) to be powered and cooled in a package only 90mm on a side. Each logic chip site offers an engineering change capability to provide rapid engineering change turn-around time during system bring-up. The close physical proximity of the chips provides for a very short delay associated with chip to chip signal propagation.

The TCM's 1800 pins (1200 of which are made available for signal interconnection) provide for wide band communication to other TCMs mounted on the integrated circuit package. Cooling capability is a maximum of 4 watts per chip allowing the total TCM to have a power dissipation capability of over 400 watts.

The present TCM, although adequate for its current application and providing for reasonable extendability, suffers from several limitations in terms of meeting long term requirements. One is the high dielectric constant associated with the alumina used in the TCM substrate. The high dielectric constant of alumina (Er $\cong$ 9) provides a delay penalty for signals propagating through the substrate. A lower dielectric constant such as is associated with glass ceramics (Er $\cong$ 5) is clearly desirable and could serve to reduce electrical delays while maintaining the same physical separation. The advisability of providing the decoupling capacitors [12], in close proximity to silicon chips is desirable perhaps even necessary to achieve the rise times required for future advanced processes. Enhanced top surface signal distribution systems utilizing thin film technology may also be needed to provide high performance chip environments. Larger substrates with more pins can also serve to minimize critical path crossings from one TCM to another.

It appears quite feasible to reduce the delay in Figure 2 associated with packaging. Higher chip levels of integration offer the potential for eliminating one chip crossing on average. The TCM improvements described above offer a further reduction. In net a factor of 2 and possibly 3 appear reasonable.

It is in the area of packaging that Josephson technology offers unique advantages [9].

The key problem is the low temperature requirement for super-conductivity and the difficulty this environment poses. Engineering is more difficult to do in liquid helium temperature (4°K) than at room temperature (e.g., testing, diagnostics, etc.). The packaging material problems are also non-trivial and the engineering work required to build a high performance processor is formidable.

INTEGRATED CIRCUITS PACKAGE

This advanced printed-circuit board serves to interconnect TCM's today in the 3081. It contains some six signal planes and some twelve power planes. There are also 19,200 connections on the board for interconnecting up to 9 TCMs [13].

Future requirements will be for better power distribution capability (already at several hundred amps) and closer effective TCM spacing to reduce delays.

To achieve the closer TCM spacing, the module shadow or sub-package images must be significantly improved. Since global wiring tracks and short pin-to-pin tracks do not affect interconnection spacing, input/output connector disposition must be improved to assist wire length distribution and wire conjestion [14].

TOLERANCES AND CLOCKS SKEW

An unwelcome but necessary contributor to system delay are tolerances and clocks skew. Historically through careful engineering they have tended to scale with cycle time, and it will be projected that this will continue to be the case.

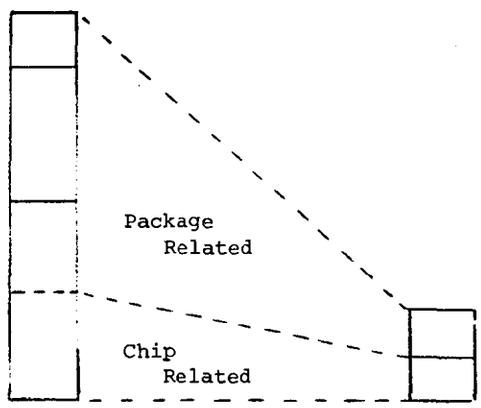

FIGURE 4 Required Technology Improvements

CONCLUSION

To satisfy these very high computing requirements, a factor of four reduction in delay must be achieved. This delay distribution - presumably available in this decade - is shown in Figure 4. The key to achieving this lies in packaging.

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