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SESSION 1

Plenary Session—Invited Papers

Monday, December 10, 1990 — 9:00 a.m.
Grand Ballroom

Chairman: Alfred C. Ipri
David Sarnoff Research Center

This year's plenary session consists of three exciting presentations that deal with diverse topics of Smart Power Technology, Optoelectronic Integrated Circuits and System Level Packaging.

The session begins with Professor Jayant Baliga from North Carolina State University who will present a paper entitled "Smart Power Technology: An Elephantine Opportunity." The presentation will begin with a description of the evolution of Smart Power and then go on to describe its impact on today's electronic systems. Structural and operational distinctions between MOSFETs used in power switching applications and logic circuits will be made. New power switches such as Insulated-Gate Bipolar Transistors (IGBTs) and MOS-Controlled Thyristors (MCTs) will also be described, as will their impact on various systems, such as motor drives and lighting ballasts.

Dr. Robert Leheny of Bellcore will next present a paper entitled "Optoelectronic Integrated Circuits." This is an emerging device technology designed to meet the future needs of telecommunications and the computing industry. This presentation will review the current status and future prospects of Opto-Electronic Integrated Circuits (OEICs) concentrating on such advantages as high reliability and performance, as well as potentially low cost. Problem areas associated with integrated components having very different materials and structural requirements, however, have presented formidable barriers to the demonstration of OEICs. Continuing advances in device design and fabrication technologies are, today, making substantial strides towards solving these problems.

The third paper, entitled "System Level Packaging An Alternative to Monolithic ULSI," will be presented by Professor R. Fabian Pease from Stanford University. System level packaging, at present, involves the use of multichip packages and high-density wire banding. Future approaches may involve silicon micromachining or superconducting chip-to-chip interconnects. The advantages of system level packaging over conventional chip packaging such as higher speed, lower power and lower cost are achieved through denser packaging and shorter chip-to-chip interconnect distances.

It is hoped that system level packaging will aid in stemming the spectacular increase in the cost of manufacturing monolithic ULSI.

NOTES

"SMART POWER TECHNOLOGY : An Elephantine Opportunity"
(INVITED PLENARY SESSION PAPER)

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ABSTRACT

Until recently, power devices have been a relatively small segment of the semiconductor industry. With the advent of MOS-gated power device technology, the option of creating a smart power technology has become viable. This paper provides a review of the evolution of smart power technology from bipolar discrete devices, through MOS-gated power devices, to the complex power integrated circuits that combine high voltage, high current devices with analog and digital circuits. The advent of smart power technology is expected to have a major impact on society via its application to computer power supplies, automotive electronics, appliance controls, and transportation systems.

INTRODUCTION

The roots of power semiconductor technology extend before those for integrated circuits. Since the invention of the bipolar transistor and the thyristor, there has been a strong motivation to increase the power handling capability of these discrete devices in order to extend their applications. The growth in the current and voltage handling capability of power thyristors over the last 35 years has been dramatic. It is impressive to note that by the 1990s, a single (monolithic) power thyristor made from a 100 mm diameter wafer is commercially available with the ability to block 6500 volts in the off-state and conduct over 2000 amperes in the on-state. Since each of these devices are fabricated out of an entire silicon wafer, the growth in the ratings of power thyristors has been determined by the availablity of high resistivity, large diameter, float-zone, silicon wafers. The sharp improvement in ratings acheived in the late 1970s can be directly linked to the development of neutron transmutation doping - a new method of doping silicon very uniformly by converting a silicon isotope to phosphorus by the absorption of thermal neutrons.

Over the years, the process technology for bipolar power devices lagged behind that developed for integrated circuits. These devices continued to be designed using design rules in the range of mil units. In addition, the junction depths used to fabricate these devices were maintained in the range of 10 to 100 microns to enable high voltage operation. Consequently, the process technology for power devices was significantly different from that used for integrated circuits. This situation changed due to the introduction of the power MOSFET in the 1970s and the advent of MOS/Bipolar devices in the 1980s.

MOS POWER DEVICES

The power MOSFET was first introduced commercially in the 1970s. When compared with the bipolar transistor, this device had the advantageous features of a high input impedance, high switching speed, ease of paralleling, and much superior safe-operating-area (SOA). This makes the power MOSFET attractive for many applications such as computer power supplies and automotive electronics.

The current rating of the power MOSFET is determined by the resistance within the device (1). The resistance can be reduced by making the channel length small, especially in the case of devices with blocking voltages below 100 volts. In the commercially available power DMOSFET structure, the channel length is controlled by adjusting the relative diffusion depth of the p-base and the N+ source regions. This allows the fabrication of devices with sub-micron channel length without the need to use advanced VLSI processing tools. However, it can be shown that the current distribution within the cell can be improved by reducing the size of the poly-silicon window by using VLSI technology (2). By scaling the DMOSFET geometry, the specific on-resistance (on-resistance per unit active area) has been reduced from 7 milli-ohm cm2 in 1970 to only 0.7 milli-ohm cm2 in 1990. In addition, the development of power MOSFETs with trench gate structures, based upon RIE processes used for DRAMs, have been explored resulting in devices with specific on-resistances as low as 0.3 milli-ohm cm2. The latter value is approaching the theoretical limit if 0.15 milli-ohm cm2 for a silicon device. For this reason, if further improvements are to be acheived, it will be necessary to embark upon the development of power devices based upon Silicon Carbide. Theoretical analysis indicates that the specific on-resistance can be reduced by over 100 times by replacing silicon with silicon carbide in the future (3).

Although the power MOSFET is well suited for applications where the blocking voltages are relatively low (less than 200 volts), its on-resistance increases rapidly with increase in the blocking voltage. Due to this phenomenon, it has not been possible to economically manufacture high voltage power MOSFETs with high current ratings. One solution to this problem was the invention of the Insulated Gate Bipolar Transistor (IGBT) (1). These devices have the same high input impedance feature of the power MOSFET and can operate at a current density of an order of magnitude larger than the power MOSFET. This makes them suitable for applications where the blocking voltage exceeds 200 volts, such as motor drives, appliance controls, robotics/numerical controls, etc.

The availability of the power MOSFET and the IGBT with their voltage controlled characteristics resulted in a tremendous simplification in the control circuit. This in turn created the opportunity for development of integrated gate drive circuits. In many applications, the power devices are used in a totem pole configuration. For this reason, the control circuit must be capable of performing level shifting to high voltages. The development of integrated control circuits also provided the impetus to incorporate protective circuits on the control chips against over-voltage, over-current, or over-temperature conditions. In addition, the need to interface with microprocessors led to the incorporation of logic circuits to provide encode/decode capability. This heralded the dawn of smart power technology in the 1990s.

SMART POWER TECHNOLOGY

In the broadest sense of definition, smart power technology provides the interface between the digital control logic and the power load (4-5). In its simplest form, it may consist of a level shifting and drive circuit that translates the logic level signals from a microprocessor to a voltage and current level sufficient to energize a load. An example of such a chip would be for display drives, where the load is usually capacitive in nature but requires drive voltages much greater than the operating voltage of logic circuits. On the other extreme, the smart power technology may be required to perform load monitoring, diagnostic functions, self-protection, and information feedback to the microprocessor, in addition to handling large amounts of power to actuate the load. An example of this is an automotive multiplexed bus system with distributed smart power modules for control of lights, motors, air-conditioning, etc.

A description of smart power technology can be made with the aid of Fig.1. Three fundamental functions that are performed with this technology are power control, sensing/protection, and interfacing. The basic components that are needed for the implementation of these functions are shown in this figure.

Power control is performed by using power devices and their drive circuits. It is the ability to handle high voltages, high currents, or a combination of both that makes smart power technology unique. The drive circuits are unusual in that they must be designed to operate at upto 30 volts to provide sufficient voltage to the gates of the power devices. In addition, for totem-pole operation, the drive circuit must be able to perform level shifting to high voltages. The regulation of power flow is performed by variety of power devices, with the MOS-gated devices being increasingly favored.

Smart power technology usually incorporates some form of sensor technology together with local feedback for protection of the IC. In addition to detecting the exceeding of a current, voltage, or temperature limit, the detection of a no-load or under-voltage condition is sometimes implemented. The under-voltage condition is useful to ensure sufficient biasing of the power devices to prevent excessive power dissipation during start-up. The current sensing is done with minimum power loss by partitioning a few cells from the power device and feeding this current to the control circuit. The protection of the IC is accomplished by using a feedback loop containing high frequency bipolar transistors. The response time of the feedback loop is critical to a benign shut-down because the system current increases at a very rapid rate during a fault. This portion of the smart power chip requires implementation of high performance analog circuits.

The interface function in the smart power IC is accomplished by using logic circuits, which perform the encode and decode operations. The chip must not only respond to signals received from a microprocessor but must be capable of sending messages regarding operating status, such as over-temperature shut-down, and information related to load monitoring, such as a no-load or short-circuit condition. This requires integration of high density CMOS circuits on the smart power chip. Due to the large voltage swings and high chip temperatures arising from self-heating, the design of the CMOS circuits for smart power chips can be quite challenging to ensure immunity from latch-up.

PROCESS TECHNOLOGY

Due to the relatively high cost of dielectrically isolated (DI) silicon wafers, most smart power chips are being fabricated using junction isolation (JI). If the cost of DI wafers can be reduced in the future, it is likely that most smart power chips will be made using DI due to simplification in design by the elimination of parasitics and the option of integrating multiple, MOS-Bipolar power devices. Meanwhile the challenges faced by designers today are the integration of analog and digital circuits on the same chip with high voltage and high current devices. This requires the use of a two-level metal process, in addition to the polysilicon gate electrode. A thin metal layer is used to fabricate the analog and digital circuits and the thick metal is used for the power devices. The need to bus high voltages around the chip also requires special metal cross-over design methodology where SIPOS layers are employed.

SMART POWER APPLICATIONS

Smart power chips are expected to have an impact on all areas in which power semiconductor devices are presently being used. The wide spectrum of voltages and currents over which power semiconductor devices are now being utilized is illustrated in Fig.2. On the one extreme are display drives that require relatively low currents and moderate voltages. These applications are already being served by smart power chips. On the other extreme lie traction (transportation systems) and High Voltage DC (HVDC) transmission which demand control of very high currents and voltages. The development of new MOS-Bipolar devices being researched at present could enable the penetration of smart power technology even to these applications. Meanwhile, a strong thrust is underway to create smart power chips for motor control, factory automation (robotics), computer power supplies, and automotive electronics. In many of these cases, application specific designs will be required putting pressure on the industry to create computer aided design (CAD) tools that can perform automated layout and mixed-mode circuit simulation at high voltages and currents.

CONCLUSIONS

Until recently, integrated circuit technology has been focussed primarily on chips for signal processing and data storage. This has resulted in a phenomenal capability for information processing that has led to the 'first electronic revolution'. This technology is akin to the brain in the human body, which assimilates data acquired via the senses and provides decision making capability. Although this technology has greatly enriched society, it has been hampered by the fact that in order to perform many functions, it is necessary to control significant amounts of energy being delivered to a variety of loads. Using the analogy of the human body, this is equivalent to the need for muscles to perform even the most basic tasks. The advent of smart power technology promises to create the 'second electronic revolution' by providing the brawn to complement the information processing capability.