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TECHNICAL DIGEST

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1990 International Electron Devices Meeting

TECHNICAL DIGEST

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TABLE OF CONTENTS

PLENARY SESSION: Invited Papers

Monday, December 10, 9:00 a.m.
Grand Ballroom

Chairman: A. Ipri, David Sarnoff Research Center

- 1.1 **SMART POWER TECHNOLOGY: AN ELEPHANTINE OPPORTUNITY**, B. Jayant Baliga, North Carolina State University, Raleigh, NC.
- 1.2 **OPTOELECTRONIC INTEGRATED CIRCUITS**, R. F. Leheny, Ballcore, Red Bank, NJ.
- 1.3 **SYSTEM LEVEL PACKAGING—AN ALTERNATIVE TO MONOLITHIC ULSI?** R. F. W. Pease, Stanford University, Stanford, CA.

Session 2: Solid State Devices—Advanced Si and SiGe Bipolar Devices

Monday, December 10, 1:00 p.m.
Grand Ballroom A

Co-Chairmen: J. Sturm, Princeton University
J. Tihanyi, Siemens

- 1:00 p.m.
Introduction
- 1:05 p.m.
2.1 **SiGe-Base Heterojunction Bipolar Transistors: Physics and Design Issues (Invited Paper)**, G. Patton, J. Stork, J. Comfort, E. Crabbe, B. Meyerson, D. Hareme and J. Sun, *IBM, Yorktown Heights, NY*
- 1:30 p.m.
2.2 **Base Transport in Near-Ideal Graded-Base Si/Si_{1-x}Ge_x/Si Heterojunction Bipolar Transistors from 150 K to 370 K**, E. Prinz and J. Sturm, *Princeton University, Princeton, NJ*
- 1:55 p.m.
2.3 **Low Temperature Operation of Si and SiGe Bipolar Transistors**, E. Crabbe, G. Patton, J. Stork, J. Comfort, B. Meyerson and J. Sun, *IBM, Yorktown Heights, NY*
- 2:20 p.m.
2.4 **Profile Leverage in a Self-Aligned Epitaxial Si or SiGe Base Bipolar Technology**, J. Comfort, G. Patton, J. Cressler, W. Lee, E. Crabbe, B. Meyerson, J. Sun, J. Stork, P. Lu, J. Burghartz, J. Warnock, K. Jenkins, K. Toh, M. D'Agostino, C. Stanis, and G. Scilla, *IBM, Yorktown Heights, NY*
- 2:45 p.m.
2.5 **Identification of 1/f Diffusion and Recombination Noise Sources in Bipolar Transistors**, S. Decoutere, L. Deferm, G. Vanhorebeek, C. Claeys and G. Declerck, *IMEC, Leuven, Belgium*
- 3:10 p.m.
2.6 **Charge Sharing Effects in Bipolar Transistors with Sub-half-micron Emitter Widths**, R. Dekker, R. Van Es, S. Jansen, P. Kranen, H. Maas, A. Pruijboom and J. Velden, *Philips Research Laboratories, Eindhoven, The Netherlands*
- 3:35 p.m.
2.7 **30 GHz Polysilicon-Emitter and Single-Crystal-Emitter Graded SiGe-Base PNP Transistors**, D. Hareme, J. Stork, B. Meyerson, E. Crabbe, G. Scilla, C. Stanis, A. Megdanis, G. Patton, J. Comfort, A. Bright, E. de Fresart, J. Johnson and S. Furkay, *IBM, Yorktown Heights, NY*

Session 3: Device Technology—Interconnect Materials and Structures for ULSI

Monday, December 10, 1:00 p.m.
Grand Ballroom B

Co-Chairmen: F. Neppl, Siemens AG
D. Verret, TI/SEMATECH

- 1:00 p.m.
Introduction

- 1 1:05 p.m.
3.1 **CVD Copper Metallurgy for ULSI Interconnection (Invited Paper)**, Y. Arita, N. Awaya, K. Ohno and M. Sato, *NTT LSI Laboratories, Kanagawa, Japan*
- 1:30 p.m.
3.2 **High Reliability Interconnections for ULSI Using Al-Si-Pd-Nb/Mo Layered Films**, J. Onuki, Y. Koubuchi, S. Fukada, M. Suwa, M. Koizumi, D. Gardner, H. Suzuki and E. Minowa, *Hitachi, Ltd., Ibaraki-ken, Japan*
- 1:55 p.m.
3.3 **A Scalable Submicron Contact Technology Using Conformal LPCVD TiN**, E. Travis, W. Paulson, F. Pintchovski, B. Boeck, L. Parrillo and K.-Y. Fu, *Motorola Inc., Austin, TX and M. Kottke, Motorola Inc., Mesa, AZ and M. Rice, J. Price and E. Eichman, Spectrum CVD, Inc., Phoenix, AZ*
- 2:20 p.m.
3.4 **Planarized Aluminum Metallization For Sub-0.5 μ m CMOS Technology**, F. Chen, Y. Lin, G. Dixit, R. Sundaresan, C. Wei and F. Liou, *SGS-Thomson Microelectronics, Dallas, TX*
- 2:45 p.m.
3.5 **VLSI Multilevel Micro-Coaxial Interconnects for High Speed Devices**, M. Thomas, I. Saadat and S. Sekigahama, *National Semiconductor, Santa Clara, CA*
- 3:10 p.m.
3.6 **High Density Dual-Active-Device-Layer(Dual)-CMOS Structure With Vertical Tungsten Plug-in Wirings**, K. Oyama, T. Kunio, R. Koh, Y. Hayashi, K. Kajiyana and K. Tsunenari, *NEC Corporation, Kanagawa, Japan*

Session 4: Solid State Devices—Advanced Device Characterization Techniques

Monday, December 10, 1:00 p.m.
Continental Ballroom 1-3

Co-Chairmen: K. Galloway, University of Arizona
S. Martin, Sandia National Laboratories

- 1:00 p.m.
Introduction
- 1:05 p.m.
4.1 **Relationship Between Mobility and Residual-Mechanical-Stress as Measured by Raman Spectroscopy for Nitrided-Oxide-Gate MOSFETs**, H. Momose, T. Morimoto, K. Yamabe and H. Iwai, *Toshiba Corporation, Kawasaki, Japan*
- 1:30 p.m.
4.2 **Extended (1.1-2.9 eV) Hot-Carrier Induced Photon Emission in n-Channel MOSFETs**, M. Lanzoni, E. Sangiorgi, C. Fiegna, M. Manfredi, and B. Ricco, *University of Bologna, Bologna, Italy*
- 1:55 p.m.
4.3 **Lateral Dopant Profiling in MOS Structures on a 100-nm Scale Using Scanning Capacitance Microscopy**, J. Slinkman, *IBM General Technology Division, Essex Jct., VT*; C. Williams, D. Abraham and H.K. Wickramasinghe, *IBM T.J. Watson Center, Yorktown Heights, NY*
- 2:20 p.m.
4.4 **Differential Capacitance Technique for Characterization of Hot Carrier Induced Degradation in p-Channel MOSFETs**, S. Kugelmass, Y. Shacham-Diamond and P. Krusius, *Cornell University, Ithaca, NY*
- 2:45 p.m.
4.5 **Lateral Distribution of Interface States in PMOSFETs**, J. Di-mauro and A. Henning, *Dartmouth College, Hanover, NH*
- 3:10 p.m.
4.6 **A New Charge Pumping Method For Determining the Spatial Interface State Density Distribution in MOSFETs**, X. Li and J. Deen, *Simon Fraser University, Burnaby, Canada*

Session 5: Integrated Circuits—Non-Volatile Memory

Monday, December 10, 1:00 p.m.
Continental Ballroom 4-5

Co-Chairmen: D. Guterman, SunDisk Corporation
J. Paterson, Texas Instruments

- 1:00 p.m.
Introduction
- 1:05 p.m.
5.1 A Novel Memory Cell Using Flash Array Contactless EPROM (FACE) Technology, B. Woo, T. Ong, A. Fazio, C. Park, G. Atwood, M. Holler, S. Tam and S. Lai, *Intel Corporation, Santa Clara, CA* 89
- 1:30 p.m.
5.2 Process and Device Technologies for 16Mbit EPROMs with Large-Tilt-Angle Implanted P-Pocket Cell, Y. Ohshima, S. Mori, Y. Kaneko, E. Sakagami, K. Yoshikawa, N. Hosokawa, *Toshiba Corporation, Kawasaki, Japan* and N. Arai, *Toshiba Microelectronics Corporation, Kawasaki, Japan* 91
- 1:55 p.m.
5.3 A Novel Method for the Experimental Determination of the Coupling Ratios in Submicron EPROM and Flash EEPROM Cells, R. Bez, E. Camerlenghi, D. Cantarelli, L. Ravazzi and G. Crisenza, *SGS-Thomson Microelectronics, Agrate Brianza, Italy* 95
- 2:20 p.m.
5.4 A $2.3\mu\text{m}^2$ Memory Cell Structure for 16Mb Nand EEPROMs, R. Shirota, R. Nakayama, R. Kirisawa, M. Momodomi, K. Sakui, Y. Itoh, S. Aritome, T. Endoh, F. Hatori and F. Masuoka, *Toshiba Corporation, Kawasaki, Japan* 103
- 2:45 p.m.
5.5 Charge Loss in EPROM due to Ion Generation and Transport in Interlevel Dielectric, G. Crisenza, G. Ghidini, S. Manzini, A. Modelli and M. Tosi, *SGS-Thompson Microelectronics, Agrate Brianza, Italy* 107
- 3:10 p.m.
5.6 A Reliable Bi-Polarity Write/ Erase Technology in Flash EEPROMs, S. Aritome, R. Shirota, R. Kirisawa, T. Endoh, R. Nakayama, K. Sakui, and F. Masuoka, *Toshiba Corporation, Kawasaki, Japan* 111
- 3:35 p.m.
5.7 A 5 Volt Only 16M Bit Flash EEPROM Cell with a Simple Stacked Gate Structure, N. Ajika, M. Ohi, H. Arima, T. Matsukawa, N. Tsubouchi, *Mitsubishi Electric Corporation, Hyogo, Japan* 115
- 4:00 p.m.
5.8 A Novel Sublithographic Tunnel Diode Based 5V-Only Flash Memory, M. Gill, R. Cleavelin, S. Lin, M. Middendorf, A. Nguyen, J. Wong, B. Huber, I. D'Arrigo, P. Shah, E. Kougiannos, P. Hefley, G. Santin and G. Naso, *Texas Instruments Inc., Houston, TX* 119
- 2:20 p.m.
6.4 Sub-picosecond Optical Pulse Generation at 350 GHz in Monolithic Passive CPM MQW Lasers, M. Wu, Y. Chen, T. Tanbun-Ek, R. Logan and M. Chin, *AT&T Bell Laboratories, Murray Hill, NJ* 137
- 2:45 p.m.
6.5 Quantum Calculation of the Performance of Travelling Wave Semiconductor Laser Amplifiers for Simultaneous Amplification and Detection, L. Thylen and M. Gustavsson, *Ericsson Telecom AB, Stockholm, Sweden*, T. Gustafson and I. Kim, *University of California, Berkeley, CA*, and A. Karlsson, *Royal Institute of Technology, Stockholm, Sweden* 141
- 3:10 p.m.
6.6 Reliable Operation of Lattice-Mis matched Indium Gallium Arsenide Photodetectors Grown on Silicon Substrates, G. Olsen, K. Woodruff, F. Speer, D. Rodefelf, V. Ban, G. Gasparian, D. Ackley, J. Hladkey, S. Mason and G. Erickson, *EPI-TAXX, Inc., Princeton, NJ*; J. Connolly and N. Dinkel, *David Sarnoff Research Center, Princeton, NJ* and S. Forrest, *University of Southern California, Los Angeles, CA* 145
- 3:35 p.m.
6.7 A High Sensitivity, High Bandwidth $\text{In}_{0.53}\text{Ga}_{0.47}\text{As/InP}$ Heterojunction Phototransistor, L. Leu, J. Gardner and S. Forrest, *University of Southern California, Los Angeles, CA* 149

Session 6: Quantum Electronics and Compound Semiconductors—Optoelectronic Devices

Monday, December 10, 1:00 p.m.
Continental Ballroom 6

Co-Chairmen: J. Campbell, University of Texas
T. Ikegami, NTT Opto-Electronic Laboratories

- 1:00 p.m.
Introduction
- 1:05 p.m.
6.1 Strained Layer Quantum Well Heterostructure Lasers (Invited Paper), J. Coleman, *University of Illinois, Urbana, IL* 125
- 1:30 p.m.
6.2 Low Threshold and Low Internal Loss 1.55- μm Strained-Layer Single Quantum Well Lasers, C. Zah, R. Bhat, K. Cheung, N. Andreadakis, S. Menocal, T. Wu, F. Favire, M. Koza, D. Hwang and T. Lee, *Bellcore, Red Bank, NJ* 129
- 1:55 p.m.
6.3 A 1.5 μm DFB Laser Array with a 1A° Channel Spacing Set by Monolithically Integrated Heaters, Y. Lo, W. Way, A. Gozdz, P. Lin, R. Bhat, C. Lin and T. Lee, *Bellcore, Red Bank, NJ* 133

Session 7: Vacuum Electronics—Vacuum Microelectronics

Monday, December 10, 1:00 p.m.
Continental Ballroom 7-9

Co-Chairmen: C. Spindt, SRI International
A. Shroff, Thomson Tubes Electronique

- 1:00 p.m.
Introduction
- 1:05 p.m.
7.1 RF Amplifiers Based on Vacuum Microelectronic Technology (Invited Paper), R. Parker, *Naval Research Laboratory, Washington, DC* 967
- 1:30 p.m.
7.2 Novel Silicon-Avalanche Diode as a Direct Modulated Cathode with Integrated Planar Electron-Optics, A. Hoeberechts, *Philips Research Laboratories, Eindhoven, The Netherlands* 155
- 1:55 p.m.
7.3 A Study of Field Emission Microtriodes, C. Holland, A. Rosengreen and C. Spindt, *SRI International, Menlo Park, CA* 979
- 2:20 p.m.
7.4 Field Emission from Submicron Emitter Arrays, M. Sokolich, E. Adler, R. Longo, D. Goebel and R. Benton, *Hughes Aircraft Company, Torrance, CA* 159
- 2:45 p.m.
7.5 Development Progress Toward the Fabrication of Vacuum Microelectronic Devices Using Conventional Solid Semiconductor Processing, S. Zimmerman, D. Colavito and W. Babie, *IBM, Hopewell Junction, NY* 163
- 3:10 p.m.
7.6 Porous Silicon Electron-Emitting Source, W. Yue, D. Parker and M. Weichold, *Texas A&M University, College Station, TX* 167
- 3:35 p.m.
7.7 1 to 25 GHz Vacuum FET Distributed Amplifier Analysis, H. Warren, E. Chou, T. Wiltsey, F. Wong and N. Luhmann Jr., *University of California, Los Angeles CA* 171

Session 8: Modeling and Simulation—Applied Device/Circuit Simulation

Monday, December 10, 1:00 p.m.
Imperial Ballroom

Co-Chairmen: J. Fossum, University of Florida
J. Chern, Texas Instruments, Inc.

- 1:00 p.m.
Introduction

1:05 p.m.	8.1 Modeling Advanced Bipolar Devices For High Performance Applications (Invited Paper) , R. Knepper, <i>IBM General Technology Division, Hopewell Junction, NY</i>	177
1:30 p.m.	8.2 Bipolar Circuit Reliability Simulation , D. Burnett, T. Horiuchi and C. Hu, <i>University of California, Berkeley, CA</i>	181
1:55 p.m.	8.3 Design Issues For Achieving Latchup-Free, Deep Trench-Isolated, Bulk, Non-Epitaxial, Submicron CMOS , S. Bhattacharya, S. Banerjee, J. Lee, A. Tasch and A. Chatterjee, <i>University of Texas, Austin, TX</i>	185
2:20 p.m.	8.4 Gate-Aided Drain to Field Breakdown of High Voltage NMOS Devices , A. Dumlao, R. Madurawe and T. McFarlane, <i>National Semiconductor Corporation, Santa Clara, CA</i>	189
2:45 p.m.	8.5 A New Efficient Method for the Transient Simulation of Three-Dimensional Interconnect Structures , S. Kumashiro, R. Rohrer and A. Strojwas, <i>Carnegie Mellon University, Pittsburgh, PA</i>	193
3:10 p.m.	8.6 Effects of the LDD Configuration on Capacitance Characteristics of Submicron MOSFETs , T. Smedes and F. Klaassen, <i>Eindhoven University of Technology, Eindhoven, The Netherlands</i>	197
3:35 p.m.	8.7 Complete Transient Simulation of Flash EEPROM Devices , S. Keeney and A. Mathewson, <i>NMRC, Cork, Ireland</i> , F. Piccinini, M. Morelli, C. Lombardi, R. Bez, D. Cantarelli, and L. Ravazzi, <i>SGS-Thomson Microelectronics, Agrate Brianza, Italy</i>	201
4:00 p.m.	8.8 Modeling and Simulation of the 16 Megabit Eprom Cell for Write/Read Operation with a Compact Spice Model , F. Gigon, <i>SGS-Thomson Microelectronics, Grenoble, France</i>	205
	Session 9: Solid State Devices—Advanced CMOS and BiCMOS Devices	209
	Tuesday, December 11, 9:00 a.m. <i>Grand Ballroom A</i> Co-Chairmen: D. Jackson, Digital Equipmen Corporation M. Taguchi, Fujitsu, Ltd.	
9:00 a.m.	Introduction	
9:05 a.m.	9.1 Design Optimization for Deep-Submicron CMOS Devices at Low Temperature Operation , M. Kakumu, D. Peters, H. Liu and K. Chiu, <i>Hewlett Packard Company, Palo Alto, CA</i>	211
9:30 a.m.	9.2 Reliability Design of p⁺-Pocket Implant LDD Transistors , C. Duvvury, T. Holloway, D. Paradis and A. Duong, <i>Texas Instruments Inc., Dallas, Texas</i>	215
9:55 a.m.	9.3 Accurate Characterizaion of Gate N- Overlapped LDD with the NEW Leff Extraction Method , J. Ida, S. Ishii and F. Ichikawa, <i>Oki Electric Industry Co., Ltd., Hachioji, Japan</i>	219
10:20 a.m.	9.4 Dependence of LDD Device Optimization on Stressing Parameters at 77K , M. Song, J. Cable, K. MacWilliams and J. Woo, <i>University of California, Los Angeles, CA</i>	223
10:45 a.m.	9.5 Suppression of Hot Carrier Effects by LGE (Laterally Graded Emitter) Structure in BiCMOS , H. Honda, Y. Ishigaki, K. Higashitani, M. Hatanaka, S. Nagao and N. Tsubouchi, <i>Mitsubishi Electric Corporation, Hyogo, Japan</i>	227
11:10 a.m.	9.6 Characterization of Speed and Stability of BiNMOS Gates with a Bipolar and PMOSFET Merged Structure , H. Momose, T. Maeda, K. Inoue, T. Kobayashi, Y. Urakawa and K. Maeguchi, <i>Toshiba Corporation, Kawasaki, Japan</i>	231
11:35 a.m.	9.7 Stacked-Nitride Oxide Gate MISFET with High Hot-Carrier-Immunity , H. Iwai, H. Momose, T. Morimoto, Y. Ozawa and K. Yamabe, <i>Toshiba Corporation, Kawasaki, Japan</i>	235
	Session 10: Device Technology—Advanced Silicide and Innovative Process Technologies	239
	Tuesday, December 11, 9:00 a.m. <i>Grand Ballroom B</i> Co-Chairmen: M. Bohr, Intel Corporation M. Ogirima, Hitachi, Ltd.	
9:00 a.m.	Introduction	
9:05 a.m.	10.1 A TiN Strapped Polysilicon Gate Cobalt Salicide CMOS Process , J. Pfister, T. Mele, Y. Limb, R. Jones, M. Woo, B. Boeck and C. Gunderson, <i>Motorola Inc., Austin, TX</i>	241
9:30 a.m.	10.2 Characterization of Lateral Dopant Diffusion in Silicides , C. Chu, K. Saraswat and S. Wong, <i>Stanford University, Stanford, CA</i>	245
9:55 a.m.	10.3 New Silicidation Technology by SITOX (Silicidation Through Oxide) and Its Impact on Sub-half Micron MOS Devices , H. Sumi, T. Nishihara, Y. Sugano, H. Masuya and M. Takasu, <i>Sony Corporation, Kanagawa, Japan</i>	249
10:20 a.m.	10.4 A Polycrystalline-Si₃Ge_{1-x}-Gate CMOS Technology , T. King, J. Shott, J. McVittie and K. Saraswat, <i>Stanford University, Stanford, CA and J. Pfister, Motorola, Inc., Austin, TX</i>	253
10:45 a.m.	10.5 A Deep-Submicron Isolation Technology with T-Shaped Oxide (TSO) Structure , T. Ishijima, E. Ikawa, T. Hamada, Y. Fujimoto and K. Terada, <i>NEC Corporation, Sagamihara, Japan</i>	257
11:10 a.m.	10.6 Self-Gettering and Proximity Gettering for Buried Layer Formation by MeV Ion Implantation , T. Kuroi, S. Komori, H. Miyatake and K. Tsukamoto, <i>Mitsubishi Electric Corp., Hyogo, Japan</i>	261
	Session 11: Detectors, Sensors and Displays—CCDs and Image Sensors	265
	Tuesday, December 11, 9:00 a.m. <i>Continental Ballroom 1-3</i> Co-Chairmen: J. Bosiers, Philips Research Laboratories C. Stancampiano, Eastman Kodak Company	
9:00 a.m.	Introduction	
9:05 a.m.	11.1 A Resistive-Gate Two-Phase 2DEG CCD for III-V IR Detectors , J.-I. Song, <i>Columbia University, New York, NY</i> and E.R. Fossum, <i>NASA/JPL, Pasadena, CA</i>	267
9:30 a.m.	11.2 Simulation, Design, and Fabrication of Thin-Film Resistive-Gate GaAs Charge Coupled Devices , N. Ula, G. Cooper, C. Davidson, S. Swierkowski and C. Hunt, <i>University of California, Davis CA</i>	271
9:55 a.m.	11.3 Hg-sensitized Photochemical Vapor Deposition Method Application to Hydrogenated Amorphous Silicon Photoconversion Layer Overlaid on CCD Imaging Device , H. Nozaki, N. Sakuma, T. Niiyama, H. Ihara, Y. Iida and N. Harada, <i>Toshiba Corporation, Kawasaki, Japan</i>	275
10:20 a.m.	11.4 Design and Implementaion of a 3D-LSI Character Recognition Image Sensor , K. Kioi, T. Shinozaki, S. Toyoyama, K. Shirakawa, K. Ohtake and S. Tsuchimoto, <i>Sharp Corporation, Nara, Japan</i>	279
10:45 a.m.	11.5 Submicron Spaced Lens Array Process Technology For a High Photosensitivity CCD Image Sensor , Y. Sano, T. Nomura, H. Aoki, S. Terakawa, H. Kodama, T. Aoki and Y. Hiroshima, <i>Matsushita Electronics Corporation, Kyoto, Japan</i>	283

- 11:10 a.m.
11.6 A Large Area 1.3 Megapixel Full-Frame CCD Image Sensor with a Lateral-Overflow Drain and a Transparent Gate Electrode, S. Kosman, E. Stevens, J. Cassidy, W. Chang, P. Roselle, W. Miller, B. Burkey, T. Lee, G. Hawkins, R. Khosla and M. Mehra, *Eastman Kodak Company, Rochester, NY* 287
- 11:35 a.m.
11.7 Amorphous Silicon Four-Quadrant Orientation Detector (FO-QUOD) for Application to Neural Network Image Sensors, W. Sah and S. Lee, *National Taiwan University, Taiwan, Republic of China* 291
- 10:45 a.m.
13.5 AlAs Etch-Stop Layers for InGaAlAs/InP Heterostructure Devices and Circuits, T. Broekaert and C. Fonstad, *Massachusetts Institute of Technology, Cambridge, MA* 339
- 11:10 a.m.
13.6 Quantum Effect of the Source Electrode on Electrical and Optical Characteristics of Double-Barrier Resonant Tunneling Structures, J. Wu, C. Lee, C. Chang, K. Chang, D. Liou and D. Liu, *National Chiao Tung University, Taiwan, Republic of China* 343

Session 12: Integrated Circuits—High Speed Integrated Circuits 295

Tuesday, December 11, 9:00 a.m.
Continental Ballroom 4-5

Co-Chairmen: P. Krusius, Cornell University
 J. Mikkelsen, Vitesse Semiconductor Corporation

- 9:00 a.m.
Introduction
- 9:05 a.m.
12.1 Sub-30ps ECL Circuits Using High-ft Si and SiGe Epitaxial Base SEEW Transistors, J. Burghartz, J. Comfort, G. Patton, J. Cressler, B. Meyerson, J. Stork, J. Sun, G. Scilla, J. Warnock, B. Ginsberg, K. Jenkins, K. Toh, D. Hareme and S. Mader, *IBM, Yorktown Heights, NY* 297
- 9:30 a.m.
12.2 35 GHz/35 psec ECL PNP Technology, J. Warnock, P. Lu, J. Cressler, K. Jenkins and J. Sun, *IBM, Yorktown Heights, NY* 301
- 9:55 a.m.
12.3 A 36GHz 1/8 Frequency Divider with GaAs BP-MESFETs, S. Nishi, H. Tsuji, H. Fujishiro, M. Shikata, K. Tanaka, *Okai Electric Industry Co., Ltd., Tokyo, Japan* 305
- 10:20 a.m.
12.4 A 11.7 GHz 1/8-Divider Using 43 GHz Si High Speed Bipolar Transistor with Photoepitaxially Grown Ultra-Thin Base, T. Yamazaki, I. Namura, H. Goto, A. Tahara and T. Ito, *Fujitsu Laboratories Ltd., Atsugi, Japan* 309
- 10:45 a.m.
12.5 A Bipolar-EPROM (Bi-EPROM) Structure for 3.3V Operation and High Speed Application, N. Matsukawa, K. Masuda, J. Miyamoto, *Toshiba Corp., Kawasaki, Japan* 313
- 11:10 a.m.
12.6 A Wide-Margin, Multiple-Fan-In NOR Gate for Josephson Decoder, P. Yuh, *Hypres, Inc., Elmsford, NY* 317

Session 13: Quantum Electronics and Compound Semiconductors—Novel Electronic Devices 321

Tuesday, December 11, 9:00 a.m.
Continental Ballroom 6

Co-Chairmen: M. Stroschio, ARO
 C.-E. Zah, Bellcore

- 9:00 a.m.
Introduction
- 9:05 a.m.
13.1 Microwave Performance of InGaAs/InAlAs Charge Injection Transistors, P. Mensz, H. Schumacher, P. Garbinski, A. Cho, D. Sivco and S. Luryi, *AT&T Bell Laboratories, Murray Hill, NJ* 323
- 9:30 a.m.
13.2 Optoelectronic Pulse Generation and Detection of 80 GBITS/S, Train, C. Shu, X. Zhang, E. Yang and D. Auston, *Columbia University, New York, NY* 327
- 9:55 a.m.
13.3 Improvements in the Heteroepitaxy of GaAs on Si by Incorporating a ZnSe Buffer Layer, M. Lee, R. Horng, D. Wu and P. Chen, *National Sun Yat-Sen University, Taiwan, Republic of China* 331
- 10:20 a.m.
13.4 Criteria for One-Dimensional Transport in Split-Gate Field-Effect Transistors, C. Eugster, J. del Alamo, P. Belk and M. Rooks, *Massachusetts Institute of Technology, Cambridge, MA* 335

- 11:35 a.m.
13.7 Sequential vs. Coherent Tunneling in Double-Barrier Diodes Investigated by Differential Absorption Spectroscopy, T. Woodward, D. Chemla and H. Barranger, *AT&T Bell Laboratories, Holmdel, NJ* and I. Bar-Joseph, *Weizmann Institute of Science, Rehovot, Israel*, and D. Sivco and A. Cho, *AT&T Bell Laboratories, Murray Hill, NJ* 959

Session 14: Modeling and Simulation—Advanced Physical Device Models 347

Tuesday, December 11, 9:00 a.m.
Continental Ballroom 7-9

Co-Chairmen: M. Fukuma, NEC Corporation
 B. Meinerzhagen, University of Aachen

- 9:00 a.m.
Introduction
- 9:05 a.m.
14.1 Unified Generation Model with Donor and Acceptor-Type Trap States for Heavily Doped Silicon, S. Voldman, T. Linton, J. Johnson and S. Titcomb, *IBM General Technology Division, Essex Junction, VT* 349
- 9:30 a.m.
14.2 An Efficient Non-Parabolic Formulation of the Hydrodynamic Model for Silicon Device Simulation, T. Bordelon, X. Wang, C. Maziar and A. Tasch, *The University of Texas, Austin, TX* 353
- 9:55 a.m.
14.3 A Unified Mobility Model for Device Simulation, D. Klaassen, *Philips Research Laboratories, Eindhoven, The Netherlands* 357
- 10:20 a.m.
14.4 Heavy-Doping Transport Parameter Set Describing Consistently the DC and AC Behavior of Bipolar Transistors, J. Popp, T. Meister, J. Weng and H. Klose, *Siemens AG, Munich, FRG* 361
- 10:45 a.m.
14.5 A Novel DC Measurement Method for the Accurate Extraction of Bipolar Resistive Parasitics, R. Taft and J. Plummer, *Stanford University, Stanford, CA* 365
- 11:10 a.m.
14.6 New Concept of Collector Design for 0.35 μ m BiCMOS Driver Based on a Base Pushout Model in the Presence of Velocity Overshoot, T. Fuse, T. Hamasaki, K. Matsuzawa, and S. Watanabe, *Toshiba Corporation, Kawasaki, Japan* 369

Session 15: Solid State Devices—Novel Device Structures 373

Tuesday, December 11, 2:15 p.m.
Grand Ballroom A

Co-Chairmen: H. Massoud, Duke University
 J.-P. Colinge, IMEC

- 2:15 p.m.
Introduction
- 2:20 p.m.
15.1 Ultra High Hole Mobility In Strain-Controlled Si-Ge Modulation-Doped FET, E. Murakami, K. Nakagawa, H. Etoh, A. Nishida and M. Miyao, *Hitachi, Ltd., Tokyo, Japan* 375
- 2:45 p.m.
15.2 A Si/SiGe Heterojunction Bipolar Transistor with Undoped SiGe Spacer for Cryo-BiCMOS Circuits, T. Yamazaki, K. Imai, T. Tashiro, T. Tatsumi, T. Niino and M. Nakamae, *NEC Corporation, Kanagawa, Japan* 379
- 3:10 p.m.
15.3 Carrier Confinement in MOS-Gated $\text{Ge}_{1-x}\text{Si}_x$ /Si Heterostructures, P. Garone, V. Venkataraman and J. Sturm, *Princeton University, Princeton, NJ* 383

- 3:35 p.m.
15.4 Si Resonance Transport Device, E. Takeda, H. Matsuoka T. Yoshimura and T. Ichiguchi, *Hitachi Ltd., Tokyo, Japan* **387**
- 4:00 p.m.
15.5 A Novel Source-to-Drain Nonuniformly Doped Channel (NUDC) MOS-FET for High Current Drivability and Threshold Voltage Controlability, Y. Okumura, M. Shirahata, T. Okudaira, A. Hachisuka, H. Arima, T. Matsukawa and N. Tsoubouchi, *Mitsubishi Electric Corporation, Hyogo, Japan* **391**

- 4:25 p.m.
15.6 A Novel CMOS-Compatible Lateral Bipolar Transistor for High-Speed BICMOS LSI, A. Tamba, T. Someya, T. Sakagami, N. Akiyama and Y. Kobayashi, *Hitachi Ltd., Ibaraki, Japan* **395**
- 4:50 p.m.
15.7 Analysis of Submicron Double-Gated Polysilicon MOS Thin Film Transistors, A. Adan, S. Ono, H. Shibayama and R. Miyake, *SHARP Corporation, Nara, Japan* **399**

Session 16: Device Technology—Advanced Surface Preparation in Thin Dielectric Technologies **403**

Tuesday, December 11, 2:15 p.m.

Grand Ballroom B

Co-Chairmen: K. Hashimoto, Toshiba Corporation
 T. Russell, NIST

- 2:15 p.m.
Introduction
- 2:20 p.m.
16.1 Enhanced Degradation of Oxide Breakdown in the Peripheral Region by Metallic Contamination, H. Uchida, I. Aikawa, N. Hirashita and T. Ajioka, *Oki Electric Industry Co., Ltd., Tokyo, Japan* **405**

- 2:45 p.m.
16.2 Dry Cleaning Procedure for Silicon IC Fabrication, J. Ruzyllo and D. Frystak, *Penn State University, University, PA*, R. Bowling, *Texas Instruments, Dallas, TX* **409**

- 3:10 p.m.
16.3 Novel Dry Cleaning Using Trisilane with a New Single-Wafer Reactor, F. Mieno, H. Miyata, A. Tsukune, Y. Furumura, and H. Tsuchikawa, *Fujitsu Ltd., Kawasaki, Japan* **413**

- 3:35 p.m.
16.4 Endurance Properties of Ferroelectric PZT Thin Films, R. Moazzami and C. Hu, *University of California, Berkeley, CA*, and W. Shepherd, *National Semiconductor, Santa Clara, CA* **417**

- 4:00 p.m.
16.5 Electrical and Reliability Characteristics of Ultrathin Oxynitride Gate Dielectric Prepared by Rapid Thermal Processing in N₂O, H. Hwang, W. Ting, D. Kwong and J. Lee, *University of Texas, Austin, TX* **421**

- 4:25 p.m.
16.6 High Performance Dual-gate Sub-halfmicron CMOSFETs with 6 nm-thick Nitrided SiO₂ Films Formed in an N₂O Ambient, A. Uchiyama, H. Fukuda, T. Hayashi, T. Iwabuchi and S. Ohno, *Oki Electric Industry Co., Ltd., Tokyo, Japan* **425**

- 4:50 p.m.
16.7 Effects of Boron Penetration and Resultant Limitations in Ultra Thin Pure-Oxide and Nitrided-Oxide Gate-Films, T. Morimoto, H. Momose, Y. Ozawa, K. Yamabe and H. Iwai, *Toshiba Corporation, Kawasaki, Japan* **429**

Session 17: Modeling and Simulation—Monte Carlo Simulation **433**

Tuesday, December 11, 2:15 p.m.

Continental Ballroom 1-3

Co-Chairmen: D. Frank, IBM T. J. Watson Research Center
 C. Maziar, University of Texas

- 2:15 p.m.
Introduction

- 2:20 p.m.
17.1 Overshoot in Transient and Steadystate GaAs, InP, Ga_{0.47}In_{0.53}As and InAs Bipolar Transistors, S. Tiwari, M. Fischetti and S. Laux, *IBM, Yorktown Heights, NY* **435**

- 2:45 p.m.
17.2 Transient and Steady-State Monte-Carlo Simulation of the Effects of Junction Grading on Carrier Transport in InAlAs/InGaAs HBTs, J. Hu, D. Pavlidis and K. Tomizawa, *The University of Michigan, Ann Arbor, MI* **439**

- 3:10 p.m.
17.3 Monte Carlo Simulation of Gunn Domain Dynamics in Power GaAs MESFETs with a Recessed Gate Structure, M. Kuzuhara, T. Itoh and K. Hess, *NEC Corporation, Kawasaki, Japan* **443**

- 3:35 p.m.
17.4 MOSFET Hot Electron Gate Current Calculation by Combining Energy Transport Method with Monte Carlo Simulation, S.-L. Wang, N. Goldsman, L. Henrickson and J. Frey, *University of Maryland, College Park, MD* **447**

- 4:00 p.m.
17.5 Efficient Non-Local Modeling of the Electron Energy Distribution in Sub-Micron MOSFETs, C. Fiegna, F. Venturi, E. Sangiorgi and B. Ricco, *University of Bologna, Bologna, Italy* **451**

- 4:25 p.m.
17.6 Hot-Holes Generation and Transport in n-MOSFETs: A Monte Carlo Investigation, F. Venturi, C. Fiegna, A. Abramo, E. Sangiorgi and B. Ricco, *University of Bologna, Bologna, Italy* **455**

- 4:50 p.m.
17.7 Modeling of Bias-Stress Dependent Transconductance Degradation of Submicron MOSFETs, S. Sugino, Z. Yu, F. Venturi and R.W. Dutton, *Stanford University, Stanford, CA* **459**

- 5:15 p.m.
17.8 The Impact of Non-Equilibrium Transport on Breakdown and Transit Time in Bipolar Transistors, E. Crabbe, J. Stork, G. Baccarani, M. Fischetti and S. Laux, *IBM, Yorktown Heights, NY* **463**

Session 18: Integrated Circuits—SRAM/BiCMOS Technology **467**

Tuesday, December 11, 2:15 p.m.

Continental Ballroom 4-5

Co-Chairmen: T. Dellin, Sandia National Laboratories
 R. de Werd, Philips Research Laboratory

- 2:15 p.m.
Introduction

- 2:20 p.m.
18.1 A Polysilicon Transistor Technology for Large Capacity SRAMs (Invited Paper), S. Ikeda, S. Hashiba, I. Kuramoto, H. Katoh, S. Ariga, T. Yamanaka, T. Hashimoto, N. Hashimoto and S. Meguro, *Hitachi, Ltd., Tokyo, Japan* **469**

- 2:45 p.m.
18.2 A 25 μm^2 Bulk Full CMOS SRAM Cell Technology with Fully Overlapping Contacts, R. Verhaar, R. Augur, C. Aussems, L. de Bruin, F. Op den Buijsh, L. Dingen, T. Geuns, W. Havermans, A. Montree, P. van der Plas, H. Pomp, M. Vertregt, R. de Werd, N. Wils and P. Woerlee, *Philips Research Laboratories, Eindhoven, The Netherlands* **473**

- 3:10 p.m.
18.3 A 5.9 μm^2 Super Low Power SRAM Cell Using A New Phase-Shift Lithography, T. Yamanaka, N. Hasegawa, T. Tanaka, K. Ishibashi, T. Hashimoto, A. Shimizu, N. Hashimoto, D. Sasaki, T. Nishida and E. Takeda, *Hitachi Ltd., Tokyo, Japan* **477**

- 3:35 p.m.
18.4 A High Performance 0.5 μm BiCMOS Triple Polysilicon Technology for 4Mb Fast SRAMs, T. Mele, J. Hayden, F. Walczyk, M. Lien, Y. See, D. Denning, S. Cosentino and A. Perera, *Motorola, Inc., Austin, TX* **481**

- 4:00 p.m.
18.5 Process Design for Merged Complementary BiCMOS, N. Roveto, S. Ogura, J. Acocella, K. Barnes, A. Dally, T. Yanagisawa, C. Ng, J. Burkhardt, E. Valsamakis, J. Hamers, T. Buti and C. Richwine, *IBM, Hopewell Junction, NY* **485**

- 4:25 p.m.
18.6 Low Voltage Performance of an Advanced CMOS/BiCMOS Technology Featuring 18GHz Bipolar FT and Sub-70ps CMOS Gate Delays, M. El-Diwan, M. Brassington, R. Razouk, P. v. Wijnen and V. Akylas, *Signetics, Sunnyvale, CA* **489**

4:50 p.m.

- 18.7 HSST/BiCMOS Technology with 26ps ECL and 45ps 2V CMOS Inverter**, S. Konaka, T. Kobayashi, T. Matsuda, M. Ugajin, K. Imai and T. Sakai, *NTT Advanced Fabrication Technology Lab., Kanagawa, Japan* **493**

Session 19: Quantum Electronics and Compound Semiconductors—Compound Semiconductor FETs **497**

Tuesday, December 11, 2:15 p.m.

Continental Ballroom 6

Co-Chairmen: T. Mimura, Fujitsu Research Laboratories
H. Kondoh, Hewlett Packard

2:15 p.m.

Introduction

2:20 p.m.

- 19.1 Fabrication of 80 nm Self-Aligned T-Gate AlInAs/GaInAs HEMT**, L. Nguyen, L. Jelloian, M. Thompson and M. Lui, *Hughes Aircraft Company, Malibu, CA* **499**

2:45 p.m.

- 19.2 0.2µm T-Shaped Gate 2DEGFETs with an (InAs)(GaAs) Short Period Superlattice Channel on a GaAs Substrate**, K. Onda, H. Toyoshima, E. Mizuki, N. Samoto, Y. Makino, M. Kuzuhara, and T. Itoh, *NEC Corporation, Kawasaki, Japan* **503**

3:10 p.m.

- 19.3 Short-Gate-Length Epitaxial-Channel Self-Aligned GaAs MESFETs with Very Large k-factor**, T. Jackson, G. Pepper, J. DeGelormo and T. Kuech, *IBM T.J. Watson Research Center, Yorktown Heights, NY* **507**

3:35 p.m.

- 19.4 Possible Scaling Limit of Ion-Implanted GaAs MESFET for Large-Scale Integrated Circuits**, M. Hirose and N. Uchitomi, *Toshiba Corporation, Kawasaki, Japan* **511**

4:00 p.m.

- 19.5 High Performance GaSb-P-Channel MODFETs**, L. Luo, K. Longenbach and W. Wang, *Columbia University, New York, NY* **515**

4:25 p.m.

- 19.6 Complementary III-V Heterostructure FETs for Low Power Integrated Circuits**, A. Akinwande, P. Ruden, D. Grider, J. Nohava, T. Nohava, P. Joslyn and J. Breezley, *Honeywell Inc., Bloomington, MN* **983**

Session 20: Vacuum Electronics—Crossed-Field Devices **519**

Tuesday, December 11, 2:15 p.m.

Continental Ballroom 7-9

Co-Chairmen: G. Thomas, Varian Associates
R. Abrams, Naval Research Laboratories

2:15 p.m.

Introduction

2:20 p.m.

- 20.1 Computer Simulations of Re-Entrant Crossed-Field Amplifiers**, D. Chernin and A. Drobot, *Science Applications International Corporation, McLean, VA* **521**

2:45 p.m.

- 20.2 Simulations of Crossed-Field Amplifier Operation Using Guiding Center Dynamics (Invited Paper)**, S. Riyopoulos, *Science Applications International Corporation, McLean, VA* **525**

3:10 p.m.

- 20.3 Methods for Enhancing Low Noise CFA Performance**, N. Dionne, W. Griffin and W. Smith, *Raytheon Company, Waltham, MA* **529**

3:35 p.m.

- 20.4 Rotary Probe Measurements of a Crossed-Field Amplifier Slow Wave Circuit**, W. Best and T. Treado, *Varian Associates, Beverly, MA* **533**

4:00 p.m.

- 20.5 Measurements of Electron-RF Interactions and Noise in a Low Frequency Crossed-Field Amplifier**, J. Browning, C. Chan, J. Ye and T. Ruden, *Northeastern University, Boston, MA* **537**

4:25 p.m.

- 20.6 Experimental Results of Power Combining and Phase-Locking Magnetrons for Accelerator Applications**, L. Zurk, T. Treado, R. Smith III, T. Hansen, J. Barry, D. Jenkins and G. Thomas, *Varian Associates, Inc., Beverly, MA* **541**

4:50 p.m.

- 20.7 Millimeter Wave High Gain CFA**, G. MacMaster and L. Nichols, *Raytheon Company, Waltham, MA* **963**

Session 21: Evening Panel Discussion **545**

Tuesday, December 11, 8:00 p.m.

Continental Ballroom 1-4

Panel Moderator: Dan Hutcheson
VLSI Research
San Jose, CA

WILL LOW-VOLUME SUBMICRON MANUFACTURING BE COST EFFECTIVE IN THE 1990's?

Panel Members:

M. K. Allen
Cypress Semiconductor
San Jose, CA

T. Kubota
NEC Electronics
Roseville, CA

S. Emori
Fujitsu
Kawasaki, Japan

G. Stouder
Motorola, Inc.
Austin, TX

R. F. Graham
Novellus
San Jose, CA

D. Toombs
Sematech
Austin, TX

C. J. Koomen
Phillips
Hilversum, The Netherlands

Session 22: Evening Panel Discussion **547**

Tuesday, December 11, 8:00 p.m.

Continental Ballroom 5

Panel Moderator: Yoichi Akasaka
Mitsubishi Electric Corporation
Itami-si, Japan

SILICON ON INSULATOR—IS IT REAL?

Panel Members:

A. J. Auberton-Herve
Leti
Grenoble, France

K. Izumi
NTT
Atsugi, Japan

M. Burnham
Motorola Inc.
Mesa, AZ

K. Natori
Toshiba
Kawasaki, Japan

J. P. Colinge
IMEC
Leuven, Belgium

Y. Nishi
Hewlett Packard
Palo Alto, CA

Session 23: Evening Panel Discussion **549**

Tuesday, December 11, 8:00 p.m.

Continental Ballroom 6-9

Panel Moderator: Herwig Kogelnik
AT&T Bell Laboratories
Holmdel, NJ

THE FUTURE OF OPTICAL AND ELECTRONIC COMPUTING

Panel Members:

J. L. Hennessy
Stanford University
Stanford, CA

D. A. B. Miller
AT&T Bell Laboratories
Holmdel, NJ

R. W. Keyes
IBM
Yorktown Heights, NY

A. Sawchuck
USC
Los Angeles, CA

H. T. Kung
Carnegie Melon University
Pittsburgh, PA

Session 24: Solid State Devices—Hot-Carrier Effects and Reliability 551

Wednesday, December 12, 9:00 a.m.

Grand Ballroom A

Co-Chairmen: T-Y. Huang, Xerox PARC
K. Natori, Toshiba Corporation

9:00 a.m.

Introduction

9:05 a.m.

- 24.1 The Effects of Hot-Electron Degradation on Analog MOSFET Performance**, J. Chung, K. Quader, C. Sodini, P. Ko and C. Hu, *University of California, Berkeley, CA* 553

9:30 a.m.

- 24.2 Roles of Oxide Trapped Charge and Generated Interface States on GIDL Under Hot-Carrier Stressing**, G. Lo and D. Kwong, *The University of Texas at Austin, Austin, TX* 557

9:55 a.m.

- 24.3 A New Monitor to Predict Hot-Carrier Damage of PMOST Transistors**, R. Woltjer and G. Paulzen, *Philips Research Laboratories, Eindhoven, The Netherlands* 561

10:20 a.m.

- 24.4 Gate-Oxide Thickness Dependence of Hot-Carrier Induced Degradation in Buried p-MOSFETs**, S. Odanaka and A. Hiroki, *Matsushita Electric Industrial Company, Osaka, Japan* 565

10:45 a.m.

- 24.5 Hot Carrier Reliability in Deep Submicrometer MOSFETs**, H. Hazama, M. Iwase and S. Takagi, *Toshiba Corporation, Kawasaki, Japan* 569

11:10 a.m.

- 24.6 AC Hot-Carrier Degradation due to Gate-Pulse-Induced Noise**, R. Izawa, K. Umeda and E. Takeda, *Hitachi, Ltd., Tokyo, Japan* 573

11:35 a.m.

- 24.7 Lucky Hole Injection Induced by Band-to-Band Tunneling Leakage in Stacked Gate Transistors**, K. Yoshikawa, S. Mori, E. Sakagami, Y. Ohshima, Y. Kaneko and N. Arai, *Toshiba Corporation, Kawasaki, Japan* 577

Session 25: Device Technology—Silicon on Insulator and Advanced Bipolar Technologies 581

Wednesday, December 12, 9:00 a.m.

Grand Ballroom B

Co-Chairmen: A. Nasr, Digital Equipment Company
J. Ruzyllo, Pennsylvania State University

9:00 a.m.

Introduction

9:05 a.m.

- 25.1 A Half-Micron CMOS Technology using Ultra Thin Silicon on Insulator**, P. Woerlee, C. Juffermans, H. Lifka, W. Manders, F. Lansink, G. Paulzen, P. Sheridan and A. Walker, *Philips Research Laboratories, Eindhoven, The Netherlands* 583

9:30 a.m.

- 25.2 Fabrication of CMOS on Ultrathin SOI Obtained by Epitaxial Lateral Overgrowth and Chemical-Mechanical Polishing**, G. Shahidi, B. Davari, Y. Taur, J. Warnock, M. Wordeman, S. Mader, P. McFarland, M. Rodriguez, R. Assenza, G. Bronner, B. Ginzberg, T. Lii, M. Polcari and T. Ning, *IBM T. J. Watson Research Center, Yorktown Heights, NY* 587

9:55 a.m.

- 25.3 Structure Design for Submicron MOSFET on Ultra Thin SOI**, Y. Yamaguchi, T. Iwamatsu, H. Oda, Y. Inoue, T. Nishimura, Y. Akasaka, *Mitsubishi Electric Corporation, Itami, Japan* 591

10:20 a.m.

- 25.4 Silicon-on-Insulator "Gate-All-Around Device,"** J-P. Colinge, M. Gao, A. Romano-Rodriguez, H. Maes and C. Claeys, *IMEC, Leuven, Belgium* 595

10:45 a.m.

- 25.5 4-Layer 3-D IC Technologies for Parallel Signal Processing**, K. Yamazaki, Y. Itoh, A. Wada, K. Morimoto and Y. Tomita, *Matsushita Electric Industrial Co., Ltd., Osaka, Japan* 599

11:10 a.m.

- 25.6 Epitaxial-Base Double-Poly Self-Aligned Bipolar Transistors**, E. Ganin, T. Chen, J. Stork, B. Meyerson, J. Cressler, G. Scilla, J. Warnock, D. Harame, G. Patton and T. Ning, *IBM, Yorktown Heights, NY* 603

11:35 a.m.

- 25.7 A "Self-Aligned" Selective MBE Technology for High-Performance Bipolar Transistors**, F. Sato, H. Takemura, T. Tashiro, H. Hirayama, M. Hiroi, K. Koyama and M. Nakamae, *NEC Corporation, Kanagawa, Japan* 607

Session 26: Detectors, Sensors and Displays—Sensors, Actuators and Detectors 611

Wednesday, December 12, 9:00 a.m.

Continental Ballroom 1-3

Co-Chairman: R. Bicking, Honeywell
L. Chrisel, Nova Sensor

9:00 a.m.

Introduction

9:05 a.m.

- 26.1 Microstructure Sensors (Invited Paper)**, H. Guckel, T. Christenson, K. Skrobis, J. Sniegowski, J. Kang, B. Choi and E. Lovell, *University of Wisconsin, Madison, WI* 613

9:30 a.m.

- 26.2 Lead Zirconate Titanate (PZT) Thin Films in Surface-Micromachined Sensor Structures**, T. Tamagawa, D. Polla and C. Hsueh, *University of Minnesota, Minneapolis, MN* 617

9:55 a.m.

- 26.3 Interfacial Force Sensor with Force-Feedback Control**, S. Joyce, J. Houston and B.K. Smith, *Sandia National Laboratories, Albuquerque, NM* 621

10:20 a.m.

- 26.4 Single Crystal Silicon Micro-Actuators**, K. Suzuki, *NEC Corporation, Kanagawa, Japan* 625

10:45 a.m.

- 26.5 Surface-Micromachined Linear Thermal Microactuators**, J. Judy, T. Tamagawa and D. Polla, *University of Minnesota, Minneapolis, MN* 629

11:10 a.m.

- 26.6 New Position-Sensitive Avalanche Photodiode with Single Photon Sensitivity and Picosecond Resolution**, G. Ripamonti, S. Cova, M. Ghioni, M. Mastrapasqua, and F. Giannetta, *Politecnico di Milano, Milan, Italy* 633

11:35 a.m.

- 26.7 Integrated Waveguide Photodetector Using Si/SiGe Multiple Quantum Wells for Long Wavelength Applications**, V. Kesan, P. May, E. Bassous and S. Iyer, *IBM Research Division, Yorktown Heights, NY* 637

12:00 p.m.

- 26.8 A Novel Si-Based LWIR Detector: "The SiGe/Si Heterojunction Internal Photoemission Detector"**, T. Lin, E. Jones, A. Ksendzov, S. Dejewski, R. Fathauer, T. Krabach and J. Maserjian, *California Institute of Technology, Pasadena, CA* 641

Session 27: Integrated Circuits—Dynamic Memories 645

Wednesday, December 12, 9:00 a.m.

Continental Ballroom 4-5

Co-Chairmen: C. Dennison, Micron Technology Inc.
B. Yeagain, Motorola Inc.

9:00 a.m.

Introduction

9:05 a.m.

- 27.1 Process Integration for 64M DRAM Using an Asymmetrical Stacked Trench Capacitor (AST) Cell**, K. Sunouchi, F. Horiguchi, A. Nitayama, K. Hieda, H. Takato, N. Okabe, T. Yamada, T. Ozaki, K. Hashimoto, S. Takedai, A. Yagishita, Y. Takahashi, A. Kumagai and F. Masuoka, *Toshiba Corporation, Kawasaki, Japan* 647

9:30 a.m.

- 27.2 A Novel Stacked Capacitor Cell with Dual Cell Plate for 64 Mb DRAMs**, H. Arima, A. Hachisuka, T. Ogawa, T. Okudaira, Y. Okumura, Y. Matsui, K. Motonami, T. Matsukawa and N. Tsubouchi, *Mitsubishi Electric Corporation, Hyogo, Japan* 651

9:55 a.m.

- 27.3 A Capacitor Over Bit-Line (COB) Cell with A Hemispherical-Grain Storage Node for 64Mb DRAMs**, M. Sakao, N. Kasai, T. Ishijima, E. Ikawa, H. Watanabe, K. Terada and T. Kikawa, *NEC Corporation, Kanagawa, Japan* 655

10:20 a.m.

- 27.4 Rugged Surface Poly-Si Electrode and Low Temperature Deposited Si₃N₄ for 64MBT and Beyond STC DRAM Cell**, M. Yoshimaru, J. Miyano, N. Inoue, A. Sakamoto, S. You, H. Tamura and M. Ino, *Oki Electric Industry Co., Ltd., Tokyo, Japan* 659

10:45 a.m.

- 27.5 Electrical Characterization of Textured Interpoly Capacitors for Advanced Stacked DRAMs**, P. Fazan and A. Ditali, *Micron Technology Inc., Boise, ID* 663

Session 28: Quantum Electronics and Compound Semiconductors—Heterojunction Bipolar Transistors 667

Wednesday, December 12, 9:00 a.m.

Continental Ballroom 6

Co-Chairmen: S. Forrest, University of Southern California
P. Ruden, University of Minnesota

9:00 a.m.

Introduction

9:05 a.m.

- 28.1 Comparison of PNP AlGaAs/GaAs Heterojunction Bipolar Transistor with and without Base Quasielectric Field**, W. Liu, D. Hill, D. Costa and J. Harris, Jr., *Stanford University, Stanford, CA* 669

9:30 a.m.

- 28.2 Current Induced Degradation of Be-doped AlGaAs/GaAs HBTs and Its Suppression by Zn Diffusion into Extrinsic Base Layer**, O. Nakajima, H. Ito, T. Nittono, and K. Nagata, *NTT LSI Laboratories, Kanagawa, Japan* 673

9:55 a.m.

- 28.3 High-Gain, High-Speed InGaAs/InP Heterojunction Bipolar Transistors**, C. Kyono, P. Cheung, C. Pinzone, N. Gerrard, T. Bustami, C. Maziar, D. Neikirk and R. Dupuis, *The University of Texas at Austin, Austin, TX* 677

10:20 a.m.

- 28.4 InAlAs/InGaAs HBTs Using Magnesium P-type Dopant**, A. Miura, T. Yakihara, S. Uchida and S. Oka, *Yokogawa Electric Corporation, Tokyo, Japan* 681

10:45 a.m.

- 28.5 256 bit Parallel XOR Gate Operating with Optical Input and Output**, K. Matsuda, H. Adachi, T. Chino and J. Shibata, *Matsushita Electric Industrial Company, Ltd., Osaka, Japan* 685

11:10 a.m.

- 28.6 Models and Measurements of Hg_{1-x}Cd_xTe Heterojunction Transistors**, M. Jack, G. Chapman, M. Kalisher, K. Kosai, J. Myrosznyi, W. Radford and M. Ray, *Santa Barbara Research Center, Goleta, CA*, O. Wu, *Malibu Research Laboratories, Malibu, CA* 689

11:35 a.m.

- 28.7 Integrated Multiquantum Well Heterojunction Bipolar Transistors for Optical Switching and Thresholding Applications (Invited Paper)**, P. Bhattacharya, J. Singh, S. Goswami, W.Q. Li and S.-C. Hong, *The University of Michigan, Ann Arbor, MI* 693

Session 29: Vacuum Electronics—Gyrotrons and Other Advanced Concepts 697

Wednesday, December 12, 9:00 a.m.

Continental Ballroom 7-9

Co-Chairmen: V. Granatstein, University of Maryland
N. Luhmann, University of California, Los Angeles

9:00 a.m.

Introduction

9:05 a.m.

- 29.1 Recent Developments in Millimeter-Wave Gyro-TWT Research at NTHU (Invited Paper)**, K. Chu, L. Barnett, W. Lau, L. Chang and C. Kou, *National Tsing Hua University, Hsinchu, Taiwan* 699

9:30 a.m.

- 29.2 Gain Broadening in an Inhomogeneous Gyrotron Traveling Wave Amplifier**, G. Park and S. Park, *Omega P, Inc., New Haven, CT*, R. Kyser, *BK Systems, Inc., Rockville, MD*, and C. Armstrong and A. Ganguly, *Naval Research Laboratory, Washington, DC* 703

9:55 a.m.

- 29.3 Negative Energy Cyclotron Resonance Maser**, E. Lednum, D. McDermott, A. Lin and N. Luhmann, Jr., *University of California, Los Angeles, CA* 707

10:20 a.m.

- 29.4 Dielectric Loaded Broadband Gyro-TWT**, K. Leou, D. McDermott and N. Luhmann, Jr., *University of California, Los Angeles, CA* 711

10:45 a.m.

- 29.5 Pulsed Microwave and Millimeter Wavelength Radiation from the Back-Lighted Thyratron**, R. Liou, H. Figueroa, A. McCurdy, G. Kirkman-Amemiya, R. Temkin, H. Fetterman and M. Gundersen, *University of Southern California, Los Angeles, CA* 715

11:10 a.m.

- 29.6 A Comparison of Different Approaches to Using the New High T_c Superconductors for Microwave Tube Magnets**, C. Shiffman and C.D. Wu, *Northeastern University, Boston, MA* and G. Thomas, *Varian Associates, Inc., Beverly, MA* 719

11:35 a.m.

- 29.7 Measurements of the Inverse Smith-Purcell Effect at Submillimeter Wavelengths**, J. Bae, H. Shirai, T. Nishida, T. Nozokido, K. Furuya and K. Mizuno, *Tohoku University, Sendai, Japan* 723

Session 30: Modeling and Simulation—Process Modeling 727

Wednesday, December 12, 9:00 a.m.

Imperial Ballroom A

Co-Chairmen: C. Rafferty, AT&T Bell Laboratories
L. Borucki, Motorola Inc.

9:00 a.m.

Introduction

9:05 a.m.

- 30.1 Impurity and Point Defect Redistribution in the Presence of Crystal Defects (Invited Paper)**, M. Orlowski, *Motorola Inc., Austin, TX* 729

9:30 a.m.

- 30.2 Non-equilibrium Diffusion Process Modeling Based on Three-Dimensional Simulator and a Regulated Point-Defect Injection Experiment**, T. Okada, S. Kambayashi, S. Onga, I. Mizushima, K. Yamabe and J. Matsunaga, *Toshiba Corporation, Kawasaki, Japan* 733

9:55 a.m.

- 30.3 Modeling of Polysilicon Diffusion Sources**, F. Lau, *Siemens AG, Munich, FRG* 737

- 10:20 a.m.
30.4 Viscous Nitride Model for Nitride/Oxide Isolation Structures, P. Griffin, *Stanford University, Stanford, CA*, and C. Rafferty, *AT&T Bell Laboratories, Murray Hill, NJ* **741**
- 10:45 a.m.
30.5 Monte Carlo Simulation of Ion Implantation into Single-Crystal Silicon Including New Models for Electronic Stopping and Cumulative Damage, K. Klein, C. Park and A. Tasch, *University of Texas, Austin, TX* **745**
- 11:10 a.m.
30.6 Simulation and Experimental Study of the Dynamics of Arsenic Clustering and Precipitation Including Ramp-Up and Ramp-Down Conditions, R. Subrahmanyam, M. Orlowski and G. Huffman, *Motorola Inc., Austin, TX* **749**
- 11:35 a.m.
30.7 Evidence and Modeling of Anomalous Low Concentration Arsenic Inactivation, L. Borucki, *Motorola Inc., Mesa, AZ* **753**

Session 31: Modeling and Simulation—Quantum Transport

757

Wednesday, December 12, 9:00 a.m.
Imperial Ballroom B

Co-Chairmen: F. Buot, *Naval Research Laboratories*
T. Toyabe, *University of California, Berkeley*

9:00 a.m.

Introduction

9:05 a.m.

- 31.1 Bandgap Narrowing and III-V Heterostructure FETs**, D. Myers, J. Lott, J. Lowney, J. Klem and C. Tigges, *Sandia National Laboratories, Albuquerque, NM* **759**

9:30 a.m.

- 31.2 Advanced Electron Mobility Model of MOS Inversion Layer Considering 2D-degenerated Electron Gas Physics**, M. Ishizaka, T. Iizuka, S. Ohi, M. Fukuma and H. Mikoshiba, *NEC Corporation, Sagami-hara, Japan* **763**

9:55 a.m.

- 31.3 Self-Consistent Modeling of Bipolar Tunnel Heterostructures with Quantum Mechanical Current**, J. Bigelow and J. Leburton, *Beckman Institute for Advanced Science and Technology, Urbana, IL* **767**

10:20 a.m.

- 31.4 The Numerical Simulation of Particle Trajectories in Quantum Transport and the Effects of Scattering and Self-consistency on the Performance of Quantum Well Devices**, K. Jensen and F. Buot, *Naval Research Laboratory, Washington, DC* **771**

10:45 a.m.

- 31.5 An Efficient Quantum Monte Carlo Simulation Method—Path Integral Approach for Dissipative Transport in Quantum Devices**, K. Katayama, S. Kamohara and S. Itoh, *Hitachi, Ltd., Tokyo, Japan* **775**

11:10 a.m.

- 31.6 Theoretical Studies of Current Transport in Interband Tunnel Structures Using the Effective Bond-Orbital Model**, D. Ting, E. Yu and T. McGill, *California Institute of Technology, Pasadena, CA* **779**

Session 32: Solid State Devices—Power Devices and Integrated Circuits

783

Wednesday, December 12, 1:30 p.m.
Grand Ballroom A

Co-Chairmen: S. Robb, *Motorola Inc.*
K. Shenai, *GE Corporate Research and Development Center*

1:30 p.m.

Introduction

1:35 p.m.

- 32.1 A Review of the Status of Diamond and Silicon Carbide Devices for High Power, -Temperature and -Frequency Applications (Invited Paper)**, R. Davis, J. Palmour and J. Edmond, *North Carolina State University, Raleigh, NC* **785**

2:00 p.m.

- 32.2 Characterization and Modeling of the Temperature Dependence of Lateral DMOS Transistors for High Temperature Applications of Power Integrated Circuits**, G. Dolny, G. Nosstrand, *David Sarnoff Research Center, Princeton, NJ*, and K. Hill, *General Electric, Binghamton, NY* **789**

2:25 p.m.

- 32.3 Optimum Low-Voltage Silicon Power Switches Fabricated Using Scaled Trench MOS Technology**, K. Shenai, W. Hennessy, M. Ghezzi, C. Korman, H. Chang, M. Adler and V. Temple, *General Electric, Schenectady, NY* **793**

2:50 p.m.

- 32.4 Method of Internal Overvoltage Protection and Current Limit for a Lateral PNP Transistor Formed by Poly Self-Aligned Emitter and Base, With Extended Collector**, M. Masquelier and D. Okada, *Motorola Inc., Phoenix, AZ* **799**

3:15 p.m.

- 32.5 1000 and 1500 Volts Planar Devices Using Field Plate and Semi-Resistive Layers: Design and Fabrication**, G. Charitat, D. Jaume, A. Peyre-Lavigne and P. Rossel, *Laboratoire d'Automatique et d'Analyse des Systemes, Toulouse Cedex, France* **803**

3:40 p.m.

- 32.6 A 2000 V-Non-Punch-Through-IGBT with Dynamic Properties like a 1000 V-IGBT**, T. Laska and G. Miller, *Siemens AG, Munich, FRG* **807**

4:05 p.m.

- 32.7 Turn-On Mechanism of 2500V MOS Assisted Gate Triggered Thyristor (MAGT)**, A. Nakagawa, H. Yoshida and Y. Kamei, *Toshiba Research & Development Center, Kawasaki, Japan* **811**

Session 33: Device Technology—Advanced Photolithography and Sub-half Micron CMOS Device Reliability

815

Wednesday, December 12, 1:30 p.m.
Grand Ballroom B

Co-chairmen: S. Hillenius, *AT&T Bell Laboratories*
B. Davari, *IBM Research Center*

1:30 p.m.

Introduction

1:35 p.m.

- 33.1 Fabrication of 64M DRAM with i-Line Phase-Shift Lithography**, K. Nakagawa, M. Taguchi and T. Ema, *Fujitsu Limited, Kawasaki, Japan* **817**

2:00 p.m.

- 33.2 Transparent Phase Shifting Mask**, H. Watanabe, Y. Todokoro and M. Inoue, *Matsushita Electronics Corporation, Kyoto, Japan* **821**

2:25 p.m.

- 33.3 0.2 μ m or Less i-line Lithography by Phase-Shifting-Mask Technology**, H. Jinbo and Y. Yamashita, *Oki Electric Industry Co., Ltd., Tokyo Japan* **825**

2:50 p.m.

- 33.4 Self-Aligned Silicided Inverse-T Gate LDD Devices for Sub-Half Micron CMOS Technology**, M. Chen, S. Hillenius, W. Juengling, T. Yang, A. Kornblit, W. Lindenberger, J. Swiderski and D. Favreau, *AT&T Bell Laboratories, Allentown, PA* **829**

3:15 p.m.

- 33.5 Drain Structure Optimization for Highly Reliable Deep Submicron nMOSFETs with 3.3V High Performance Operation on the Scaling Trend**, F. Matsuoka, K. Kasai, H. Oyamatsu, M. Kinugawa and K. Maeguchi, *Toshiba Corporation, Kawasaki, Japan* **833**

3:40 p.m.

- 33.6 Deep-Submicron Nitrided-Oxide CMOS Technology for 3.3-V Operation**, T. Hori, *Matsushita Electric Industrial Co., Ltd., Osaka, Japan* **837**

Session 34: Detectors, Sensors and Displays—Thin Film Transistors and Displays

Wednesday, December 12, 1:30 p.m.
Continental Ballroom 1-3

Co-Chairmen: D. Greve, Carnegie Mellon University
R. Troutman, IBM T.J. Watson Research Center

1:30 p.m.

Introduction

1:35 p.m.

- 34.1 Active Matrix Liquid Crystal Display Design Using Low and High Temperature Processed Polysilicon TFTs (Invited Paper)**, A. Lewis, I. Wu, T. Huang, A. Chiang, R. Bruce, Xerox Palo Alto Research Centre, Palo Alto, CA 843

2:00 p.m.

- 34.2 A High-Reliability, Low-Operation -Voltage Monolithic Active-Matrix LCD by Using Advanced Solid-Phase -Growth Technique**, A. Nakamura, F. Emoto, E. Fujii, A. Yamamoto, Y. Uemoto, S. Hayashi, Y. Kato, and K. Senda, Matsushita Electronics Corporation, Osaka, Japan 847

2:25 p.m.

- 34.3 A new a-Si TFT with Al₂O₃/SiN Double-layered Gate Insulator for 10.4-inch Diagonal Multicolor Display**, H. Yamanoto, H. Matsumaru, K. Tsutsui, N. Konishi, M. Nakatani, K. Shirahashi, A. Sasano and T. Tsukada, Hitachi, Ltd., Tokyo, Japan 851

2:50 p.m.

- 34.4 Modeling and Parameter Extraction of Amorphous Silicon Thin-Film-Transistors for Active-Matrix Liquid-Crystal Displays**, R. Troutman and F. Libsch, IBM, Yorktown Heights, NY 855

3:15 p.m.

- 34.5 Two-Dimensional Device Simulation for Avalanche Induced Short Channel Effect in Poly-Si TFT**, S. Yamada, S. Yokoyama and M. Koyanagi, Hiroshima University, Higashi-Hiroshima, Japan 859

3:40 p.m.

- 34.6 Evaluation of Polycrystalline Silicon Thin Film Transistors with the Charge Pumping Technique**, M. Koyanagi, Hiroshima University, Higashi-Hiroshima, Japan, I.-W. Wu, A. Lewis, R. Bruce, Xerox PARC, Palo Alto, CA, and M. Fuse, Fuji Xerox Company, Ltd., Kanagawa, Japan 863

4:05 p.m.

- 34.7 Mechanism and Device-to-Device Variation of Leakage Current in Polysilicon Thin Film Transistors**, I. Wu, A. Lewis, T. Huang, W. Jackson and A. Chiang, Xerox Palo Alto Research Center, Palo Alto, CA 867

Session 35: Vacuum Electronics—Linear Beam Devices

Wednesday, December 12, 1:30 p.m.
Continental Ballroom 7-9

Co-Chairmen: J. Christensen, Hughes Aircraft Co.
C. Liss, Raytheon Company

1:30 p.m.

Introduction

1:35 p.m.

- 35.1 Development of Sidebands in Ultra High Power Traveling Wave Tube Amplifiers (Invited Paper)**, J. Nation, G. Kerslick, D. Shiffler and L. Schachter, Cornell University, Ithaca, NY 873

2:00 p.m.

- 35.2 2.5-Dimensional Time Domain Particle-In-Cell Simulation Code For Collector Design**, Y. Goren, R. Wilson and P. Lally, Teledyne MEC, Palo Alto, CA 877

2:25 p.m.

- 35.3 Development of An 800 Watt KA-Band, Ring-Bar TWT**, R. LeBorgne, C. Goodman, R. Hull, O. Sauseng and G. Lee, Hughes Aircraft Company, Torrance, CA 881

2:50 p.m.

- 35.4 Modification of Klystron Beam Loading by Initial Velocity Modulation of the Beam**, R. Symons and R. Vaughan, Litton Systems Inc., San Carlos, CA 885

3:15 p.m.

- 35.5 Design of an 850-MHz Klystron**, B. Goplen, L. Ludeking, K. Nguyen and G. Warren, Mission Research Corporation, Newington, VA 889

3:40 p.m.

- 35.6 Emission Gated Device Experiment**, M. Kodis, N. Vanderplaats and E. Zaidman, Naval Research Laboratory, Washington, DC 893

4:05 p.m.

- 35.7 A Submillimeter-Wave Extended Interaction Oscillator with Novel Broadband Mechanical Tuning**, D. Perring, G. Phillips and R. Carter, European Space Research and Technology Centre, Noordwijk, The Netherlands 897

4:30 p.m.

- 35.8 Submillimeter Backward-Wave Oscillator**, L. Barnett, N. Stanekiewicz, V. Heinen and J. Dayton, NASA Lewis Research Center, Cleveland, OH 901

Session 36: Modeling and Simulation—Equipment Modeling

Wednesday, December 12, 1:30 p.m.
Imperial Ballroom A

Co-Chairmen: B. Mulvaney, MCC

1:30 p.m.

Introduction

1:35 p.m.

- 36.1 New Topography Expression Model and 3D-Topography Simulation of Al-Sputter Deposition, Etching, and Photolithography**, M. Fujinaga, T. Kunikiyo, T. Uchida, N. Kotani, A. Osaki and Y. Akasaka, Mitsubishi Electric Corporation, Hyogo, Japan 905

2:00 p.m.

- 36.2 Physically-Based Models of Alignment Schemes in Commercial Steppers**, C. Yuan and A. Strojwas, Carnegie Mellon University, Pittsburgh, PA 909

2:25 p.m.

- 36.3 Optimization and Design of Plasma Etching Process Utilizing a Glow Discharge Model and a Transport Model Simulation**, S. Park, Motorola Inc., Austin TX, and D. Economou, University of Houston, Houston, TX 913

2:50 p.m.

- 36.4 LPCVD Profile Simulation Using a Re-Emission Model**, J. McVittie, J. Rey, L. Cheng, M. Islam Raja and K. Saraswat, Stanford University, Stanford, CA 917

3:15 p.m.

- 36.5 Gas Flow Patterns and Thermal Uniformity in Rapid Thermal Processing Equipment**, S. Campbell, K. Knutson, K. Ahn, J. Leighton and B. Liu, University of Minnesota, Minneapolis, Minnesota 921

Late News Papers 925

SESSION 1

Plenary Session—Invited Papers

**Monday, December 10, 1990 — 9:00 a.m.
Grand Ballroom**

**Chairman: Alfred C. Ipri
David Sarnoff Research Center**

This year's plenary session consists of three exciting presentations that deal with diverse topics of Smart Power Technology, Optoelectronic Integrated Circuits and System Level Packaging.

The session begins with Professor Jayant Baliga from North Carolina State University who will present a paper entitled "Smart Power Technology: An Elephantine Opportunity." The presentation will begin with a description of the evolution of Smart Power and then go on to describe its impact on today's electronic systems. Structural and operational distinctions between MOSFETs used in power switching applications and logic circuits will be made. New power switches such as Insulated-Gate Bipolar Transistors (IGBTs) and MOS-Controlled Thyristors (MCTs) will also be described, as will their impact on various systems, such as motor drives and lighting ballasts.

Dr. Robert Leheny of Bellcore will next present a paper entitled "Optoelectronic Integrated Circuits." This is an emerging device technology designed to meet the future needs of telecommunications and the computing industry. This presentation will review the current status and future prospects of Opto-Electronic Integrated Circuits (OEICs) concentrating on such advantages as high reliability and performance, as well as potentially low cost. Problem areas associated with integrated components having very different materials and structural requirements, however, have presented formidable barriers to the demonstration of OEICs. Continuing advances in device design and fabrication technologies are, today, making substantial strides towards solving these problems.

The third paper, entitled "System Level Packaging An Alternative to Monolithic ULSI," will be presented by Professor R. Fabian Pease from Stanford University. System level packaging, at present, involves the use of multichip packages and high-density wire bonding. Future approaches may involve silicon micromachining or superconducting chip-to-chip interconnects. The advantages of system level packaging over conventional chip packaging such as higher speed, lower power and lower cost are achieved through denser packaging and shorter chip-to-chip interconnect distances.

It is hoped that system level packaging will aid in stemming the spectacular increase in the cost of manufacturing monolithic ULSI.

NOTES

"SMART POWER TECHNOLOGY : An Elephantine Opportunity"
(INVITED PLENARY SESSION PAPER)

Professor B. Jayant Baliga

Electrical and Computer Engineering Department,
North Carolina State University,
Raleigh, N.C. 27695-7911.

ABSTRACT

Until recently, power devices have been a relatively small segment of the semiconductor industry. With the advent of MOS-gated power device technology, the option of creating a smart power technology has become viable. This paper provides a review of the evolution of smart power technology from bipolar discrete devices, through MOS-gated power devices, to the complex power integrated circuits that combine high voltage, high current devices with analog and digital circuits. The advent of smart power technology is expected to have a major impact on society via its application to computer power supplies, automotive electronics, appliance controls, and transportation systems.

INTRODUCTION

The roots of power semiconductor technology extend before those for integrated circuits. Since the invention of the bipolar transistor and the thyristor, there has been a strong motivation to increase the power handling capability of these discrete devices in order to extend their applications. The growth in the current and voltage handling capability of power thyristors over the last 35 years has been dramatic. It is impressive to note that by the 1990s, a single (monolithic) power thyristor made from a 100 mm diameter wafer is commercially available with the ability to block 6500 volts in the off-state and conduct over 2000 amperes in the on-state. Since each of these devices are fabricated out of an entire silicon wafer, the growth in the ratings of power thyristors has been determined by the availability of high resistivity, large diameter, float-zone, silicon wafers. The sharp improvement in ratings achieved in the late 1970s can

be directly linked to the development of neutron transmutation doping - a new method of doping silicon very uniformly by converting a silicon isotope to phosphorus by the absorption of thermal neutrons.

Over the years, the process technology for bipolar power devices lagged behind that developed for integrated circuits. These devices continued to be designed using design rules in the range of mil units. In addition, the junction depths used to fabricate these devices were maintained in the range of 10 to 100 microns to enable high voltage operation. Consequently, the process technology for power devices was significantly different from that used for integrated circuits. This situation changed due to the introduction of the power MOSFET in the 1970s and the advent of MOS/Bipolar devices in the 1980s.

MOS POWER DEVICES

The power MOSFET was first introduced commercially in the 1970s. When compared with the bipolar transistor, this device had the advantageous features of a high input impedance, high switching speed, ease of paralleling, and much superior safe-operating-area (SOA). This makes the power MOSFET attractive for many applications such as computer power supplies and automotive electronics.

The current rating of the power MOSFET is determined by the resistance within the device (1). The resistance can be reduced by making the channel length small, especially in the case of devices with blocking voltages below 100 volts. In the commercially available power DMOSFET structure, the channel length is controlled by adjusting the relative diffusion depth of the p-base and the N+ source regions. This allows the fabrication of devices with sub-micron channel length

without the need to use advanced VLSI processing tools. However, it can be shown that the current distribution within the cell can be improved by reducing the size of the poly-silicon window by using VLSI technology (2). By scaling the DMOSFET geometry, the specific on-resistance (on-resistance per unit active area) has been reduced from 7 milli-ohm cm² in 1970 to only 0.7 milli-ohm cm² in 1990. In addition, the development of power MOSFETs with trench gate structures, based upon RIE processes used for DRAMs, have been explored resulting in devices with specific on-resistances as low as 0.3 milli-ohm cm². The latter value is approaching the theoretical limit if 0.15 milli-ohm cm² for a silicon device. For this reason, if further improvements are to be achieved, it will be necessary to embark upon the development of power devices based upon Silicon Carbide. Theoretical analysis indicates that the specific on-resistance can be reduced by over 100 times by replacing silicon with silicon carbide in the future (3).

Although the power MOSFET is well suited for applications where the blocking voltages are relatively low (less than 200 volts), its on-resistance increases rapidly with increase in the blocking voltage. Due to this phenomenon, it has not been possible to economically manufacture high voltage power MOSFETs with high current ratings. One solution to this problem was the invention of the Insulated Gate Bipolar Transistor (IGBT) (1). These devices have the same high input impedance feature of the power MOSFET and can operate at a current density of an order of magnitude larger than the power MOSFET. This makes them suitable for applications where the blocking voltage exceeds 200 volts, such as motor drives, appliance controls, robotics/numerical controls, etc.

The availability of the power MOSFET and the IGBT with their voltage controlled characteristics resulted in a tremendous simplification in the control circuit. This in turn created the opportunity for development of integrated gate drive circuits. In many applications, the power devices are used in a totem pole configuration. For this reason, the control circuit must be capable of performing level shifting to high voltages. The development of integrated control circuits also provided the impetus to incorporate protective circuits on the control chips against over-voltage,

over-current, or over-temperature conditions. In addition, the need to interface with microprocessors led to the incorporation of logic circuits to provide encode/decode capability. This heralded the dawn of smart power technology in the 1990s.

SMART POWER TECHNOLOGY

In the broadest sense of definition, smart power technology provides the interface between the digital control logic and the power load (4-5). In its simplest form, it may consist of a level shifting and drive circuit that translates the logic level signals from a microprocessor to a voltage and current level sufficient to energize a load. An example of such a chip would be for display drives, where the load is usually capacitive in nature but requires drive voltages much greater than the operating voltage of logic circuits. On the other extreme, the smart power technology may be required to perform load monitoring, diagnostic functions, self-protection, and information feedback to the microprocessor, in addition to handling large amounts of power to actuate the load. An example of this is an automotive multiplexed bus system with distributed smart power modules for control of lights, motors, air-conditioning, etc.

A description of smart power technology can be made with the aid of Fig.1. Three fundamental functions that are performed with this technology are power control, sensing/protection, and interfacing. The basic components that are needed for the implementation of these functions are shown in this figure.

Power control is performed by using power devices and their drive circuits. It is the ability to handle high voltages, high currents, or a combination of both that makes smart power technology unique. The drive circuits are unusual in that they must be designed to operate at up to 30 volts to provide sufficient voltage to the gates of the power devices. In addition, for totem-pole operation, the drive circuit must be able to perform level shifting to high voltages. The regulation of power flow is performed by variety of power devices, with the MOS-gated devices being increasingly favored.

Smart power technology usually incorporates some form of sensor technology together with local feedback for protection of the IC. In addition

to detecting the exceeding of a current, voltage, or temperature limit, the detection of a no-load or under-voltage condition is sometimes implemented. The under-voltage condition is useful to ensure sufficient biasing of the power devices to prevent excessive power dissipation during start-up. The current sensing is done with minimum power loss by partitioning a few cells from the power device and feeding this current to the control circuit. The protection of the IC is accomplished by using a feedback loop containing high frequency bipolar transistors. The response time of the feedback loop is critical to a benign shut-down because the system current increases at a very rapid rate during a fault. This portion of the smart power chip requires implementation of high performance analog circuits.

The interface function in the smart power IC is accomplished by using logic circuits, which perform the encode and decode operations. The chip must not only respond to signals received from a microprocessor but must be capable of sending messages regarding operating status, such as over-temperature shut-down, and information related to load monitoring, such as a no-load or short-circuit condition. This requires integration of high density CMOS circuits on the smart power chip. Due to the large voltage swings and high chip temperatures arising from self-heating, the design of the CMOS circuits for smart power chips can be quite challenging to ensure immunity from latch-up.

PROCESS TECHNOLOGY

Due to the relatively high cost of dielectrically isolated (DI) silicon wafers, most smart power chips are being fabricated using junction isolation (JI). If the cost of DI wafers can be reduced in the future, it is likely that most smart power chips will be made using DI due to simplification in design by the elimination of parasitics and the option of integrating multiple, MOS-Bipolar power devices. Meanwhile the challenges faced by designers today are the integration of analog and digital circuits on the same chip with high voltage and high current devices. This requires the use of a two-level metal process, in addition to the polysilicon gate electrode. A thin metal layer is used to fabricate the analog and digital circuits and the thick metal is used for the power

devices. The need to bus high voltages around the chip also requires special metal cross-over design methodology where SIPOS layers are employed.

SMART POWER APPLICATIONS

Smart power chips are expected to have an impact on all areas in which power semiconductor devices are presently being used. The wide spectrum of voltages and currents over which power semiconductor devices are now being utilized is illustrated in Fig.2. On the one extreme are display drives that require relatively low currents and moderate voltages. These applications are already being served by smart power chips. On the other extreme lie traction (transportation systems) and High Voltage DC (HVDC) transmission which demand control of very high currents and voltages. The development of new MOS-Bipolar devices being researched at present could enable the penetration of smart power technology even to these applications. Meanwhile, a strong thrust is underway to create smart power chips for motor control, factory automation (robotics), computer power supplies, and automotive electronics. In many of these cases, application specific designs will be required putting pressure on the industry to create computer aided design (CAD) tools that can perform automated layout and mixed-mode circuit simulation at high voltages and currents.

CONCLUSIONS

Until recently, integrated circuit technology has been focussed primarily on chips for signal processing and data storage. This has resulted in a phenomenal capability for information processing that has led to the 'first electronic revolution'. This technology is akin to the brain in the human body, which assimilates data acquired via the senses and provides decision making capability. Although this technology has greatly enriched society, it has been hampered by the fact that in order to perform many functions, it is necessary to control significant amounts of energy being delivered to a variety of loads. Using the analogy of the human body, this is equivalent to the need for muscles to perform even the most basic tasks. The advent of smart power technology promises to create the 'second electronic revolution' by providing the brawn to complement the information processing capability.