Emerging Semiconductor Technology

Gupta/Langer
editors

STP 960
ASTM

EMERGING SEMICONDUCTOR TECHNOLOGY

A symposium
sponsored by
ASTM Committee F-1
on Electronics
San Jose, CA, 28-31 Jan. 1986

ASTM SPECIAL TECHNICAL PUBLICATION 960
Dinesh C. Gupta, Siliconix, Inc., and
Paul H. Langer, AT&T Bell Laboratories,
editors

ASTM Publication Code Number (PCN)
04-960000-46

1916 Race Street, Philadelphia, PA 19103

Library of Congress Cataloging-in-Publication Data

Emerging semiconductor technology.

(ASTM special technical publication; 960)
Papers presented at the Fourth International Symposium on Semiconductor Processing.
"ASTM publication code number (PCN) 04-960000-46."
Includes bibliographies and index.
1. Semiconductor industry—Congresses. 2. Semiconductors—Design and construction—Congresses. I. Gupta, D.C. (Dinesh C.) II. Langer, Paul H. III. ASTM Committee F-1 on Electronics. IV. Symposium on Semiconductor Processing (4th: 1986: San Jose, Calif.) V. Series.
TK7871.85.E47 1987 621.3815'2 86-28761
ISBN 0-8031-0459-6

Library of Congress Catalog Card Number: 86-28761

Foreword

The Fourth International Symposium on Semiconductor Processing was held at San Jose, California on 28-31 January, 1986 under the chairmanship of Dinesh C. Gupta, Siliconix Incorporated. The Symposium was sponsored by ASTM Committee F-1 on Electronics and co-sponsored by National Bureau of Standards, Semiconductor Equipment and Materials Institute, Stanford University Center for Integrated Systems, and IEEE Components, Hybrids and Manufacturing Technology Society. The Technical Committee was headed by Paul H. Langer, AT&T Bell Laboratories and the Arrangements and Publicity Committee was headed by Carl A. Germano, Motorola Incorporated.

The Symposium was successful because of the efforts of many persons who participated in the Advisory Board, and various committees, namely, the Technical Committee, the Arrangements and Publicity Committee, Registration Committee and the Spouse Committee. These persons included: Winthrop A. Baylies, ADE Corporation, Kenneth E. Benson, AT&T Bell Laboratories, W. Murray Bullis, Siltec Corporation, Paul Davis, Semiconductor Equipment and Materials Institute, James R. Ehrstein, National Bureau of Standards, Bruce L. Gehman, Deposition Technology Incorporated, Kathleen Greene, ASTM, Gilbert A. Gruber, Siliconix Incorporated, Lou Ann Gruber, Vijay Gupta, John A.Imbalzano, E.I. DuPont DeNemours & Company, Sharon Kaufmann and Philip L. Lively, ASTM, George E. Moore, Sr., Semiconductor Equipment and Materials Institute, James D. Plummer, Stanford University Center for Integrated Systems, Robert I. Scace, National Bureau of Standards, William R. Schevey, Allied Chemical Corp., Donald G. Schimmel, AT&T Bell Laboratories, Robert B. Swaroop, Fairchild Semiconductor, Gail Wesling, and Paul Wesling, Tandem Computers Incorporated.

In addition, the guidance was provided by the Chairman and the officers of ASTM Committee F-1 on Electronics, its various subcommittees including the Executive subcommittee. The following persons presided the technical and workshop sessions: J. Albers and A. Baghdadi, National Bureau of Standards, K. E. Benson, AT&T Bell Laboratories, J.O.Borland, Applied Materials, Inc., R.H.Bruce, Xerox Palo Alto Research Center, M. Buehler, Jet Propulsion Laboratory, W. M. Bullis, Siltec Corporation, S. Cox, AT&T Technologies, M. Current, Applied Materials, Inc., J. R. Ehrstein, National Bureau of Standards, B. Fay, Micronix Corporation, T. Francis, Air Products & Chemicals, G. A. Gruber and D. C. Gupta,

Siliconix, Inc., T. I. Kamins, Hewlett-Packard Laboratories, G. Koch, Flexible Manufacturing Systems, P. H. Langer, AT&T Bell Laboratories, J. Matlock, SEH America, R. K. Pancholy, Gould AMI Semiconductor, M. Pawlik, GEC Research, D. Perloff, Prometrix, Inc., J. Plummer, Stanford University Center for Integrated Systems, D. Walters, Varian Associates, Inc., W. R. Schevey, Allied Chemical Corporation, L. Shive, Monsanto Company, E. R. Sirkin, Zoran Corporation, F. Voltmer, Intel Corp., and W. Weisenberger, Ion Implant Services.

We are indebted to Richard D. Skinner, President, Integrated Circuit Engineering Corporation who presented a dinner speech on "Semiconductor Industry - An Economic Review", Richard A. Blanchard, Vice President, Siliconix Incorporated, Pat Hill Hubbard, Vice President, American Electronics Association, Richard Reis, Assistant Director, Stanford University Center for Integrated Systems, Robert I. Scace, Deputy Director, Center for Electronics and Electrical Engineering, National Bureau of Standards, James E. Springgate, President, Monsanto Electronic Materials Company, and James A. Thomas, Vice President, ASTM for the keynote speeches on the various topics on the first day of the Symposium.

We are grateful to the members and guests of ASTM Committee F-1 and Standards Committees of SEMI who were called upon from time to time for special assignments during the two-year planning of the Symposium.

Over one hundred and fifty scientists participated all over the world in the review process for the papers published in this publication. Without their participation, this publication would not have been possible.

And finally, we acknowledge the hard work and efforts of the staff of publication, review, editorial and marketing departments of ASTM in bringing out this book.

A Note of Appreciation to Reviewers

The quality of the papers that appear in this publication reflects not only the obvious efforts of the authors but also the unheralded, though essential, work of the reviewers. On behalf of ASTM we acknowledge with appreciation their dedication to high professional standards and their sacrifice of time and effort.

ASTM Committee on Publications

Related ASTM Publications

Semiconductor Processing, STP 850 (1984), 04-850000-46

Silicon Processing, STP 804 (1983), 04-804000-46

Lifetime Factors in Silicon, STP 712 (1980), 04-712000-46

Laser-Induced Damage in Optical Materials: 1982, STP 847 (1984), 04-847000-46

Laser-Induced Damage in Optical Materials: 1981, STP 799 (1983), 04-799000-46

Laser-Induced Damage in Optical Materials: 1983, STP 911 (1985), 04-911000-46

Preface

The papers in this volume were presented at the Fourth International Symposium on Semiconductor Processing held in San Jose, California on 28-31 January, 1986. The Symposium was sponsored by ASTM Committee F-1 on Electronics, and co-sponsored by National Bureau of Standards, Semiconductor Equipment and Materials Institute, Stanford University Center for Integrated Systems, and IEEE Components, Hybrids and Manufacturing Technology Society. In addition to the technical presentations, the symposium included two well-attended workshops, impressions of which are provided in appendix I.

The symposium addressed new problems in semiconductor technology and day-to-day problems in semiconductor processing for the mid 80's which arise from the rapid increases in device complexity and performance, emergence of integrated systems on-a-chip, automated factories, and silicon foundries. In the face of these demands, the realization of acceptable yields and reliability requires greater manufacturing and process-control disciplines from starting materials to finished devices. The symposium theme was, again this year, chosen to be Quality Through Measurement and Control.

The symposium opened with the talks on Standards and Product Quality by James A. Thomas, ASTM, and Standards for the Semiconductor Industry from ASTM and SEMI by Robert I. Scace, National Bureau of Standards. These presentations were followed by two papers giving the overview of silicon technology and relating it to device requirements. The requirements of silicon materials were described by James E. Springgate, Monsanto Electronic Materials Company. The process and equipment considerations were discussed by Richard A. Blanchard, Siliconix Incorporated.

The opening general session included a presentation and a discussion on Graduate Education for the Electronics Industry. Pat Hill Hubbard, Vice President, American Electronics Association discussed various programs that the Foundation is involved in in order to make doctoral study and academic careers more attractive. She said, "The need to have an adequate supply of quality engineers and sufficient faculty to educate them is considered of paramount importance to the health of the high tech industry and to the economic health of the nation." Richard Reis, Assistant Director, Stanford University Center for Integrated Systems presented a graduate education mix from Stanford's point

of view, noting the exceptions which make Stanford different from other schools in the nation.

The response to the symposium was extremely favorable once again. The involvement of industry, academia and government including the participation of foreign institutions confirmed a continued need for a regular forum to discuss technology topics in the context of measurement and control, a consistent theme which the Symposium established in 1982 involving the understanding and day-to-day control of the complex process technologies required for VLSI and other advanced device concepts.

The plans for the next symposium in 1988 in the series of symposia to be held at two-year intervals are underway. The problem areas and standardization needs identified in these symposia will provide the feedback to the research community and voluntary standards system essential for the future growth of the industry.

The cooperation and support of the ASTM staff in the formulation of this publication is appreciated. We are indebted to our industrial, government and university colleagues who contributed to the Symposium and the Proceedings.

Dinesh C. Gupta
San Jose, California.

Paul H. Langer
Allentown, Pennsylvania.

Contents

PLASMA TECHNOLOGY AND OTHER FABRICATION TECHNIQUES

MATERIAL DEFECTS, OXYGEN AND CARBON IN SILICON

YIELD ENHANCEMENT AND CONTAMINATION CONTROL ASPECTS

FAB EQUIPMENT: AUTOMATION AND RELIABILITY

APPENDIXES

Introduction

This volume is organized into seven sections: (1) Standards for Semiconductor Industry; (2) Epitaxial Technology; (3) Dielectrics and Junction Formation Techniques; (4) Plasma Technology and Other Fabrication Techniques; (5) Material Defects, Oxygen and Carbon in Silicon; (6) Yield Enhancement and Contamination Control Aspects; (7) Dopant Profiling Techniques and In-Process Measurements; and (8) Fab Equipment: Automation and Reliability. The papers describe the emerging semiconductor processes used in device fabrication, from its simplest use to discrete circuits through the complex applications to very-large-scale-integrated (VLSI) circuits.

After the introduction, unedited excerpts of one keynote paper, "Silicon and Semiconductors: Partners in the Late 1980's" are given. The synopses on workshops and graduate education are presented in two appendixes, I & II at the end of the volume.

STANDARDS FOR SEMICONDUCTOR INDUSTRY

Quality of measurement is the cornerstone of ASTM's system for the development of voluntary consensus standards. From the inception of the test method, through balloting and interlaboratory testing, the volunteers assure a high level of precision. The standard test methods, nomenclature, and specifications developed by ASTM and SEMI for the semiconductor industry support many acceptance tests and online measurements. The history of this collaborative work and its expected future course is discussed in this paper. The standards activities of foreign organizations and the interactions among these groups are also discussed.

EPITAXIAL TECHNOLOGY

The epitaxial layer is a backbone of the device structure. Major emphasis in epitaxial technology is to lower the defect level and improve the dopant distribution within the layer. The papers in this section discuss various techniques to improve epilayer quality. R. Reif presents a low pressure CVD system to deposit epitaxial films both with and without plasma enhancement at temperatures as low as 650°C. Chang and Rosczak adopt a more conventional atmospheric CVD system at 825°C to deposit epitaxial films. Swaroop and Fisher, et al present methods to improve epitaxial quality with respect to as-grown defects and electrical

parameters. Medernach and Wells study the vapor etch, and Wong et al present methods to improve the epilayer quality using intrinsic gettering techniques.

DIELECTRICS AND JUNCTION FORMATION TECHNIQUES

Deposition and properties of ultra-thin dielectric insulators are presented by S. Roberts and others. Various aspects of both, the conventional and implantation techniques for junction formation are discussed. These include doped oxide spin-on source diffusion, and measurement of cross-contamination levels produced during implantation. The ion beam nitridation and a CVD reactor (productivity model) are also given in this section.

PLASMA TECHNOLOGY AND OTHER FABRICATION TECHNIQUES

A wide variety of plasma technology issues are presented in six papers. The topics of these papers include: RIE damage , bonding structure and chemical analysis of PECVD and LPCVD dielectric films, plasma etch emission endpoint, profile control, quality control and optimization during plasma deposition. Also presented in this section are the effects of UV radiation on photoresist in Al etch and palladium silicide contact process.

MATERIAL DEFECTS, OXYGEN AND CARBON IN SILICON

Material defects may be classified in various catagories: bulk defects, surface defects, process-induced defects, deep levels, gettered impurities etc. Most of these catagories are discussed in the papers in this section.Liaw et al and Rose suggest the use of wafer scanners to screen the incoming wafers for defects. Dyer discusses many defects introduced in ingot-to-wafer processing which may lead to device degradation. Shiraiwa and Inenaga explain the haze on wafers. The haze may be due to silicon oxide nodules which grow on the silicon surface in the density of about 1000 to 10 000 per square centimeter. Arst describes a laser-induced mass analysis technique to identify impurities captured in defect structures. Suga and Murai discuss the effects of bulk defects on the intrinsic and extrinsic gettering in silicon.

YIELD ENHANCEMENT AND CONTAMINATION CONTROL ASPECTS

Device yields are dependent upon a number of factors. Processing defects, variability in fabrication, and contamination during device processing are just a few factors which can impact the device yields. These

aspects are discussed in this section. Kar and Tewari attempt to identify the nature of defects induced by e-beam evaporation at the silicon-oxide interface. Maass describes the application of the Generation of Moments method and relates device parameters to processing variables. He shows that tightening the distributions of key device parameters results in an enhancement and prediction of yields. Beck explains that an overall circuit yield is the product of two independent factors, namely, the device physics limitations yield factor and the process defect loss yield factor. The papers on contamination control emphasize the following points: the need to provide a clean environment for fabrication including ultra clean SMIF boxes, dedicated robotic mechanisms and clean air equipment enclosures, particulate control on the wafers and in gases and chemicals.

DOPANT PROFILING TECHNIQUES AND IN-PROCESS MEASUREMENTS

A number of papers were presented on the dopant profiling techniques. These techniques included SIMS, Rutherford backscatter, spreading resistance, and capacitance-voltage. These papers are listed in this section. A workshop was also held on this topic. The synopsis of workshop is given in appendix I.

FAB EQUIPMENT: AUTOMATION AND RELIABILITY

Computer-aided Manufacturing [CAM] and Computerized Integrated Manufacturing [CIM] are discussed in detail in this section. The development of a flexible wafer fab automation system is described. The latter performs three basic functions, real-time inventory control, material distribution throughout the fab, and automated loading of cassette-to-cassette process equipments.

In as much as the automation and mechanization are essential to the future of our industry, so is the understanding of both, the raw capability of each component of a system and the capability of each component with human factors integrated. The paper by Greiner isolates and defines components of real factory time and formulates them in two distinct ways: with and without human interfacing. This paper is the result of a SEMI document, presently in preparation by the SEMI Standards Committee.

Dinesh C. Gupta
Symposium Chairman and Co-Editor