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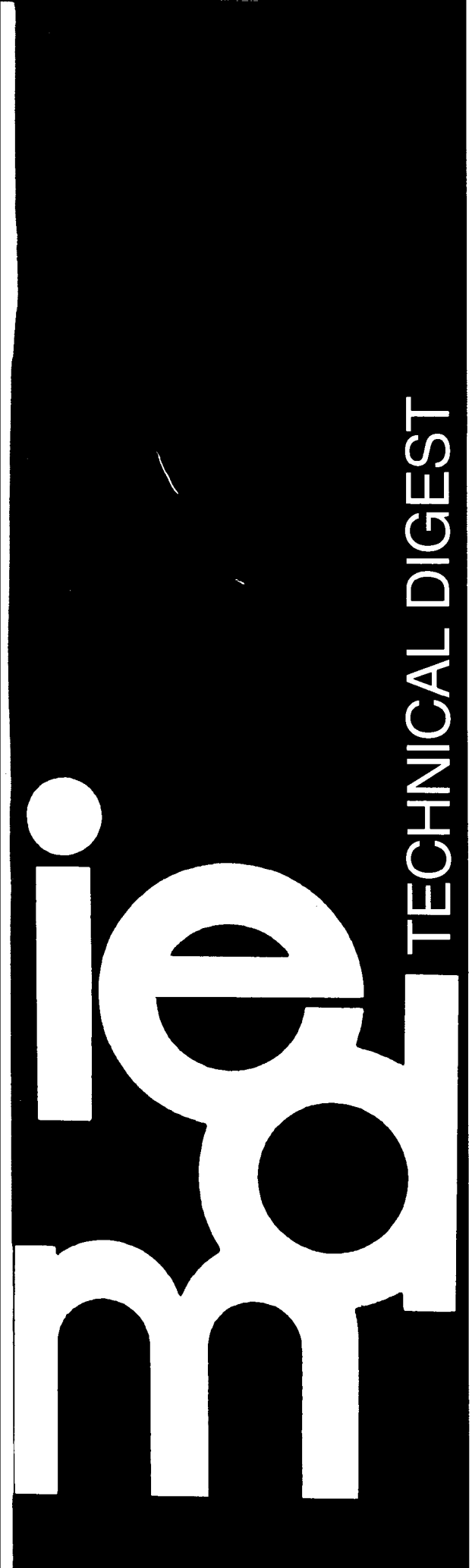
TECHNICAL DIGEST

international ELECTRON DEVICES meeting

2001

WASHINGTON, DC
DECEMBER 2-5, 2001

Sponsored by Electronic Devices Society of IEEE



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IEEE Catalog Number: 01CH37224
ISBN 0-7803-7050-3 (softbound)
ISBN 0-7803-7051-1 (Microfiche Edition)
ISBN 0-7803-7052-X (CD-ROM)
Library of Congress Number: 81-642284

WELCOME FROM THE GENERAL CHAIR

001815

On behalf of the IEDM Committee, I would like to welcome you to the 2001 IEEE International Electron Devices Meeting. This year the conference returns to Washington, DC and continues a long tradition as the leading forum for the presentation of research and development in the area of electron devices and their applications. The strong international nature of our industry and the broad range of topics are evident, with invited speakers and contributed papers from around the world. A total of 595 abstracts were submitted from 28 different countries, with 498 of these abstracts submitted electronically via the World Wide Web. The total number of accepted abstracts was 204. We continue to focus on accessibility to the information in the IEDM abstracts. Short summaries of each abstract are included on the IEDM home page, and we encourage everyone to visit the site at http://www.ieee.org/conference/iedm. This year, the IEDM features digital projection of presentation materials at the conference, for the first time.

Judy Hoyt
General Chair

Two short courses are scheduled for Sunday. These are designed for broad appeal to IEDM participants with material suitable for both newcomers as well as experts in the field. The courses are entitled "Device and Process Technology for sub-70nm CMOS" and "Advanced Memory Technology and Architecture". These courses have been organized by internationally known researchers and will be presented by people active in the respective topics.

The plenary talks on Monday will feature presentations on "How Deep Sub-Micron will Boost Internet Appliances in the Digital Home Network", "Organic and Polymer Semiconductor Devices", and "Future Directions and Technology Requirements of Wireless Communications". Speakers from Europe, North America and Asia will be featured.

Shuji Ikeda
Technical Program Chair

This year the Emerging Technologies session returns to the conference. The session is entitled "Interconnecting Devices," and consists of invited talks from experts in the field. The talks will cover a broad range of emerging technologies all aimed at addressing the challenges of high-speed communication both across a chip and between chips. The session will also serve as a launching pad for a debate on the topic in one of the two Tuesday evening panel sessions, "Interconnecting Devices for the Terabit Era." The second panel discussion is entitled "The 10-nm MOSFET barrier".

The IEDM Luncheon speaker this year will be Dr. Kurt Petersen, President and co-founder of Cepheid. He will be speaking on microfluidics and microelectronic technologies to create revolutionary test systems for DNA analysis. Such devices find applications in cancer research, disease detection, food contamination detection, environmental monitoring, monitoring for biological agents, etc. Dr. Petersen, a "classical EE now immersed in the world of molecular biology," has co-founded several successful companies and is well known as one of the leaders in the silicon MEMS and BioMEMS areas.

Leda Lunardi
Technical Program
Vice Chair

On behalf of the IEEE Electron Devices Society, which sponsors the IEDM, Shuji Ikeda, Technical Program Chair and Leda Lunardi, Technical Program Vice Chair, I wish to express my sincere appreciation and congratulations to the members of the IEDM committee for the outstanding job they have done in planning and organizing the 2001 meeting. The authors are to be commended for their efforts in preparing and presenting the high-quality papers that form the foundation of the IEDM.

It is with great pleasure that I extend a warm welcome to everyone attending the 2001 IEEE International Electron Devices Meeting.

Judy L. Hoyt
General Chair

SB085/02

AWARD PRESENTATIONS

PLENARY SESSION

Monday, December 3

2000 Roger A. Haken Best Student Paper Award
To: Martin Dvorak, Simon Fraser University
For the paper entitled: "Abrupt Junction InP/$GaA_{sx}Sb_{1-x}$/InP Double Heterostructure Bipolar Transistors with F_T as High as 250 Ghz"

Paul Rappaport Award
To: Didier Dutartre, Malgorzata Jurczak, Damien Lenoble, Jose Martins, Stephane Monfray, Roland Pantel, M. Paoli, Jorge Luis Regolini, Pascal Ribot, Thomas Skotnicki, Beatrice Tormen, Centre National d'Estudesdes Telecommunications (CNET), Grenoble, France
For the paper entitled: "Silicon-on-Nothing (SON) --an Innovative Process for Advanced CMOS"

EDS Chapter of the Year Award
To: V. Ramgopal Rao
"To an EDS chapter based on the quantity and quality of the activities and programs implemented by the chapter."

EDS Graduate Fellowships
To: Yee-Chia Yeo, University of California, Berkeley, CA, Sergei Kucheyev, Australian National University, Tusharkanti Ghosh, Lancaster University
"To promote, recognize, and support graduate level study and research within the Electron Devices Society's field of interest"

EDS Distinguished Service Award
To: H. Craig Casey, Jr.
"To recognize and honor outstanding service to the Electron Devices Society and its sponsored activities"

J.J. Ebers Award
To: Hiroshi Iwai
"To honor a single or a series of contributions of recognized scientific, economic, or social significance in the broad field of electron devices"

IEDM LUNCHEON

Tuesday, December 4

2001 Cledo Brunetti Award
To: R. Fabian W. Pease, Stanford University
"For advancing high resolution patterning technologies, high performance thermal management, and scanning electron microscopy for microelectronics"

2001 IEEE Andrew S. Grove Award
To: Al F. Tasch, University of Texas at Austin
"For contributions to MOS technology, and ion planation and device modeling"

2001 IEEE Daniel E. Noble Award
To: Katsutoshi Izumi, Osaka Prefecture University
"For pioneering development of Spearation by Implanted Oxygen (SIMOX) technology"

LUNCHEON PRESENTATION

"MEMS and DNA Analysis: The Road From Device Engineering to Molecular Biology," Dr. Kurt E. Petersen, Cepheid

CONFERENCE HIGHLIGHTS

Date	Time	Room	Event
12/2	9:00 a.m. – 5:30 p.m.	International Ballrooms East and Center	Short Courses
12/3	9:00 a.m. – 12:00 p.m.	International Ballroom	Plenary Session
12/3	6:00 p.m. – 7:30 p.m.	International Ballroom Center	Reception
12/4	12:20 p.m. – 2:00 p.m.	Exhibit Hall	Luncheon
12/4	8:00 p.m. – 10:00 p.m.	International Ballrooms Center and East	Panel Sessions

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Seated from left to right: Yoshihiro Hayashi, Short Course Vice-Chair; Lisa Su, Short Course Chair; Shuji Ikeda, Technical Program Chair; Judy Hoyt, General Chair; Leda Lunardi, Technical Program Vice-Chair; Kaizad Mistry, Publications Chair; Paul Packan, Publicity Chair; Jon Candelaria, Publicity Vice-Chair
First row standing from left to right: Phyllis Mahoney, Conference Manager; Bin Zhao, Integrated Circuits and Manufacturing Subcommittee Chair; H-S Philip Wong, Modeling and Simulation Subcommittee Chair; Laura Rea, Quantum Electronics and Compound Semiconductors Subcommittee Chair; Jeff Welser, Emerging Technologies Chair; Dieter Vook, Detectors, Sensors and Displays Subcommittee Chair; Jong Woo Park, Asian Arrangements Co-Chair; Hiroshi Iwai, CMOS and Interconnect Reliability Subcommittee Chair; Akihiro Nitayama, Asian Arrangements Co-Chair; Hans-Joachim Barth, Process Technology Subcommittee Chair; Melissa Widerkehr, Conference Manager
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Co-Chairs: Robert Chau, Intel Corp.
Greg Timp, University of Illinois

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International Ballroom West

Co-Chairs: Tatsuyuki Saito, Hitachi, Ltd.
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4.2 **Robust 130nm-Node Cu Dual Damascene Technology with Low-k Barrier SiCN,** H. Aoki, K. Torii, T. Oshima, J. Noguchi, U. Tanaka, H. Yamaguchi, T. Saito, N. Miura, T. Tamaru, N. Konishi, S. Uno, S. Morita*, T. Fujii and K. Hinode, Hitachi, Ltd., Tokyo, Japan and *Hitachi ULSI Systems Co., Ltd., Tokyo, Japan — 76

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4.3 **CMP-Free and CMP-Less Approaches for Multilevel Cu/low-k BEOL Integration,** M.H. Tsai, S.W. Chou, C.L. Chang, C.H. Hsieh, M.W. Lin, C.M. Wu, W.S. Shue, D.C.Yu and M.S. Liang, TSMC, Hsin-Chu, Taiwan, R.O.C. — 80

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4.4 **Newly Developed Electro-Chemical Polishing Process of Copper as Replacement of CMP Suitable for Damascene Copper Inlaid in Fragile Low-k Dielectrics,** S. Sato, Z. Yasuda, M. Ishihara, N. Komai, H. Ohtorii, A. Yoshio, Y. Segawa, H. Horikoshi, Y. Ohoka, K. Tai, S. Takahashi and T. Nogami, Sony Corp., Kanagawa, Japan — 84

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4.5 **Integration of Porous Ultra Low-k Dielectric with CVD Barriers,** K. Mosig*+, H. Cox*#, E. Klawuhn**, T. Suwwan de Felipe** and A. Shiota***, *International Sematech, Austin, TX, +Infineon Technologies, Munich, Germany, #Philips, Eindhoven, Netherlands, **Novellus Systems, San Jose, CA and ***JSR Corporation, Tsukuba, Japan — 88

Session 5: Modeling and Simulation – Scaling Trends of Advanced Devices

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Georgetown Room

Co-Chairs: Antonio Abramo, University of Udine
Edwin Kan, Cornell University

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5.1 **The Ballistic FET: Design, Capacitance and Speed Limit,** P.M. Solomon and S.E. Laux, IBM T.J. Watson Research Center, Yorktown Heights, NY — 95

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5.2 **Reduction of Direct-Tunneling Gate Leakage Current in Double-Gate and Ultra-Thin Body MOSFETs,** L. Chang, K.J. Yang, Y.-C. Yeo, Y.-K. Choi, T.-J. King and C. Hu, University of California, Berkeley, CA — 99

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5.3 **3D Analytical Subthreshold and Quantum Mechanical Analyses of Double-Gate MOSFET,** G. Pei, V. Narayanan, Z. Liu and E.C. Kan, Cornell University, Ithaca, NY — 103

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5.4 **Examination of Design and Manufacturing Issues in a 10 nm Double Gate MOSFET using Nonequilibrium Green's Function Simulation,** Z. Ren, R. Venugopal, S. Datta and M. Lundstrom, Purdue University, West Lafayette, IN — 107

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5.5 **Full Quantum Simulation, Design, and Analysis of Si Tunnel Diodes, MOS Leakage and Capacitance, HEMTs, and RTDs,** R. Lake, University of California, Riverside, CA — 111

Session 6: CMOS and Interconnect Reliability – Thin Dielectric Reliability

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Jefferson Room

Co-Chairs: Luca Selmi, DIEGM, University of Udine
Hyeon-Deok Lee, Samsung Electronics

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6.1 **Understanding Soft and Hard Breakdown Statistics, Prevalence Ratios and Energy Dissipation During Breakdown Runaway,** J. Suñe, E.Y. Wu*, D. Jimenez, R.P. Vollertsen** and E. Miranda***, Universitat Autonoma de Barcelona, Bellaterra, Spain, *IBM Microelectronics Division, Essex Junction, VT, **Infineon Technologies, Essex Junction, VT, ***Universidad de Buenos Aires, Bueno Aires, Argentina — 117

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6.2 **Statistical Model for Stress-Induced Leakage Current and Pre-Breakdown Current Jumps in Ultra-Thin Oxide Layers,** R. Degraeve, B. Kaczer, F. Schuler*, M. Lorenzini, D. Wellekens, P. Hendrickx, J. Van Houdt, L. Haspeslagh, G. Tempel* and G. Groeseneken, IMEC, Leuven, Belgium and *Infineon Technologies affiliated at IMEC — 121

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6.4 **Experimental Evidence of Hydrogen-Related SILC Generation in Thin Gate Oxide,** Y. Mitani, H. Satake and A. Toriumi*, Toshiba Corporation, Yokohama, Japan and *The University of Tokyo, Tokyo, Japan — 129

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6.5 **Soft Breakdown Free Atomic-Layer-Deposited Silicon-Nitride/SiO_2 Stack Gate Dielectrics,** A. Nakajima, Q.D.M. Khosru, T. Yoshimoto, T. Kidera and S. Yokoyama, Hiroshima University, Higashi-Hiroshima, Japan **133**

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6.6 **Reliability Evaluation of HfSiON Gate Dielectric Film with 12.8 Å SiO_2 Equivalent Thickness,** A. Shanware, J. McPherson, M.R. Visokay, J.J. Chambers, A.L.P. Rotondaro, H. Bu, M.J. Bevan, R. Khamankar and L. Colombo, Texas Instruments, Dallas, TX **137**

Session 7: Solid State Devices – Nanoelectronic Devices

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Lincoln Room

Co-Chairs: Byung Gook Park, Seoul National University
Andrea Lacaita, Politecnico di Milano

1:35 p.m.
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7.2 **A Multiple-Valued Logic with Merged Single-Electron and MOS Transistors,** H. Inokawa, A. Fujiwara and Y. Takahashi, NTT Corporation, Kanagawa, Japan **147**

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7.3 **Si Single-Electron Transistors with Sidewall Depletion Gates and their Application to Dynamic Single-Electron Transistor Logic,** D.H. Kim, S.-K. Sung, K.R. Kim, B.H. Choi*, S.W. Hwang*, D. Ahn*, J.D. Lee and B.-G. Park, Seoul National University, Seoul, Korea and *University of Seoul, Seoul, Korea **151**

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7.4 **Memory Characteristics of Si Quantum Dot Devices with SiO_2/ALD Al_2O_3 Tunneling Dielectrics,** A. Fernandes, B. DeSalvo, T. Baron*, J.F. Damlencourt, A.M. Papon, D. Lafond, D. Mariolle, B. Guillaumot**, P. Besson**, P. Masson*, G. Ghibaudo***, G. Pananakakis***, F.Martin and S. Haukka+, CEA/LETI, Grenoble, France, *LPM, Villeurbanne, France, **STMicroelectronics, Grenoble, France, ***LPCS, Grenoble, France and +ASM Microchemistry Ltd., Espoo, Finland **155**

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Session 8: Detectors, Sensors and Displays – Photon/Electron Emitting Devices

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Co-Chairs: Min-koo Han, Seoul National University
Kenichiro Suzuki, NEC Corporation

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8.1 **Efficient Organic Light Emitting Diodes and Photodetectors (Invited),** S.R. Forrest, C. Adachi, M.A. Baldo, P. Peumans and M.E. Thompson*, Princeton University, Princeton, NJ and *University of Southern California, Los Angeles, CA **165**

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8.3 **Strong and Efficient Light Emission in ITO/Al_2O_3 Superlattice Tunnel Diode,** A. Chin, C.S. Liang, C.Y. Lin, C.C. Wu and J. Liu*, National Chiao Tung University, Hsinchu, Taiwan and *United Mircoelectronic Corporation, Hsinchu, Taiwan **171**

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8.5 **Field Emitter Arrays for Low Voltage Applications with Sub 100 nm Apertures and 200 nm Period,** D.G. Pflug, M. Schattenburg, H.I. Smith and A.I. Akinwande, Massachusetts Institute of Technology, Cambridge, MA **179**

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8.6 **Simultaneous Conduction Band and Valence Band Electron Field Emission from n-type and p-type Silicon Field Emitter Arrays,** M. Ding and A.I. Akinwande, Massachusetts Institute of Technology, Cambridge, MA **183**

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Co-Chairs: Paolo Lugli, University of Rome
Michael Schlechtweg, Fraunhofer Institute

1:35 p.m.
9.1 **Suppression of Drain Conductance Dispersion in InP-based HEMTs for Broadband Optical Communication Systems,** N. Okamoto, T. Takahashi, K. Imanishi, K. Sawada and N. Hara, Fujitsu Laboratories, Ltd., Kanagawa, Japan **189**

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9.3 **Hetrogeneous Integration: From Substrate Technology to Active Packaging (Invited),** A.S. Brown, N.M. Jokerst, A. Doolittle, M. Brooke, T.F. Kuech*, S.-W. Seo, S. Kang, S. Huang and J.J. Shen, Georgia Institute of Technology, Atlanta, GA and *The University of Wisconsin, Madison, WI **197**

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9.4 **Programmed Electrophoretic Assembly and Heterogeneous Integration of Optoelectronic Devices at Silicon Substrates,** A. O'Riordan, K. Dwane and G. Redmond, NMRC, Cork, Ireland 201

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Session 10: CMOS Devices – Analog-/RF-CMOS

Tuesday, December 4, 9:00 a.m.
International Ballroom East

Co-Chairs: Ralf Brederlow, Infineon Technologies
Toshihiro Sugii, Fujitsu

9:05 a.m.

10.1 **Analog Integration in a 0.35µm Cu Metal Pitch, 0.1 µm Gate Length, Low-power Digital CMOS Technology,** A. Chatterjee, D. Mosher, S. Sridhar, Y. Kim, M. Nandakumar, S.-W. Aur, Z. Chen, P. Madhani, S. Tang, R. Aggarwal, S. Ashburn and H. Shichijo, Texas Instruments, Dallas, TX 211

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10.2 **CMOS Device Optimization for Mixed-Signal Technologies (Invited),** P.A. Stolk, H.P. Tuinhout*, R. Duffy, E. Augendre**, L.P. Bellefroid***, M.J.B. Bolt+, J. Croon**, C.J.J. Dachs, F.R.J. Huisman+, A.J. Moonen+, Y.V. Ponomarev, R.F.M. Roes*, M. Da Rold**, E. Seevinck***#, K.N. Sreerambhatla***, R. Surdeanu, R.M.D.A. Velghe, M. Vertregt*, M.N. Webster*, N.K.J. van Winkelhoff*** and A.T.A. Zegers-Van Duijnhoven*, Philips Research Leuven, Leuven, Belgium, *Philips Research Labs, Eindhoven, The Netherlands, **IMEC, Leuven, Belgium, ***Philips Semiconductors, Eindhoven, The Netherlands, +Philips Semiconductors, Nijmegen, The Netherlands, #Circuit Research International, Eersel, The Netherlands 215

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10.5 **A 50-nm CMOS Technology for High-speed, Low-Power, and RF Applications in 100-nm Node SoC Platform,** K. Ohnishi, R. Tsuchiya, T. Yamauchi*, F. Ootsuka, K. Mitsuda, M. Hase**, T. Nakamura*, T. Kawahara and T. Onai, Hitachi, Ltd., Tokyo, Japan, *Hitachi ULSI Systems Co., Ltd., Tokyo, Japan and **Hosei University, Tokyo, Japan 227

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10.6 **High-Frequency Response of 100nm Integrated CMOS Transistors with High-K Gate Dielectrics,** D. Barlage, R. Arghavani, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros, A. Murthy, B. Roberds, P. Stokley and R. Chau, Intel Corporation, Hillsboro, OR 231

Session 11: Integrated Circuits and Manufacturing – High Performance CMOS Logic Technologies

Tuesday, December 4, 9:00 a.m.
International Ballroom Center

Co-Chairs: Medhi Moussavi, Applied Materials
Kazunari Ishimaru, Toshiba Corporation

9:05 a.m.

11.1 **High Performance 50 nm CMOS Devices for Microprocessor and Embedded Processor Core Applications,** S.-F. Huang, C.-Y. Lin*, Y.-S. Huang*, T. Schafbauer**, M. Eller**, Y.-C. Cheng*, S.-M. Cheng*, S. Sportouch, W. Jin, N. Rovedo, A. Grassmann**, Y. Huang*, J. Brighten**, C.H. Liu*, B. von Ehrenwall**, N. Chen*, J. Chen, O.S. Park**, M. Commons**, A. Thomas, M.-T. Lee*, S. Rauch, L. Clevenger, E. Kaltalioglu**, P. Leung*, J. Chen*, T. Schiml** and C. Wann, IBM Microelectronics, *United Microelectronics Corporation and **Infineon Technologies 237

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11.2 **Highly Stable SOI Technology to Suppress Floating Body Effect for High Performance CMOS Device,** H.S. Kang, Y.W. Kim, K.S. Chung, K.M. Nam, K. Bae, N.I. Lee, C.B. Oh, K.I. Kim, S. Park and K.P. Suh, Samsung Electronics, Kyoungi-Do, Korea 241

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11.3 **A High Performance 0.13 µm SOI CMOS Technology with a 70 nm Silicon Film and with a Second Generation Low-k Cu BEOL,** J.W. Sleight, P.R. Varekamp, N. Lustig, J. Adkisson*, A. Allen*, O. Bula*, X. Chen, T. Chou, W. Chu, J. Fitzsimmons, A. Gabor, S. Gates, P. Jamison, M. Khare, L. Lai, J. Lee, S. Narasimha, J. Ellis-Monaghan*, K. Peterson*, S. Rauch, S. Shukla, P. Smeys, T.-C. Su, J. Quinlan*, A. Vayshenker, B. Ward*, S.Womack, E. Barth, G. Biery, C. Davis, R. Ferguson, R. Goldblatt, E. Leobandung, J. Welser, I. Yang and P. Agnello, IBM Semiconductor Research and Development Center, Hopewell Junction, NY and *IBM Microelectronics, Essex Junction, VT 245

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11.4 **A High Density 0.10µm CMOS Technology Using Low K Dielectric and Copper Interconnect,** S. Parihar, M. Angyal, B. Boeck , D. Reber, A. Singhal, T. Van Gompel, R. Li, B. Wilson, M. Wright, J. Chen, P. Grudowski, Y. Jeon, W. Qi, X. Bai, L. Parker, K. Strozewski, D. Smith, S. Roling, T. Sparks, T. Stephens, F. Huang, R. Mora, M. Amipour, K. Hellig, L. Vishnubhotla, Y. Solomentsev, V. Arunachalam, A. Phillips, K. Junker, S. Filipiak, N. Ramani, M. Turner, M. Rendon, J. Molloy, K. McGuffin, A. Michel, R. Pena, D. Rose, J. Schmidt, M. Smith, M. Wilson, L. Terpolilli, P. Le, J. Sun, R. Ross, K. Yu, M. Hall, P. Ingersoll, M. Woo, G. Yeap and C. Lage, Motorola, Inc., Austin, TX and Advanced Micro Devices, Austin, TX 249

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