Pentium™ Family User's Manual

Volume 1: Data Book

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One good thing

1979 – 8086 and 8088 CPU

leads to another...

1982 – 80286 CPU

and another...

1985 – Intel386™ CPU

and another...

1989 – Intel486™ CPU

and another...

1993 – Pentium™ Processor

1994 – Pentium™ Processor (90 & 100 MHz)

and another...and another...

奔腾™ 系列用户手册

第一卷　数据手册

（英文版）

上海科学普及出版社

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Pentium™ Processor Family User's Manual

Volume 1: Pentium™ Processor Family Data Book

NOTE: The *Pentium™ Processor Family User's Manual* consists of three books: *Pentium™ Processor Family Data Book*, Order Number 241428; the *82496/82497 Cache Controller and 82491/82492 Cache SRAM Data Book*, Order Number 241429; and the *Architecture and Programming Manual*, Order Number 241430. Please refer to all three volumes when evaluating your design needs.

1994

(沪)新登字第 305 号

责任编辑 胡名正

奔腾™系列用户手册
第一卷 数据手册
(英文版)
上海科学普及出版社出版发行
(上海曹杨路 500 号 邮政编码 200063)
上海竟成印刷厂印刷
开本 787×960 1/16 · 印张 39
1994 年 10 月第 1 版 1994 年 10 月第 1 次印刷
ISBN 7-5427-0930-5/TP · 221 定价：85.00 元

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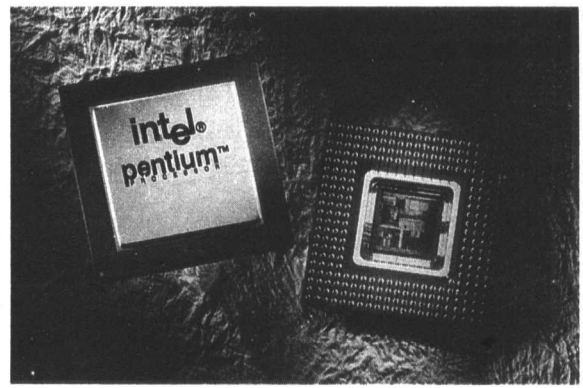
PENTIUM™ PROCESSOR at iCOMP™ INDEX 510\60 MHz
PENTIUM™ PROCESSOR at iCOMP™ INDEX 567\66 MHz

- Binary Compatible with Large Software Base
  - DOS, OS/2*, UNIX*, Windows*
- 32-Bit Microprocessor
  - 32-Bit Addressing
  - 64-Bit Data Bus
- Superscalar Architecture
  - Two pipelined integer units
  - Capable of under one Clock per Instruction
  - Pipelined Floating-Point Unit
- Separate Code and Data Caches
  - 8K Code, 8K Write Back Data
  - 2-Way 32-Byte Line Size
  - Software Transparent
  - MESI Cache Consistency Protocol
- Advanced Design Features
  - Branch Prediction
  - Virtual Mode Extensions
- 273-Pin Grid Array Package
- BiCMOS Silicon Technology
- Increased Page Size
  - 4M for Increased TLB Hit Rate
- Multiprocessor Support
  - Multiprocessor Instructions
  - Support for Second Level Cache
- Internal Error Detection
  - Functional Redundancy Checking
  - Built in Self Test
  - Parity Testing and Checking
- IEEE 1149.1 Boundary Scan Compatibility
- Performance Monitoring
  - Counts Occurrence of Internal Events
  - Traces Execution through Pipelines
- Upgradable with a Future Pentium™ OverDrive™ Processor

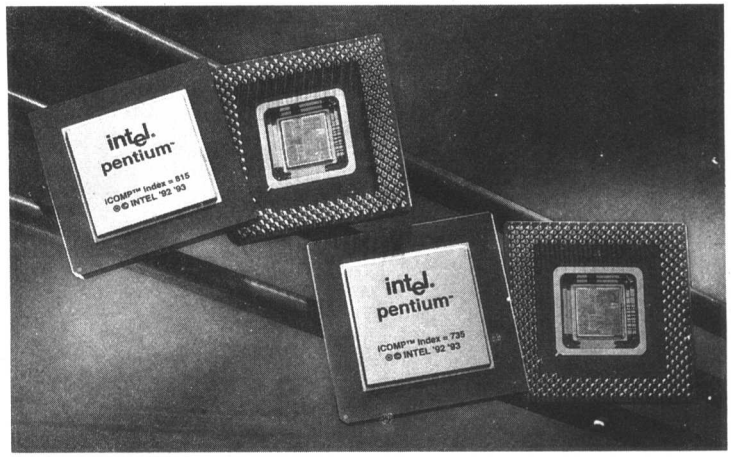
The Pentium™ processor provides the new generation of power for high-end workstations and servers. The Pentium processor is compatible with the entire installed base of applications for DOS, Windows, OS/2, and UNIX. The Pentium processor's superscalar architecture can execute two instructions per clock cycle. Branch Prediction and separate caches also increase performance. The pipelined floating-point unit of the Pentium processor delivers workstation level performance. Separate code and data caches reduce cache conflicts while remaining software transparent. The Pentium processor has 3.1 million transistors and is built on Intel's .8 Micron BiCMOS silicon technology.



PENTIUM™ PROCESSOR at iCOMP™ INDEX 735\90 MHz
PENTIUM™ PROCESSOR at iCOMP™ INDEX 815\100 MHz

- Compatible with Large Software Base
  - MS-DOS‡, Windows‡, OS/2‡, UNIX‡
- 32-Bit CPU with 64-Bit Data Bus
- Superscalar Architecture
  - Two Pipelined Integer Units are Capable of 2 Instructions/Clock
  - Pipelined Floating Point Unit
- Separate Code and Data Caches
  - 8K Code, 8K Write Back Data
  - MESI Cache Protocol
- Advanced Design Features
  - Branch Prediction
  - Virtual Mode Extensions
- 3.3V BiCMOS Silicon Technology
- 4M Pages for Increased TLB Hit Rate
- IEEE 1149.1 Boundary Scan
- Dual Processing Configuration
- Multi-Processor Support
  - Multiprocessor Instructions
  - Support for Second Level Cache
- On-Chip Local APIC Controller
  - MP Interrupt Management
  - 8259 Compatible
- Internal Error Detection Features
- Upgradable with a Future Pentium™ OverDrive™ Processor
- Power Management Features
  - System Management Mode
  - Clock Control
- Fractional Bus Operation
  - 100-MHz Core / 66-MHz Bus
  - 100-MHZ Core / 50-MHz Bus
  - 90-MHz Core / 60-MHz Bus

The Pentium processor (735\90, 815\100) extends the Pentium processor family, providing performance needed for mainstream desktop applications as well as for workstations and servers. The Pentium processor is compatible with the entire installed base of applications for DOS, Windows, OS/2, and UNIX. The Pentium processor (735\90, 815\100) superscalar architecture can execute two instructions per clock cycle. Branch prediction and separate caches also increase performance. The pipelined floating point unit delivers workstation level performance. Separate code and data caches reduce cache conflicts while remaining software transparent. The Pentium processor (735\90, 815\100) has 3.3 million transistors and is built on Intel's advanced 3.3V BiCMOS silicon technology. The Pentium processor (735\90, 815\100) has on-chip dual processing support, a local multiprocessor interrupt controller, and SL power management features.



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ABOUT THIS MANUAL

The *Pentium™ Processor Family User's Manual, Volume 1: Pentium™ Processor Family Data Book* is divided into two parts. Part I, Chapters 1 to 16, contains information pertaining to the entire Pentium Processor family as well as information specific to the Pentium Processor at iCOMP index 510\60 MHz and to the Pentium Processor at iCOMP index 567\66 MHz. Part II, Chapters 17 to 32, contains information that pertains only to the Pentium Processor at iCOMP 735\90 MHz and the Pentium Processor at iCOMP index 815\100 MHz.

The name "Pentium Processor (510\60, 567\66)" will be used in this document to refer to the Pentium Processor at iCOMP index 510\60 MHz and at iCOMP index 567\66 MHz. The name "Pentium Processor (735\90, 815\100)" will be used in this document to refer to the Pentium Processor at iCOMP 735\90 MHz and at iCOMP index 815\100 MHz. "Pentium Processor" will be used in this document to refer to the entire Pentium Processor family in general.

Since the majority of the information in Part I also applies to the Pentium Processor (735\90, 815\100), Part II will be used to describe the additional features and differences of the Pentium Processor (735\90, 815\100) as compared to the Pentium Processor (510\60, 567\66).

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