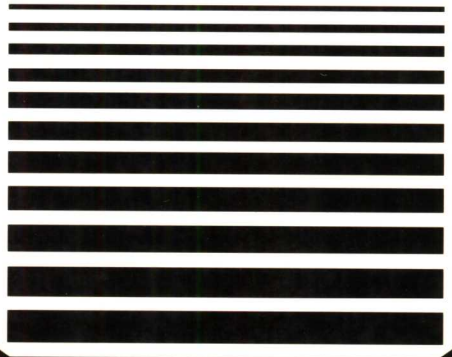
# PROCEEDINGS

## Twelfth Annual IEEE International ASIC/SOC Conference




**15-18 September, 1999**
**DoubleTree Hotel National Airport**
**Washington, DC**

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**Washington, DC**



**Editors**

Ramalingam Sridhar
*University of Buffalo, State University of New York*

Thomas Büchner
*IBM Böblingen Development Lab., Germany*

Ram K. Krishnamurthy
*MRL, Intel Corporation*

The ASIC/SOC Conference is sponsored by the IEEE Solid State Circuits Society and the IEEE Rochester Section

12th Annual IEEE International ASIC/SOC Conference
Digest of Technical Papers

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## WELCOME TO ASIC/SOC

We welcome you all to the 12th Annual IEEE International ASIC/SOC Conference. For the past eleven years, this conference has been a forum for education and dissemination of new ideas related to the ASIC community. The only constant thing in life is change, and as the world of ASICs has seen some significant changes over the last years, the IEEE ASIC conference has been changing as well. The complexity and integration density of custom integrated circuits has increased dramatically, and the old paradigm of ASICs being a rather small part of a whole system is no longer valid.

The 1999 ASIC/SOC conference theme is "The Road to System-on-Chip (SOC)". On this road, we face many important issues such as IP, design reuse, and new establishing technologies like SOI, SiGe and Cu interconnects. ASIC/SOC 99 addresses these topics and presents new methods, ideas, solutions and paradigms for System-on-Chip design and verification.

Once again we were able to put together an outstanding program of great value to the ASIC and SOC Community. Six distinguished speakers from industry and research will provide inside coverage of the latest trends in the field of SOC development and other fields. A panel discussion will address the new challenges that today's and future ASIC and System designers are facing in regard to their qualification and education. Eighteen technical paper sessions with 77 technical paper presentations from 19 countries all over the world will make this conference a truly international event. On the last day of the conference, six carefully selected half-day tutorials will offer in-depth coverage of the most important areas in ASIC and SOC design and verification, helping you to stay both effective and innovative in this highly competitive world.

Our keynote speech titled "System on a Chip in the Internet Economy" is by Wilfred J. Corrigan, Chairman and chief executive officer of LSI Logic Corporation, which refers itself as "The System on a Chip Company". The keynote is followed by talks from three internationally renowned experts in Gigascale integration, System-on-Chip Test and Microsystems integration, Professor James D. Meindl, Dr. Yervant Zorian and Professor Kensall D. Wise. All these topics are highly relevant and important to the topic of our theme. Also, we have distinguished speakers for Banquet on Thursday and luncheon on Friday.

We thank our distinguished speakers, the authors of our technical papers, and the workshop presenters for their invaluable contributions in making this conference a great success.

We also thank all the volunteers who are technical experts in various areas of ASIC/SOC and have helped the conference by participating in the organizing committee, technical committee and the steering committee. Their tireless efforts through numerous ways in improving the quality of the event is greatly appreciated. We thank Ms. Wendy Walker and Widerkehr Associates for their excellent service in managing this conference and for their prompt attention to the conference details. Finally, we thank our attendees, for helping us make significant contribution to the ASIC/SOC community at large.

With the revised focus of the ASIC Conference to include SOC, we hope that this conference and its proceedings will be even more valuable to the ASIC/SOC professionals on the road to a new millennium.

Sincerely,

Ramalingam Sridhar, General Chair
Tom Büchner, Technical Program Chair
Robert Frye, Technical Program Co-Chair.

# PROGRAM-AT-A GLANCE

| | |
|---|---|
| **Wednesday, September 15** | |
| Conference Registration | 7:00 a.m. - 5:00 p.m. |
| Plenary Session | 8:15 a.m. – 12:15 p.m. |
| Lunch Break | 12:15 p.m. – 1:30 p.m. |
| Technical Program | 1:30 p.m. - 5:15 p.m. |
| Panel Discussion | 5:30 p.m. – 7:00 p.m. |
| **Thursday, September 16** | |
| Conference Registration | 7:30 a.m. - 5:00 p.m. |
| Technical Program | 8:15 a.m. - 5:40 p.m. |
| Lunch Break | 12:00 p.m. - 1:30 p.m. |
| Conference Reception | 5:40 p.m. – 6:30 p.m. |
| Conference Banquet | 6:30 p.m. – 8:30 p.m. |
| **Friday, September 17** | |
| Conference Registration | 7:30 a.m. - 3:30 p.m. |
| Technical Program | 8:15 a.m. – 3:20 p.m. |
| Conference Luncheon | 12:10 p.m. - 1:40 p.m. |
| **Saturday, September 18** | |
| Tutorial Workshops (Morning Sessions) | 8:00 a.m. – 12:00 p.m. |
| Tutorial Workshops (Afternoon Sessions) | 1:00 p.m. – 5:00 p.m. |

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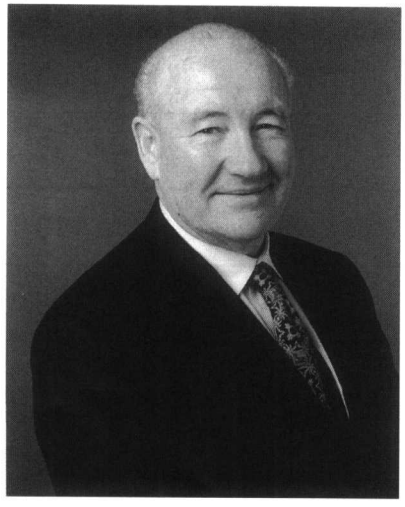
**Front Row (left to right)**

Paul Lee, Raju Damarla, Thomas Büchner, Ramalingam Sridhar, Robert Frye, Cherrice Traver, John Chickanosky

## Keynote Speech

# System on a Chip in the Internet Economy



Wilfred J. Corrigan
Chairman and CEO
LSI Logic Corporation

Wilf Corrigan is chairman and chief executive officer of LSI Logic Corporation, Milpitas, California. Prior to founding LSI Logic in 1981, Mr. Corrigan was president, chairman and chief executive officer of Fairchild Camera and Instrument Corporation in Mountain View, California. He joined Fairchild in August 1968 and held a series of management positions before becoming president and CEO in July 1974. The position of chairman was added in May 1977. Before joining Fairchild, he was director of Transistor Operations at Motorola Inc.'s Semiconductor Products Division in Phoenix, Arizona.

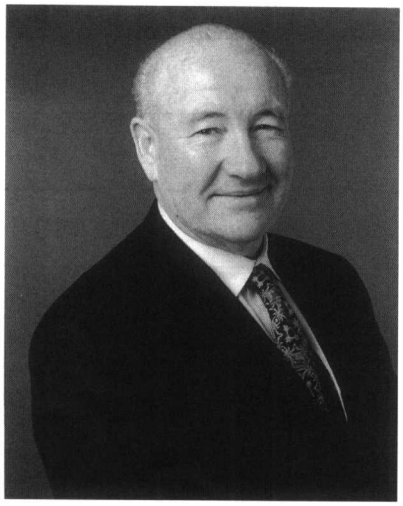
Mr. Corrigan graduated from the Imperial College of Science, London, England in 1960 with a bachelor of science degree in Chemical Engineering. In addition, he holds an honorary degree, Doctors of Laws, from the University of Calgary, Canada. Mr. Corrigan was born in Liverpool, England and is now a U.S. citizen.

Mr. Corrigan is a director and past chairman of the Semiconductor Industry Association. He is a member of the Board of Directors for the Silicon Valley Manufacturing Group, Silicon Power Corporation and LucasArts Entertainment Company.

In October 1998, Mr. Corrigan received the highest honor in the U.S. semiconductor industry---the Robert N. Noyce Award. The Noyce Award recognizes the lifetime achievements of leaders in the chip industry. Mr. Corrigan was recognized as a technology innovator, industry risk-taker, and political entrepreneur who helped bring the semiconductor industry to international prominence.

## Keynote Speech

# System on a Chip in the Internet Economy



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## Summary

Throughout the past four decades, semiconductor technology has advanced at exponential rates in both productivity and performance. The most revealing productivity metric, the number of transistors per chip at a virtually constant chip cost, indicates an improvement of over eight orders of magnitude. The single most revealing performance metric, the signal energy transfer per binary switching transition, reveals an enhancement of over six orders of magnitude. In the real world, such exponential advances do not continue endlessly. Consequently, the salient feature of this discussion is a systematic assessment of early XXI century opportunities and persistent limits on a gigascale system-on-a-chip (GSoC). The central thesis of this assessment is that a hierarchy of limits will govern opportunities for a GSoC. The five levels of this hierarchy can be codified as fundamental, material, device, circuit and system.
Fundamental limits are derived from virtually immutable physical laws of thermodynamics, quantum mechanics, electromagnetics and information theory.

Key material limits based upon silicon switching energy, transit time and thermal conduction have been and are very likely to remain highly important and highly persistent. An interesting newly critical yet intrinsic semiconductor material limit is imposed by random placement of dopant atoms. Interconnect materials impose a virtually unbreakable time-of-flight limit and a key relaxation time limit (or resistivity-permittivity product) that strongly suggests cooling of conductors in order to reduce resistivity.

Key MOSFET device limits indicate opportunities to scale bulk devices with retrograde channel doping profiles to the sub-50nm range and very thin channel SOI devices to the sub-25nm range. These channel lengths will then determine the key MOSFET switching energy and transit time limits, although 25nm SOI MOSFETs will be constrained by parameter fluctuation limits to use essentially undoped channels. Key device-level interconnect limits are imposed by response time and crosstalk which will be aggravated by increasing copper resistivity due to film thickness becoming smaller than the mean free path of electrons in copper.

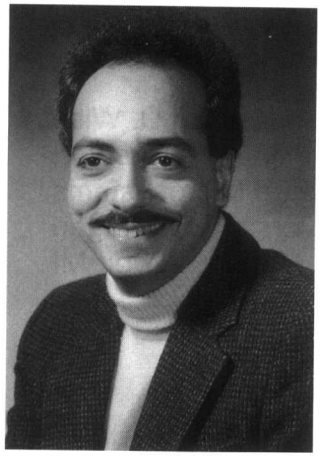
Five critical circuit limits are imposed by the static transfer characteristic, the switching energy and the propagation delay time of a CMOS logic gate and the response time and crosstalk of a global interconnect circuit exhibiting significant inductive effects at GHz clock frequencies. Greater than 60% increases in crosstalk in global interconnects for a multi-GHz GSoC can be projected.

System limits are the most restrictive constraints of the hierarchy. The most critical generic system limits are imposed by the architecture of a GSoC, the switching energy of the semiconductor technology, the heat removal capacity of the packaging technology, the clock frequency and the sheer physical size of the chip itself. In order to benefit from continued performance improvements derived from further MOSFET scaling, it is imperative to keep interconnects short for the critical paths of a future high performance GSoC.

Beyond the 15 year horizon of the 1999 International Technology Roadmap for Semiconductors, it appears that the Si GSoC will persist as the dominant electronic technology of the information revolution for the first half of the 21st century as steel remained the dominant structural technology of the industrial revolution during the first half of the 20th century.

# Plenary Speech

## *System-on-Chip Test Strategies*



Yervant Zorian
Chief Technology Advisor
Logic Vision, Inc. and
Editor in Chief
IEEE Design & Test of Computers

Yervant Zorian is the Chief Technology Advisor of LogicVision Inc. Previously, he was a Distinguished Member of Technical Staff at Bell Labs, Lucent Technologies, responsible for developing embedded test strategies for cores, chips and multi-chip modules. He received an MSc degree in Computer Engineering from the University of Southern California, a PhD in electrical engineering from McGill University.

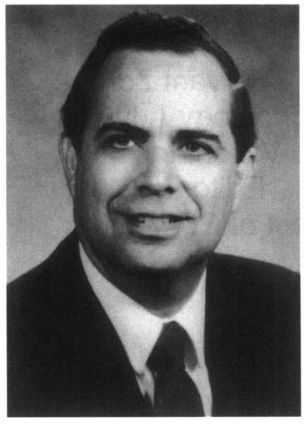
Dr. Zorian is currently serving as the Editor-in-Chief of the IEEE Design & Test of Computers and as the Chair of the Test Technology Technical Council (TTTC) of IEEE Computer Society. He is the founder and chair of the IEEE International Workshop on Testing Embedded Core-based Systems (TECS) and the IEEE P1500 Embedded Core Test standardization Working Group. He holds several U.S. patents and has published more than one hundred papers and two books. Dr. Zorian received a number of best paper awards and is a Fellow of IEEE.

## Summary

As system-on-chip (SOC) complexity and the move to very deep submicron (VDSM) technology pushes the threshold of semiconductor technology, conventional test methods become inadequate and costly. This new level of complexity and VDSM scaling trends such as complexity, performance, and density have major implications on testing SOC chips. The industry has identified a number of challenges as a result of such implications. Solving these challenges require new approaches to test, such as embedded test. Embedded test enables customers to produce higher-quality products in less time. The use of embedded test raises margins and significantly reduces the time required for system verification, test and debug. The speaker will address core-, chip- and board- level test and debug issues, test technologies, SOC integration /test issues - making SOC a reality, and the importance of embedded test and front-end (time to money, quality and cost).

## Plenary Speech

# *INTEGRATED MICROSYSTEMS: Merging MEMS, Micropower Electronics, and Wireless Communications*



Kensall D. Wise
Director,
Center for Integrated Microsystems
University of Michigan
Ann Arbor, MI

Kensall D. Wise received the BSEE degree with highest distinction from Purdue University in 1963 and the MS and Ph.D. degrees in electrical engineering from Stanford University in 1964 and 1969, respectively. From 1963 to 1965 (on leave 1965-1969) and from 1972 to 1974, he was a Member of Technical Staff at Bell Telephone Laboratories, where his work was concerned with the exploratory development of integrated electronics for use in telephone communications. From 1965 to 1972 he was a Research Assistant and then a Research Associate and Lecturer in the Department of Electrical Engineering at Stanford, working on the development of integrated circuit technology and its application to solid-state sensors. In 1974 he joined the Department of Electrical Engineering and Computer Science at the University of Michigan, Ann Arbor, where he is now the J. Reid and Polly Anderson Professor of Manufacturing Technology and Director of the Center for Integrated MicroSystems. His present research interests focus on the development of solid-state sensors for applications in health care, transportation, environmental monitoring, and semiconductor process control.

Dr. Wise organized and served as the first chairman of the Technical Subcommittee on Solid-State Sensors of the IEEE Electron Devices Society (EDS). He served as General Chairman of the 1984 IEEE Solid-State Sensor Conference, as Technical Program Chairman of the 1985 International Conference on Solid-State Sensors and Actuators, and as IEEE-EDS National Lecturer for 1986. He has also served on many program committees for the International Electron Devices Meeting and the International Solid-State Circuits Conference, was General Chairman of the 1997 IEEE International Conference on Solid-State Sensors and Actuators, and is a member of the United States National Academy of Engineering. Dr. Wise received the IEEE/EDS Paul Rappaport Award (1990), a Distinguished Faculty Achievement Award from the University of Michigan (1995), the Columbus Prize from the Christopher Columbus Fellowship Foundation (1996), the SRC Aristotle Award (1997), and the 1999 IEEE Solid-State Circuits Field Award. He is a Fellow of the IEEE and the AIMBE.

# *INTEGRATED MICROSYSTEMS:*
## *Merging MEMS, Micropower Electronics, and Wireless Communications*

Kensall D. Wise

*Center for Integrated MicroSystems*
Department of Electrical Engineering and Computer Science
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### ABSTRACT

Integrated microsystems merging microelectro-mechanical systems (MEMS), micropower integrated circuits, and, in some cases, wireless communications are developing rapidly for a wide variety of applications. Since the start of MEMS activity in the late 1960s, pressure sensor figures of merit have improved by factors of more than 40,000, now offering sub-mTorr resolution and dynamic ranges reaching five orders of magnitude. Silicon accelerometers range from micro-g to kilo-g levels while integrated gyros have reached tactical-grade and are driving toward inertial-grade performance. Scanning force microscopes have revolutionized surface science and tactile imagers may soon make electronic fingerprint readers possible for banking and security applications. In addition, many integrated transducers for optical, thermal, magnetic, and chemical parameters are emerging, including micromirror-based projection displays, IR/thermal imagers, inkjet print heads, read heads for ultra-high-density mass storage, and conductivity/calorimetric chemical sensors. Using embedded microprocessors, modular microsystems employing self-testing and digital compensa-tion promise to achieve levels of reliability and accuracy previously impossible at low cost. This paper reviews the state-of-the-art in this area and some of the challenges for the coming decade.

### INTRODUCTION

During the past thirty years, a continuing series of advances have carried microelectronics to ever higher levels. Monolithic logic chips, operational amplifiers, memory, microprocessors, data converters, digital signal processors, microcomputers, and a wide variety of ASICs have been the focus as the industry has expanded to meet market needs. Personal computers are now having a fundamental impact on society, producing a worldwide explosion in the processing and communication of information. Most of this information is still entered by typing, optical scanning, or voice, and is eventually displayed for use by another individual. Looking ahead, however, many of the functions needed for future systems involve enhancing the ability to gather information into this worldwide network and use it for control. Thus, a major emphasis will be on microsystems that can interface to the non-electronic world and monitor/control the environment around us. The key devices for these microsystems are the sensors and actuators that perform the transduction function. This is the present-day world of MicroElectroMechanical Systems (MEMS) [1,2]. Activities in this emerging area will complete the pervasiveness of electronics in society and will significantly magnify its markets and impact in the years ahead.

Pressure sensors were the first integrated silicon sensors to see high-volume production and were the first to demand a batch technology for selectively forming thin high-yield diaphragm structures at low cost. This 'bulk micro-machining' technology used wet anisotropic etchants and impurity-based etch-stops to achieve high-yield. During the early 1980s it also permitted sensors for flow and acceleration to be demonstrated. By the late-80s, surface micromachining [3] had emerged and was being applied to accelerometers, driven by the needs of the automotive industry for airbag deployment and adaptive suspension systems. Initial efforts on the development of microactuators were also underway. By the early 90s, a wide variety of additional devices were in development, including gyroscopes, tips for scanning probe microscopy, microvalves, inkjet print heads, projection displays, gas chromatography systems, and read heads for high-density mass storage. The technology was coming of age and was sparking revolutionary advances in many areas.

### DEVICE OPTIONS

Figure 1 shows three basic device options available for MEMS. Bulk micromachining, as discussed above, usually requires the use of an impurity-based etch-stop along with a deep etch from the back of the wafer. As wafer sizes and thicknesses have increased, this etch has become increasingly difficult. Front-side processes that undercut the micro-structure are simpler, compatible with foundry processes, and

typically require no modification of the process flow except for a final etch just prior to die separation. They are not applicable to all device structures but are useful with many. In surface micromachining [4], a sacrificial layer (usually PSG) is deposited on the wafer and patterned. The intended microstructure material (polysilicon or metal) is deposited over it and is patterned so that it anchors to the wafer over the ends of the sacrificial material, which is subsequently removed to leave a beam, cantilever, or diaphragm. Such devices have been used for accelerometers, for pressure sensors (using seals provided by CVD dielectrics), and for other microstructures. Control of stress in the deposited layer is important, and with polysilicon high-temperature (>1000°C) anneals are generally required.

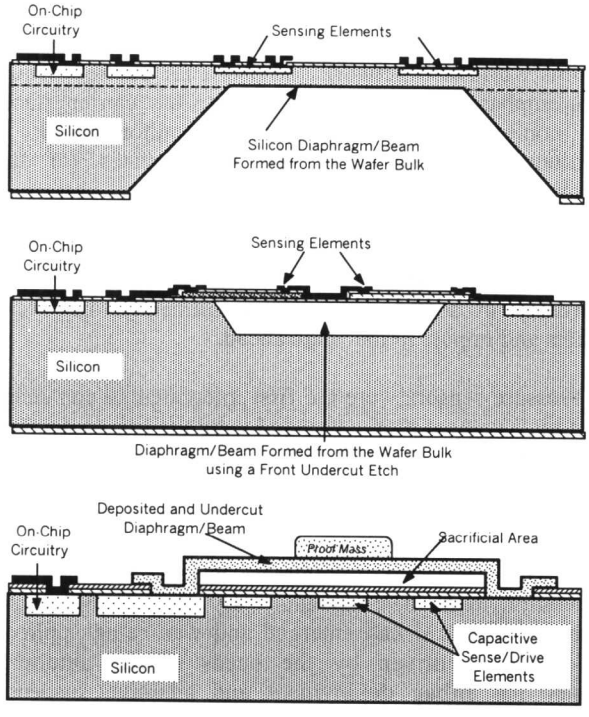



Fig. 1: Three basic device structures for use in microsystems: bulk micromachined diaphragm or beam (above); front-etched undercut bulk microstructure (middle); and surface micromachined beam (below).

Merging integrated circuits with bulk- and surface-micromachined transducers is increasingly common. For bulk micromachining, the etch-stops are formed prior to the circuit fabrication sequence. After circuit processing, special metal or an overlay of LTO to protect more standard metal (e.g., Al) from the subsequent silicon etch is normally required. This silicon etch is performed at the end of the process, where it can also aid in die separation. In surface micromachining, the extra steps for transducer formation are performed after circuit fabrication. In this case, the wafer must be sealed with a conformal nitride layer since the release etch in HF (when PSG is used as the sacrificial layer) can be quite long. Since final release is performed prior to die separation, the microstructures must be protected during this step. Surface micromachining has an advantage over bulk processes in that it is more easily added to standard process flows, and it is available from foundry services today. However, since most deposited layers are quite thin, the masses and capacitances associated with such structures (including interdigitated combs [5]) are very small (in some cases, sub-fF). While both surface- and bulk-micromachined accelerometers are in production for automotive applications [6,7], for higher sensitivity bulk structures will have an advantage because of their higher capacitances and masses, especially when fabricated using deep dry etching [8] and trench refill processes [9]. In both surface and bulk structures, electrostatic self-test is being used.

## PRESSURE SENSORS

Of all the device types, mechanical transducers have seen the most impact from MEMS and pressure sensors are the most developed. In order to put in perspective the progress made here, it is useful to define a figure of merit for these devices, recognizing that some factors will be more important than others in any given application. We will define this figure of merit as

$$F_m = \frac{SD_R}{Pt_D \$ T_d}$$

where S is the output pressure sensitivity, $D_R$ is the output dynamic range, P is the power dissipation, $t_D$ is the readout time, \$ is the device cost, and $T_d$ is the ambient temperature drift. In the early days, pressure sensors were simple piezoresistive bridges fabricated in thinned silicon. Die attach was difficult, and package-induced stresses were significant and unpredictable. The devices were of limited accuracy and suffered from poor diaphragm thickness control. Assuming values of 20ppm/mmHg, 1000mmHg, 12.5mW, 10μsec, 2, and 80ppm/°C for the above parameters, respectively, yields a convenient value of one for our figure of merit, $F_m$. The situation improved significantly with the introduction of a built-in micromachined rim, as shown in the devices of Fig. 2 [10]. The package-induced stresses were greatly reduced.

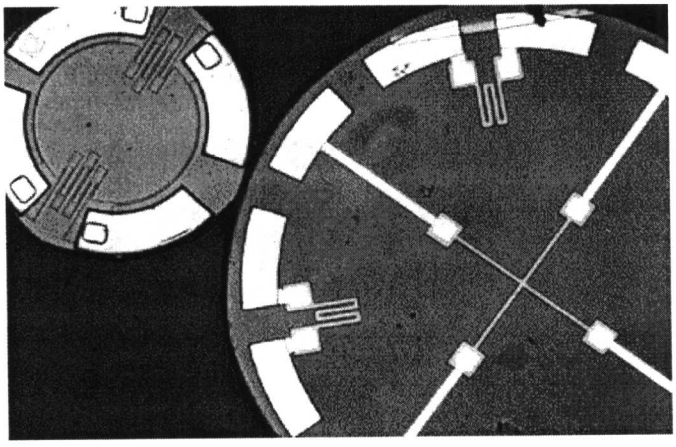


Fig. 2: Micromachined piezoresistive pressure sensors developed for cardiovascular catheters. The smaller device has a diameter of 800μm. They were the first to use a built-in thick rim.

The next development was the use of a buried-layer boron etch-stop, which reduced the variations in diaphragm thickness and permitted thinner diaphragms to be used. This improved yield substantially, increased the sensitivity, and lowered the dynamic range. Taking parameters of 80ppm/mmHg, 500mmHg, 12.5mW, 10μsec, 0.2, and 80ppm/°C, the figure of merit is about 20 for these devices. In the mid-1970s, capacitive pressure sensors were introduced based on wafer bonding and were shown to improve the pressure sensitivity and reduce the temperature sensitivity for the same diaphragm size. They also required circuitry in close proximity to the transducer to suppress/manage lead parasitics. The power dissipation of such devices is limited to that of the readout circuitry, and using switched-capacitor charge integrators, readout in 5μsec at 1mW is possible. Taking 1000ppm/mmHg, 250mmHg, 1mW, 5μsec, 0.2, and 50ppm/°C, the figure of merit jumps to 5000. Using digital compensation to allow use over a highly non-linear response range [11] and improved compensation for temperature effects, still further advances are possible. Using 10,000ppm/mmHg, 1000mmHg, 1mW, 100μsec (compensation time), 0.5, and 5ppm/°C, the figure of merit becomes 40,000.

More recent advances in pressure sensors are illustrated by the multi-element barometric pressure sensor [12] shown in Fig. 3. The device employs bossed silicon diaphragms approximately 1mm in diameter, 2μm thick, and produced using a dissolved-wafer process on glass. By staggering the diaphragm diameters, one device spans the entire barometric pressure range (e.g., 500 to 800 Torr) while separate segment devices cover 50Torr subranges with much higher sensitivity. As pressure increases, the diaphragms deflect according to their diameters and then bottom out against the glass, which serves as an overpressure stop. At least one diaphragm is always operating in its highest sensitivity range with a very narrow gap. The resulting resolution is 25mTorr or about 15b, equivalent to an altitude difference of about one foot at sea level. The devices are vacuum sealed at wafer level. Pressure sensors continue to evolve, with applications ranging from high-sensitivity silicon microphones to embedded tire pressure sensors and devices for use in hydraulic controls.

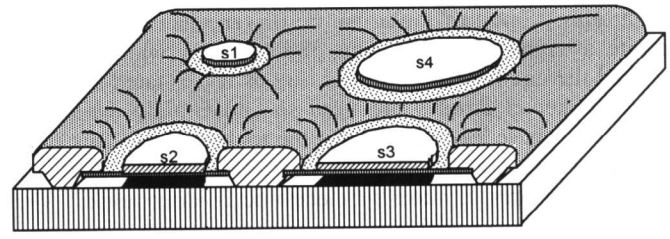



Fig. 3: A multi-element capacitive barometric pressure sensor.

## ACCELEROMETERS AND GYROS

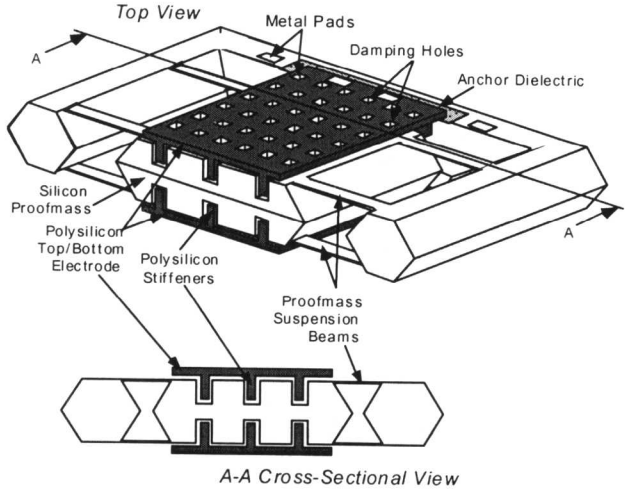
A great deal of activity over the past several years has focused on accelerometers [13]. Microstructures range from vertically-deflecting cantilever structures to lateral interdigitated comb devices. Most piezoresistive devices utilize bulk micromachining and offer sensitivities of around 1-2mV/g over a 20-50g range with an uncompensated temperature coefficient of sensitivity of <2000ppm/°C. Capacitive accelerometers can be bulk micromachined cantilever structures with electronics realized on hybrid chips [7] or surface-micromachined structures with on-chip electronics [14]. In order to increase the bandwidth and dynamic range of comb devices, closed-loop readout circuitry can be used to force-balance the moving element, reading out the feedback voltage. It is possible to detect capacitance variations of <1aF. One of the best known of the surface micromachined capacitive accelerometers is the ADXL50 from Analog Devices, which offers a 0.5mg/Hz noise floor with a range of ±5g and a shock survivability of 1000g.

Accelerometers are rapidly being scaled down from 1-100g devices to the milli-g and μ-g ranges and are expected to reach the inertial arena, where they should find wide use in tandem with GPS. To achieve these sensitivities, it is important to increase the proof mass, which makes bulk micromachined approaches attractive. The all-silicon capacitive device shown in Fig. 4 is an example of this approach [13]. Here, the proof mass is realized from the wafer bulk and is supported by eight p++ suspension beams. Trenches are etched in the proof mass using deep high-aspect-ratio RIE and are refilled to form an upper sensing electrode that is anchored to the chip rim. When the sacrificial dielectric spacer between the proof mass and the polysilicon electrode is removed, the resulting capacitor has a gap of only about 1.4μm and a sensitivity of over 5pF/g. Together with a companion readout chip [15], the noise floor is consistent with a resolution of less than 5μg.

One of the newer mechanical devices is the rate-of-turn sensor or gyro [13,16] as shown in Fig. 5. Here an electroplated nickel ring approximately 6μm high and 1mm in diameter is suspended above a silicon wafer by semicircular support struts anchored the substrate via a central post. Surrounding the ring are a number of fixed electrodes. Some of these can be driven electrostatically to excite a vibration in the ring, the lobes of which precess around the circumference of the ring as it is rotated about its axis. Other electrodes are used to capacitively detect the position of these lobes and hence the rotation rate. This first-[generation ring gyro achieved a resolution of 0.5°/sec in a 25Hz bandwidth, limited by electronic readout noise. The zero-bias drift was <10°/sec over the temperature range of –40 to +85°C [16]. Second-generation all-silicon devices are expected to reach tactical-grade performance, with a random walk as small as 0.05°/h. Like their accelerometer cousins, gyros are improving rapidly, moving toward seismic and inertial-grade performance.

## OTHER DEVICES

A second major device type developed in the mechanical arena is the flow sensor. These devices operate using both thermal (hot wire anemometry) [17] and pressure-based [11] designs. The former use heated filaments suspended on a dielectric microstructure and fabricated using bulk micromachining. Typical devices resolve flow velocities from less than 1cm/sec to several m/sec. Pressure designs measure the drop across micromachined flow tubes and can resolve as low as $10^{-8}$ SCCM. Thermal devices have also been used as micro-Pirani gauges [18], sensing pressure by measuring thermal losses through the surrounding gas.



A-A Cross-Sectional View

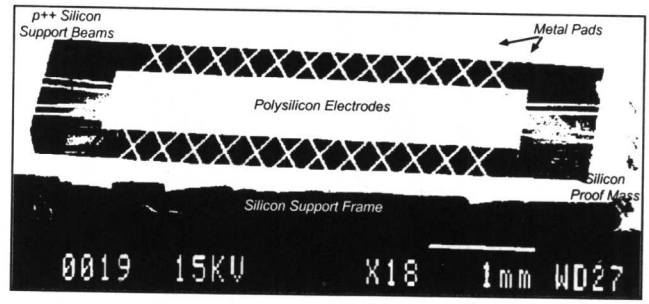


Fig. 4: Diagram of an all-silicon capacitive μg accelerometer. The device is formed using a bulk silicon proof mass and sensing electrodes produced by a DRIE poly-refill process. The proof mass is 4mm x 1mm. *(Courtesy K. Najafi, University of Michigan)*

There are a wide range of additional devices currently in development. One example is a tactile imager for reliably sensing fingerprints,. Such devices are increasingly needed for identity verification in financial transactions and for a wide range of security applications. They require a resolution of about 500dpi, or a pixel size of about 50μm. Figure 6 shows a small prototype of such an array [19]. It is x-y organized and consists of silicon row lines and orthogonal metal column lines on glass. The row lines are driven in voltage while the charges induced through the capacitive row-column crosspoints are sensed with switched-capacitor charge integrators. For a full 256x256-element array at 500dpi, the crosspoint capacitance is 10fF, the maximum capacitance change is 30fF, and the calculated total noise charge is about 7fC, making reliable operation appear possible. The devices would be covered by a metallized polymer film to protect against moisture and allow cleaning of the array.

A wide number of thermal devices have been developed based on mechanical microstructures. Recent progress in uncooled silicon thermal imagers is particularly exciting. Using bulk micromachined dielectric windows or surface undercut dielectric plates to provide thermal isolation for thermopile or microbolometer transducers, 1K-pixel area arrays for process control applications [20] and 80K-pixel imagers for night vision applications [21] have been reported. NETDs are less than 0.05°C [21], and active-pixel micromachined IR detectors have reported responsivities of more than $10^6$V/W [22]. In addition, many of the more successful microvalves have employed thermal-bimetallic or thermopneumatic actuation. Such structures have the ability to develop reasonable forces/pressures with deflections in the tens of microns. For example, a thermopneumatic structure has been reported that develops 2ATM in <100msec with a power input of only 20mW [23]. Thermally-driven inkjet print heads [24] also represent a high volume application for the technology that could soon allow color printing at low cost with a resolution of over 1000dpi.