computer science and multiple-valued logic

theory and applications

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preface

This preface briefly acquaints the reader to the book and its preparation, whereas the introductory chapter introduces the reader to the area of multiple-valued logic and how and why it has become related to computer science.

This book is aimed at those computer engineers, computer scientists, applied mathematicians and physicists who are not experts in the area of multiple-valued logic as the discipline pertains to computer engineering and computer science. Thus its primary goal is to convince these people that multiple-valued logic is indeed both intellectually challenging and practically applicable.

It was decided in conversations with a number of engineers, computer scientists and potentially interested people including design engineers that several outstanding scientists, luminaries capable of explaining our basic concepts in an interesting way, should be asked to write an updated 'handbook' of ideas contained in the better papers. With the exception of a handful of good classical works by Epstein this expectation has been carried out.

Many new developments have recently taken place in computer science and multiple-valued logic. For example, computer device technologies along with (V)LSI circuit design and testing considerations are new and extremely important fields. In fact, there is a good chance that the impact of multiple-valued testing and verification considerations will be at least as important as device and circuit considerations in the use and design of fifth and sixth generation computing and data processing systems.

The organization of this documentary is top-down in its design in that the book is divided into five parts, after a summary introduction.

I Algebraic theory.

II Logic design and switching theory.

III Threshold logic design.

IV *Physical components and implementations.*

V Applications and implementations

Each part has been broken down into several monographs or chapters, each chapter having been designed by one or more scientists. However the flow and sense from chapter to chapter is continuous. The flow between parts has been made continuous by means of introductory remarks and conclusions for each section.

The Introduction (Chapter 1) provides the new reader with interesting foundations, history and motivation for considering multiple-valued logic design and applications from both intellectual and practical points of view. No particular advanced technical background is assumed of the reader; likewise, the first portion of each monograph is written in such a way that important concepts or reasons for considering a given area can be grasped by each new reader. Since the book relates to computer science and engineering, many interesting considerations from ancient

history have not been mentioned due to lack of space. However, a conspectus on the history can be found in Rescher[41]. A short but precise historical summary of multiple-valued logic as it is related to computer science can be found in a paper by Epstein, Frieder, and Rine [14], as well as in surveys by Vranesic, Smith et al [59] Papers which could date the beginning of multiple-valued logic and modern digital computer systems are those of Grosth [20] and Metze [31].

Part I on algebraic theory gives the applied mathematical foundations for much of multiple-valued logic as related to computer science. The reader who is either partially familiar with these interesting relations or who is more immediately interested in only logic design and switching theory may wish to turn directly to Part II. Modern axioms and properties of Post algebras are nicely summarized by Traczyk[54], a Polish scientist; while Surma[53] presents a general algorithm for axiomatizing every finite logic. Relationships between Post and Boolean algebras have been studied by Wojcik and Metze[60, 61]. Completeness properties of multiple-valued logic and switching theory have been documented by Rosenberg[45] and Patt[35]. Abstractions and extensions of Post algebras have recently been introduced by Epstein[11, 12, 14], one interesting concept being that of a P-algebra; Epstein has, also, given an important equational axiomatization for the disjoint system of Post algebras[13]. Interestingly enough, Nutter, Swartwout, and Rine[37] have shown that many multiple-valued logic algebras are isomorphically equivalent to Post algebras.

Part II of this book covers logic design and switching theory. This section gives important models for computer subsystems and evaluates multiple-valued logic design criteria directly related to cost. Initially, applications of multiple-valued logic systems to circuits were studied by Metze[31] and Yoeli and Rosenfeld[62]. Since various algorithms for minimizing Boolean logic systems, for example the Quine–McCluskey technique, have been of interest, it must be noted that much research has also been directed toward the "minimizing" of multiple-valued logic systems. While this general problem is still open and is far more difficult for the multiple-valued logic cases and presents itself as a "can-of-worms", computer minimization techniques have seen partial success through the ongoing work of Allen and Givone[3], Su and Cheung[52], W. R. Smith[50], and Ostapko, Cain, and Hong[38]. Hazards and cost analyses of hazard-free logic systems have always been an important topic of investigation in computer engineering. DuCasse and Metze[10] and others[24] are studying this problem. Also, fault detection using multiple-valued test machines has been studied by Sheppard and Vranesic[40], while a multilevel balanced code with redundant digits was investigated by Asabe and Tezuka[4]. Treatment of error signals was reported by Breuer and Epstein[7]. Finally, multiple-valued logic symmetric functions and their properties were well-noted by S. C. and E. T. Lee[28] and also by Cheung and Su[8].

Threshold Logic Design, covered in Part III, is an extremely important area of computer engineering and logic design in its own right. Multiple-valued variable-threshold logic is being investigated by Aibara, Takamatsu, and Murakami, while applications of multiple-valued threshold logic to digital computer arithmetic were discovered by the Finnish computer engineers, Koukkunen and Ojala[26]. On the other hand, Druzeta and Sedra[9] have made good progress by using multiple-

threshold circuits in the design of multi-state storage elements. Finally, it must be mentioned that Moraga has achieved excellent results in the study of nonlinear[33], minimal[37], and periodic[34] ternary threshold logic systems. Another good summary paper is that of Vranesic and Hamacher on threshold logic in fast ternary multipliers[50]. Along the same lines is the work on multifunction threshold gates by Hampel[23].

It goes without saying from a commercial-industrial point of view that Parts IV and V, physical components and implementations and applications, are very important for computer engineering. Historically, despite relatively little effort being put into the design of electronic circuits for multiple-valued logic, there has been a very encouraging evolutionary trend towards many more practical realizations. In the past implementations had suffered from insufficient utilization of integrated circuit techniques. In the past, for example, stray capacitance in complex discrete circuits had led to slow operating characteristics. However, additional components and the miniaturization possible with integrated circuit technology is now leading to a much improved speed performance. Once the speed problems are overcome, the natural and very valuable advantages of multiple-valued logic techniques in the reduction of wiring complexity, a big cost factor in building present day computers, will assert themselves. The computer engineering group at the University of Toronto made elegant strides in constructing and implementing multiple-valued logic physical components; I mention the work of Vranesic and Smith[56, 57] and Sebastian and Vranesic[47]. One must also mention the independent work on multiple-valued integrated circuits by Abraham[1] at the Naval Research Laboratory. A new concept for ternary logic elements has been reported by Etiemble and Israel[16], while Mouftah and Jordan[35] have reported success on integrated circuits for ternary logic. Shiva and Nagle[49] at Auburn University advanced technology on multiple-valued memory elements, while Strasilla[57] in Switzerland made excellent headway on a multiple-valued logic memory system using capacitor storage. Also in the area of physical components Irving and Nagle[25] invented an approach to multiple-valued sequential logic. Historically, Braddock, Epstein, and Yamanaka[6] hold an original patent on a multiple-valued logic design and application in binary computers. The work of Metze[31] also deserves mention in this section.

Part V, applications and implementations, contains new material since the first edition of this book was published in 1977. Section A includes reports of recent work on multiple-valued logic devices, whereas Section B includes new chapters on circuit design and testing. Section C includes other applications related to programming and Walsh functions.

Microprogramming made it possible sensibly to study the emulation of multiple-valued logic computer systems; it is often better to build an emulator than an actual prototype of the system. It has been said that "emulation is the bridge between hardware and software". Frieder, Fong, Chao, and Luk[18, 19] used emulation to study a balanced ternary computer, particularly the arithmetic unit. On the other hand, Halpern and Yoeli[21] and Vranesic and Hamacher[22, 55] considered the actual hardware prototype of the arithmetic unit in their studies. Another good German reference is[5]. Of importance to testing in computer engineering, Rowe[46]

researched the generation by multiple-valued logic of pseudorandom noise, while Lam and Vranesic[27] reported the multiple-valued logic generation of pseudorandom numbers, potentially better than binary generation. Leibler and Roesser[29] described multiple-real-valued Walsh functions, while McDonald and Singh[30] extensively researched the extensions of the Weiner-Smith algorithm for multiple-valued logic synchronous sequential circuit design. Asabe and Tezuka[4] reported on the multilevel balanced code with redundant digits. In software applications, Rine[42, 43] mentioned applications of multiple-valued logic to programming languages and also to statistical decision theory[44]. Of interest to computer science, diagnostic pattern recognition and multiple-valued logic systems has been the variable-valued logic systems VL1 Project under the direction of R. S. Michalski[32]. Also of interest has been the work of Rasiowa[40] on a logical structure of mix-valued programs.

Aside from this book a good continuing reference on computer science and multiple-valued logic is the Proceedings of the Annual Symposium, Technical Committee on Multiple-valued Logic, IEEE Computer Society.

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a selected survey of multiple-valued logic design for digital computing systems: 1952–1983

This section covers in survey fashion an historical evolution of multiple-valued logic of digital computing systems. Logic elements are interconnected so as to perform particular logic or arithmetic operations Historically, logic functions have been classified as either combinational or sequential and parallel, and they have been formally designed at the gate level up. Logic functions have included decoders and encoders, parity and comparator functions, distributors and selectors, adders and subtractors, flip-flops and multivibrators, counters and shift registers, interrupt handling registers, universal function generators, and many others.

This section is broken down into six time periods, and each time period is correlated against major research areas relating to logic design in that era. For example, "[AM, 1952–1962]" denotes the list of references in the first era, A or 1952–1962, pertaining to logic function minimization and simplification, M. Also, in order to be as brief as possible, major bibliographies of other authors in eras have been included [AB0, AB1, AB2, BB0, CB0].

The author has tried to list in the references of each era many of the major research contributions in the leading computer science and engineering journals.

The Era of 1952 *to* 1962

The early part of this era saw the rise of the use of formal notation by logic function design engineers. The formal notations which were most successfully used were the Boolean algebra and the propositional calculus [AG, 1952–1962]. Two important reasons for the use of such formalism were the need for a logic function design language and the need for a precise notation for expressing minimization algorithms for both single and multiple output logic functions. Minimization algorithms highlighted this era Later, logic designers would witness a transition from an emphasis on Boolean algebra to the forthcoming of design languages as the importance of gate-level description was replaced by subsystems description [AB1; AB2, 1952–1962].

The end of this era witnessed a decrease in the number of articles dealing purely with logic functions. But the notation which had been developed gained wide acceptance, logic design was now constituted in Boolean algebra expressions and equations [AB0, 1952–1962].

The end of this era also witnessed a rising interest in sequential machines, as logic design became more theoretically classed with more research on sequential machines

Primary research interests in logic functions during this era were function minimization and simplification [AS, 1952–1962] and general logic function considerations [AG, 1952–1962].

The Era of 1963 *to* 1966

Primary research interests in logic functions during this second era showed a greatly increased interest in threshold logic functions [BT, 1963–1966], more on function minimization and simplification [BM, 1963–1966] and more interest in specific properties of logic functions [BD, BJ; BS; BL; BI; BC; 1963–1966].

The reasons for the increased interest in threshold logic gates and functions were discoveries of some important potential advantages over traditional Boolean realizations. First, by using a gate with more than the required number of inputs its threshold can be modified by connecting extra inputs to a 1 or a 0. Secondly, one can usually implement nearly any logic function with fewer gates than with Boolean and often with just a single gate. Threshold gates were viewed as more powerful general purpose building blocks of the future, replacing the popular NAND/NOR gates, for example. Later, one would see more interesting considerations such as the analog sum implementation of IC's (integrated circuit) and the possible fabrication of threshold gates from existing IIL and MOS (Metal oxide semiconductor) processes

There were, also, disadvantages as well as advantages encountered in threshold gate realizations. First, there was the difficult straightforward Boolean implementation of them; and, secondly, there was the high cost of analog sum implementation for IC's. Next, tolerancing problems were encountered when working with more than a small number of inputs. It would seem today that a possible new technology is necessary for efficient implementation of threshold gates.

The Era of 1967 *to* 1970

In this era traditional logic functions remained of interest but some new areas grew also. Primary research interests in logic functions witnessed a continued rise in interest of threshold logic functions [CT; CB0, 1967–1970], continued interest in function minimization and simplification [CM, 1967–1970], a rise in interest of multiple-valued logic [CL, 1967–1970] and broader investigations of registers, circuit minimization and design automation [CR, CN; CG; 1967–1970]

Reasons for increasing interest in multiple-valued logic were the emphases of some potential advantages over Boolean logic. First of all, there is the potential for storage of larger volumes of data than for two-valued Boolean logic memories and registers. Secondly, there is potential for increased information content per signal line. Then, it could be shown that fewer interconnections per logic function realization could be achieved when using multiple-valued logic design instead of two-valued logic. Also, larger logic functions could potentially be implemented for a fixed number of interconnections In a serial mode of operation one could design for more information per line, and in a parallel mode of operation one could design for fewer lines

. There were also disadvantages encountered in multiple-valued logic designs.

First, it was discovered that multiple-valued logic designs led to increased circuit complexity per gate over binary. Also, more surface area per gate and per chip was needed Today it is clear that necessary improvements are needed in speed, power consumption, packaging and pricing to make multiple-valued logic better than binary or Boolean logic, also, integrated circuits will need to be made available to reduce physical size and cost Such improvements are likely in the future. Last of all, it will be necessary to design and implement devices which can translate to and from existing binary devices, the forthcoming of such devices is, also, likely in the future.

Also, in this era of the late 1960's there was a great increase in interest in the promise of automata theory and sequential machines as design tools. There was increased interest on memories and processors from a technology point of view; and, there was increased interest in new logic function areas of cellular logic, array logic, parallel logic and associative logic.

Although, in this era, there was a decreased emphasis on study of logic functions per se, as interest in register level design increased, there was an increased interest in improving implementations of existing logic function designs for faster performance and higher density.

The Era of 1971 *to* 1973

In this era primary research interests in logic functions and their design continued to be multiple-valued logic [DL, 1971–1973], threshold logic [DT, 1971–1973] and function minimization and simplification [DM, 1971–1973].

The Era of 1974 *to* 1976

This era saw the register transfer and subsystems level, along with design languages, replacing much of the importance of logic function levels of earlier eras [EG, 1974–1976]. Moreover, techniques for minimizing arithmetic networks and entire systems at the macro level and minimizing circuits and power considerations at the micro level have replaced some of the importance of logic function minimization [EG5; EN0; EN1, 1974–1976]. In this era there is still some current theoretical interest in sequential machines, but it is not as strong as in earlier eras. However, in practice state diagrams have received wide use.

Primary research interests in logic functions during this contemporary era are function minimization and simplification [EM, 1974–1976], threshold logic functions [ET, 1974–1976], multiple-valued logic [EL, 1974–1976] and logic equations [EE, 1974–1976].

This era saw much research go into high speed logic functions for processing.

A maximum feasible number of gates per integrated circuit chip increased over the fifteen years since 1963 such that there was a three orders of magnitude increase in the maximum feasible number of components in one silicon integrated circuit chip. In fact over one hundred thousand gates per chip were predicted by the 1980's, particularly for those having moderate speed circuits where power dissipation is not such a problem.

The large scale integrated circuit package pin count, or off-chip connection density,

increased over these fifteen years at a slower rate than for gates per chip; and, the package pin count increased well under one order of magnitude in that time frame. For the logic function designer this meant a continuing increase in importance of interconnection simplification and a continuing decrease in importance of gate count simplification. Logics following this trend would be more important.

Limitations on pin count would prevent more parallelism on data and control paths, and more information per line would be needed to reduce interconnection count further. Thus, better serial operation on data and control paths may be advanced by the following techniques: (1) Greatly encoded control information (2) Multiple-valued logics. (3) Superior multiplexing of data.

All in all, it was predicted that integrated circuit chip count would continue to be a good measure for digital logic cost and reliability.

There was, however, a drawback in potential introduction of new designs. Logic function design costs for totally new complicated circuits could approach five hundred thousand dollars each and be a limiting factor unless high volumes were sold. Also, design automation could not actually lower logic design costs, except for new logic functions having simpler and more regular structures.

The Era of 1977 *to* 1983

This era saw a continued improvement of LSI multiple-valued logic circuit design. Technologies included bipolar current-mode circuits comprising I^2L and ECL quaternary logic, unipolar voltage-mode circuits comprising NMOS and MESFET ternary logic, charge-coupled quaternary logic, and ROM constructions using I^2L and MOS. This era saw the rise of VLSI in semiconductor technology and the need for major reduction in interconnections between active devices inside and outside of an integrated circuit. In order to reduce such interconnections the information content of each connection has to be increased (1) by time multiplexing or (2) by level multiplexing (current, voltage, impedence). The first approach (1) is mainly limited to interchip pin connections, but the second approach (2) can be applied to intrachip circuitry. Approach (2) has stimulated the development of multiple-valued logic circuits which are, indeed, made possible by new technologies, better lithography, and improved CAD tools and process controls.

The improved circuit design techniques will also be led by advances in testing and verification software procedures. Continued improvements in developing automated techniques for MVL circuit design may be led by the use of new tools, such as "theorem-proving" systems which can be applied to logic synthesis and verification.

This era also saw a continued rise in the application of MVL devices and circuits to testing, fault diagnosis, signal transmission, denser storage, arithmetic units, and network control.

The Era of 1984 *to*...

Many companies in the USA have now manufactured LSI/VLSI MVL chips, including Fairchild, Intel and National. Japan continues to integrate MVL technology into fifth generation machines. Competition is high, and it is not yet clear what the future will hold.

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