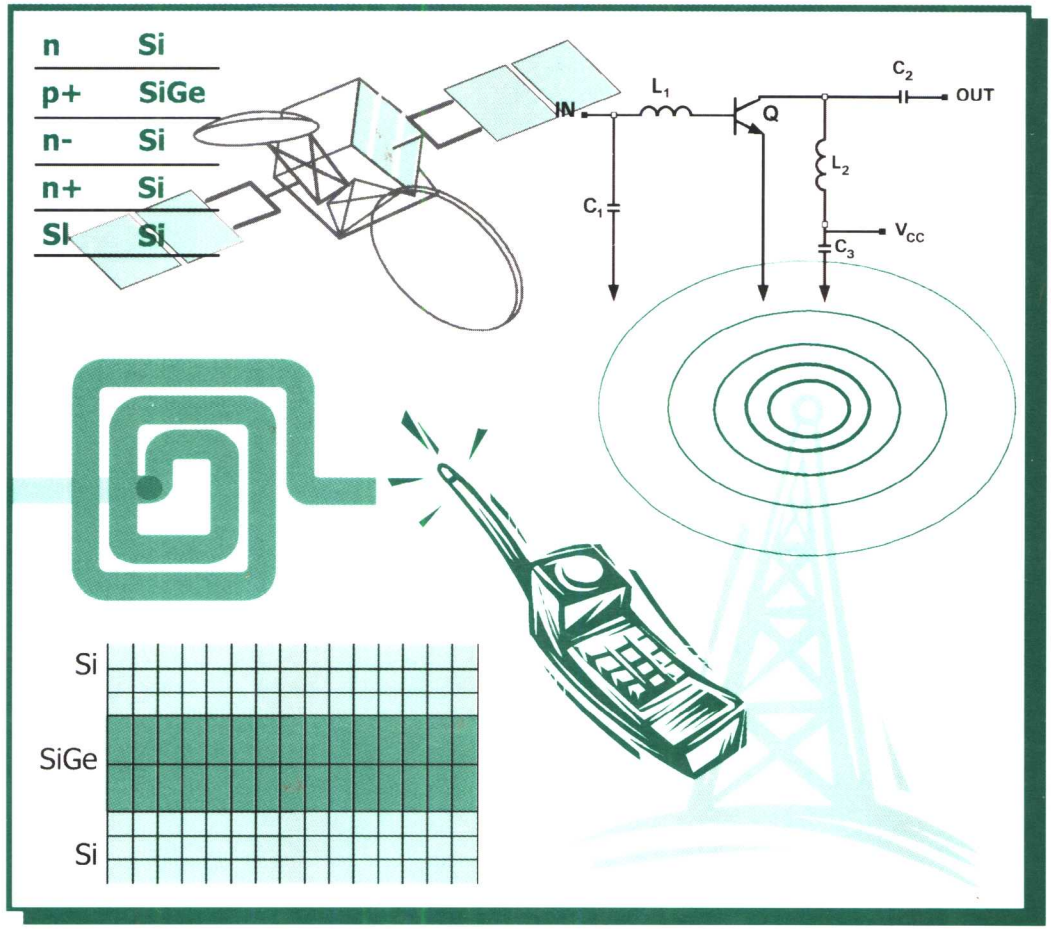
2001

Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems



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2001 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems

DIGEST OF PAPERS

George E. Ponchak, Editor

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Message from the Conference Chairs

We welcome you to the third **IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems**, which is once again being held on the campus of the University of Michigan in Ann Arbor, Michigan. In planning this meeting, we have tried to retain the successful format of the first meeting in Ann Arbor and the last meeting that was held in Garmisch, Germany while adding new features that we hope add to its success. We have retained the single session format so that everyone can participate in the presentation of every paper, and we have scheduled ample breaks and a reception so that we may catch up on news and discuss ideas in a friendly atmosphere. Of course, whatever changes and plans the organizing committee makes, the success of the meeting will be due to the technical contributions of the authors, and this year, the technical program is very strong. Thirty eight contributed papers will be presented that cover the topic areas of low noise circuits, RF MEMS on silicon, passive components, advanced devices, high frequency circuits, and reliability and yield. In addition, five invited papers that highlight the potential that silicon has to revolutionize high speed/high frequency integrated circuits will be presented. These forty three papers represent the contributions from fourteen countries making this a truly international meeting.

We look forward to seeing you at the meeting, and we hope you enjoy all of the activities that The University of Michigan and Ann Arbor, Michigan have to offer.

George E. Ponchak and Linda P. B. Katehi

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Session Chair: Joachim N. Burghartz (Delft University of Technology)

A CMOS Low Noise Amplifier at 2.4 GHz with Active Inductor Load

A. Pascht, *Member, IEEE*, J. Fischer and M. Berroth, *Member, IEEE*

Abstract--A two stage cascode CMOS low noise amplifier (LNA) with an active inductor load is presented. On-chip active inductors require 90% less silicon area at a higher quality-factor. Comparison of measurement and simulation of an active inductor shows the high quality factor. Simulations of the low noise amplifier show the advantages of active inductors with similar performance even in regard to the noise figure. The simulated gain and noise figure are 19 dB and 2 dB respectively.

***Index terms*—low noise amplifier, active inductor, CMOS**

I. Introduction

With decreasing channel length and thereby increasing transit frequency CMOS technology becomes more attractive for RF components in mobile communication products. One of the key circuits in the RF front end is the low noise amplifier (LNA), which requires inductors for the impedance and noise matching. On-chip passive inductors exhibit poor quality-factor and require large silicon die area. This paper compares two LNA designs, one with spiral inductors only and the other one applying an active inductor load which resulted in a reduction of 25% of the required chip area without deteriorating significantly the performance.

II. Active Inductor Design

The regulated cascode circuit of figure 1 is a gyrator-based technique to realize active inductors on-chip [1]. The regulated cascode active inductor allows in contrast to a simple gyrator the increase of the available bandwidth and the quality-factor. The cascode stage with the transistor T_3 is increasing the output resistance and therefore the lower cut-off-frequency is decreasing. To control the quality-factor the transistor T_4 is used in a regulated cascode structure. The disadvantage of active inductors is their poor noise performance compared with the passive counterparts because of the channel noise of the transistors [2] and their limited dynamic range.

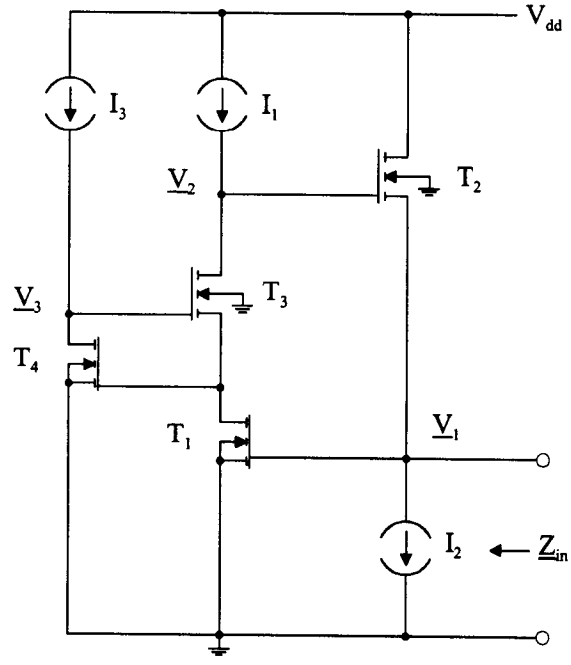

Fig. 1: Regulated cascode active inductor.

For the realization of the active inductor a standard 0.3 µm CMOS process is used. Figure 2 shows a comparison between measurement and simulation of the input reflection factor $\underline{S}_{11}$ of the active inductor. In the frequency range f=500 MHz – 2.5 GHz inductors with L=10nH – 90nH and a quality factor up to Q=60 have been realized. The tunable active inductor is useful for various applications, e.g. tunable amplifiers, tunable filters and oscillators.

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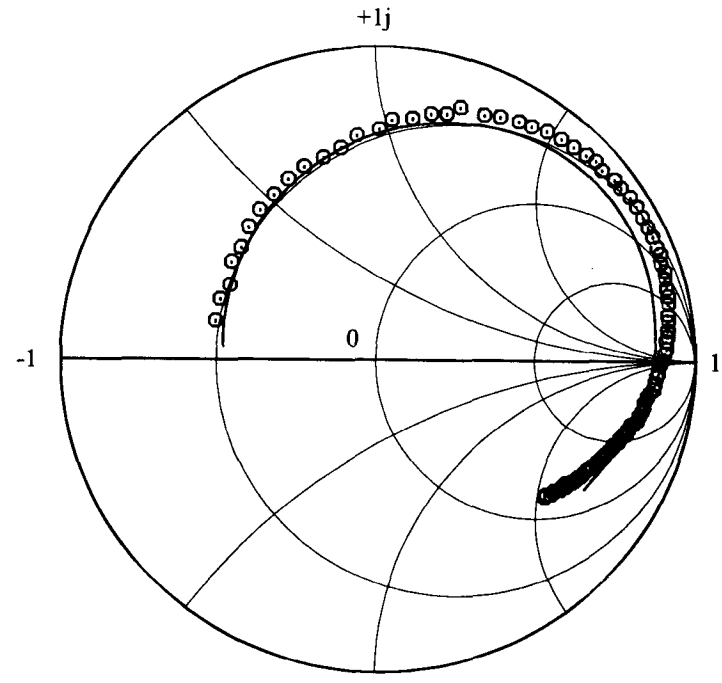

Fig. 2: Input reflection factor $\underline{S}_{11}$
(measurement: dots, simulation: line).

III. LNA DESIGN WITH ACTIVE INDUCTOR

For the design of the LNA a two stage circuit is used as shown in figure 3.

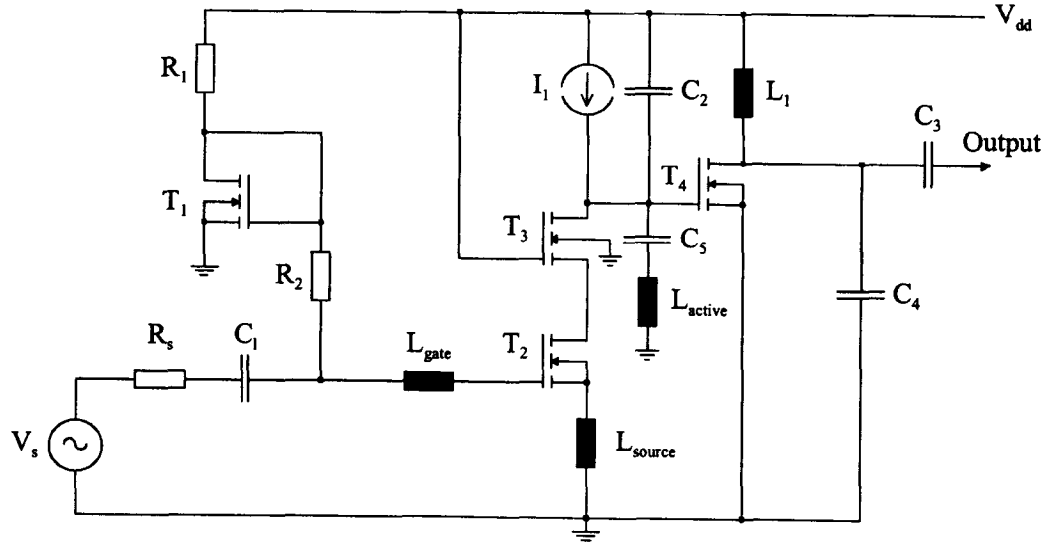

Fig. 3: Two stage low noise amplifier with active inductor.

The first stage is a cascode stage. Figure 4 shows the noise and impedance matching of the input achieved with the two input inductors L_{gate} and L_{source}.

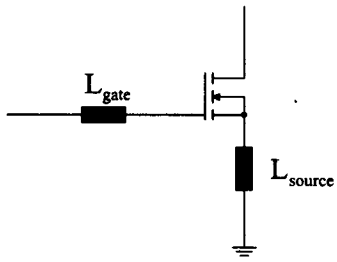

Fig. 4: Noise and impedance matching with the input inductors L_{gate} and L_{source}.

The input impedance is given by equation (1).

$$\underline{Z}_{in} = j\omega\left(L_{gate} + L_{source}\right) + \frac{1}{j\omega C_{gs}} + \left(\frac{g_m}{C_{gs}}\right) L_{source} \qquad (1)$$

With the source inductor L_{source} the input impedance at resonance can be adjusted. The gate inductor L_{gate} is used to control the resonance frequency. In the final design L_{source} was omitted cause matching was achieved with L_{gate} only. A tuned circuit is the load of the cascode stage and determines the center frequency of the amplifier. T_1 is used as a current mirror for the biasing of the input stage. The output stage is the source-stage T_4 while L_1, C_3 and C_4 are used for output matching. The published results of low noise amplifiers using active inductors come along with poor noise performance [2, 3]. To avoid a performance degradation the spiral inductor is used at the noise sensitive input and the inductor at the drain of the cascode stage as shown in figure 3 is replaced. In the same manner the drain inductor of the output circuit can be replaced.

IV. Simulation Results

Figure 5 shows the simulation of the forward transmission factor $|\underline{S}_{21}|$ of the LNA with and without active inductor. At the center frequency f=2.4 GHz the gain of LNA with only spiral inductors is $|\underline{S}_{21}|$=18.3 dB and $|\underline{S}_{21}|$=19.2 dB for the LNA with active inductor. The deviation of the transfer function can be minimized via the adjustable quality-factor of the active inductor.

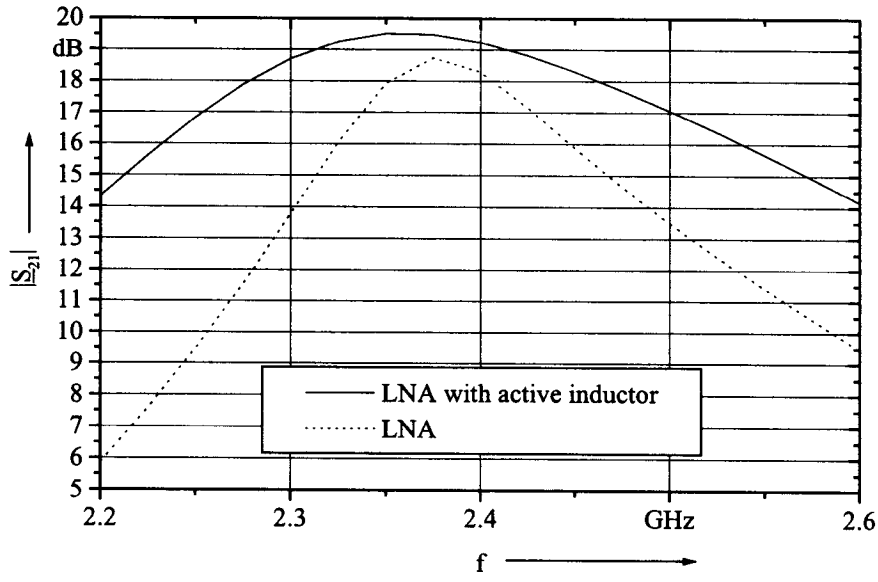

Fig. 5: Comparison of the gain.

The simulation of the noise figure is shown in figure 6 with F_{50}=1.6 dB for the standard LNA and F_{50}=2 dB for the LNA with active inductor at a center frequency of f=2.4 GHz respectively. The slightly increase of the noise figure for the design with active inductor is compensated by a 25% reduction of the chip area.

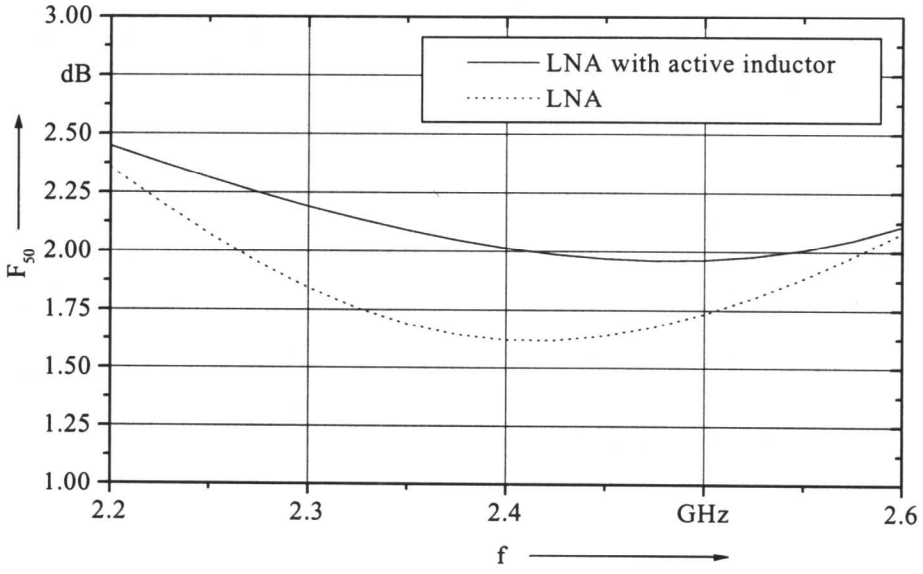

Fig. 6: Comparison of the noise figure.

The power dissipation is increasing from P=18.3 mW for the design with only spiral inductors up to P=40.8 mW for the design with active inductor.

V. Layout

The LNA and the active inductor will be fabricated in a standard 0.3 μm CMOS process with a transit frequency of f_t=40 GHz. Three metal layers on high resistive substrate are available for interconnection. Figure 7 shows the layout of the low noise amplifier without active inductor.

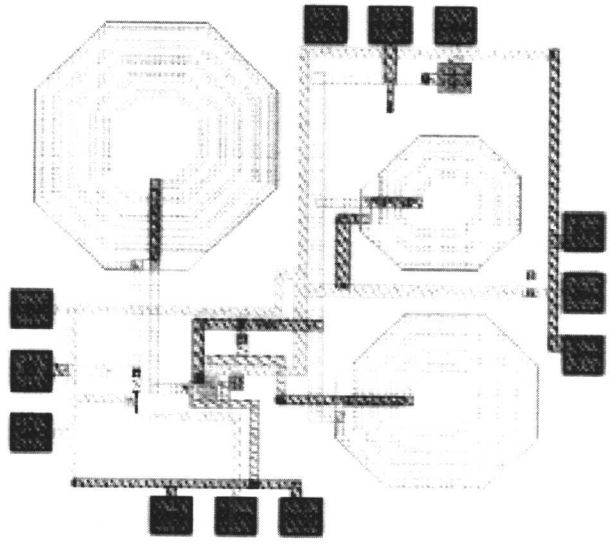

Fig. 7: Layout of the low noise amplifier without active inductor.

Figure 8 shows the layout of the low noise amplifier with one active inductor. The entire LNA without active inductor requires a silicon area of A=0.83 mm^2 and A=0.6 mm^2 with active inductor. The required silicon area of the LNA is reduced by more than 25% using the active inductor. If the second inductor at the output is also replaced by an active inductor, the chip area can be reduced by about 50%.

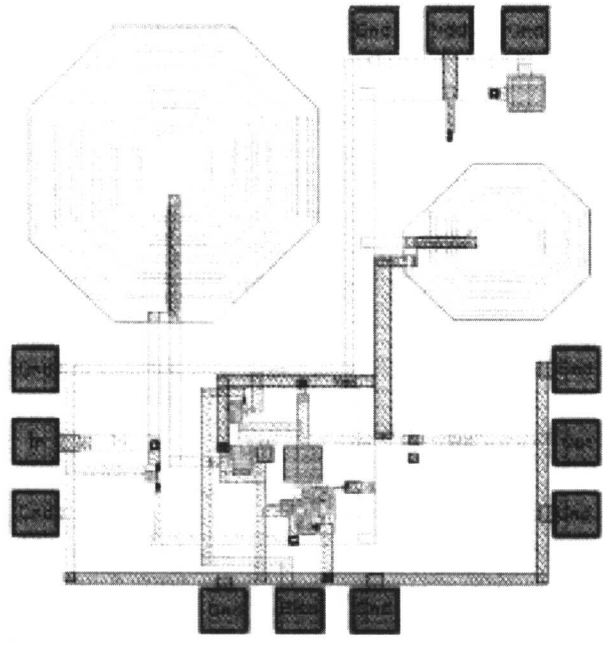

Fig. 8: Layout of the low noise amplifier with one active inductor.

VI. Conclusion

A regulated cascode active inductor is used for the design of low noise amplifiers (LNA's). For a center frequency of f=2.4 GHz the simulated noise figures are of F_{50}=1.6 dB for the standard LNA and F_{50}=2 dB for the LNA with one active inductor respectively. Moreover the gain and the power dissipation of the standard LNA is $|\underline{S}_{21}|$=18.3 dB and P=18.3 mW [4]. For the LNA using one active inductor the gain and the power dissipation are $|\underline{S}_{21}|$=19.2 dB and P=40.8 mW. For a small increase of the noise figure and an increase in power dissipation a reduction of the chip area by about 25% is achieved. Moreover the quality-factor of the active inductor is adjustable in a wide range up to Q = 60.

VII. References

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Advanced Design of high linearity, low noise amplifier for WLAN using a SiGe BiCMOS Technology.

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Abstract

In this paper, we present the design of an integrated low noise amplifier (LNA) for WLAN applications in the 6 GHz range using a SiGe BiCMOS technology. The SiGe HBTs feature a cut-off frequency "Ft" higher than 40 GHz and maximum oscillation frequency "Fmax" higher than 50 GHz.

The design of some of the passive devices of the circuit has been achieved from 2D electromagnetic simulations. We have observed a quiet good agreement between measurements and simulation even in the non linear regime. The LNA exhibits a power gain larger than 15 dB from 5 GHz to 6 GHz and 2 GHz bandwidth, a noise figure lower than 2 dB. It exhibits a 1 dB input referred compression point of more than -18 dBm and a 0 dBm input referred third order intercept point.

Index terms
LNA, SiGe HBT, high Q inductor, Non linear behavior.

INTRODUCTION

The multiplication of wireless telecommunication systems and the increase of the number of customers translate into very strict requirements concerning the performance of the microwave modules. They have to feature low noise figure and high linearity due to the overcrowding spectrum. They have also to exhibit high reliability performance and low power consumption in order to meet with the customer requirements and finally they have to be cheaper and cheaper. Among the electronic modules which are playing a key role in the front end performance. We must consider: the low noise amplifier and mixer which will be influenced by the noise behavior in the high frequency range which is related to the thermal noise associated to the resistive parts of the circuit (i.e. base, emitter and collector). The VCO circuit which will participate to the frequency translation and which has to feature a very high spectral purity. The latter is influenced by the low frequency noise sources mostly originating from the active devices that are up-converted into phase fluctuations through complex nonlinear phenomena. Finally, the power amplifier must exhibit a good linearity with the best efficiency as possible.

These last years have seen the emergence of a new contender for the microwave applications: the SiGe HBT. This type of component authorizes frequencies operating beyond 50 GHz, which makes possible to use it up to 20 GHz and more. It furthers exhibits excellent properties in term of noise (both in the high frequency range for low noise amplifier and in the low frequency range for low phase noise oscillator). Moreover, SiGe BiCMOS technology is a silicon based technology that takes advantage of the maturity of silicon processing techniques and results into very low cost components. If the situation concerning the active device seems to be clear, the problem of the passive elements on silicon is still pending despite the tremendous efforts that have been developed for many years to overcome the drawbacks inherent to silicon substrate. Another problem is still present related to the design accuracy of the SiGe integrated circuits at high frequency (>2 GHz). Actually, the literature reports numerous SiGe based circuits exhibiting very attractive performance but there is often a lack of comparison between measured and simulated data. In this paper, we aim at validating the design of a microwave SiGe circuit from such a comparison.

With this end in view, we address the design of a 5 GHz to 6 GHz low noise amplifier for WLAN applications such as HIPERLAN. The work is based on the SiGe BiCMOS process of ST Microelectronics. The available SiGe HBTs exhibit a graded Ge profile within the base in order to reduce the base transit time. The emitter width is 0.4 µm. The breakdown voltage can be adjusted through a selectively implanted collector between 5.5 V and 3.3 V. We will use the low voltage version exhibiting the higher Fmax value in order to get a low value of the noise figure. Such a device exhibits a current gain of about 50 and Ft and Fmax values of 40 GHz and 60 GHz respectively. The electrical behavior of the device is described through a modified "Gummel Poon" non linear model which has been validated up to 20 GHz. Concerning the passive elements, the technology features five

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