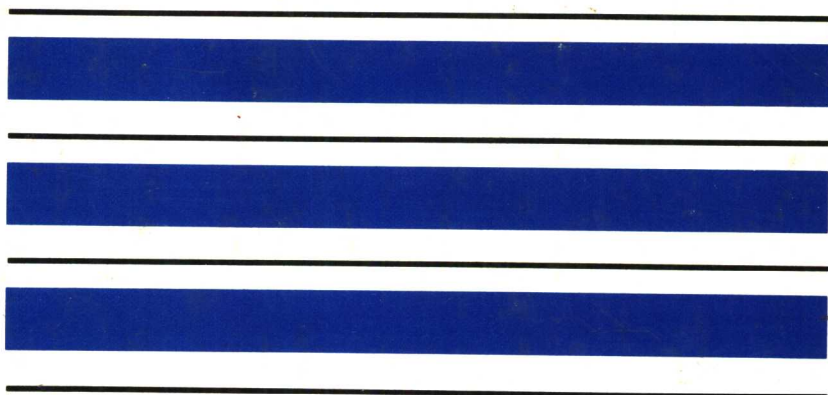

Introduction to VLSI Silicon Devices

**Physics, Technology
and Characterization**

**Badih El-Kareh
Richard J. Bombard**



Kluwer Academic Publishers

INTRODUCTION TO VLSI SILICON DEVICES

Physics, Technology and Characterization

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and
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TABLE OF SYMBOLS

| Symbol | Description | Units |
|------------|--|-----------|
| a | Grade constant, pn junction | cm^{-4} |
| a | Voltage ramp rate, quasistatic measurement | V/s |
| A | Area | cm^2 |
| A_s | Silicon surface area | cm^2 |
| BV | Breakdown voltage | V |
| BV_{CBO} | Collector-base breakdown voltage, emitter open | V |
| BV_{CEO} | Collector-emitter breakdown voltage, base open | V |
| C | Capacitance | F |
| C_A | Capacitance area component | F |
| C_D | Diffusion capacitance | F |
| C_C | Collector capacitance | F |
| C_E | Emitter capacitance | F |
| C_{FB} | Flatband capacitance | F |
| C_{it} | Interface trap capacitance | F |
| C_{HF} | High frequency capacitance | F |
| C_{LF} | Low frequency capacitance | F |
| C_{max} | Maximum MIS capacitance | F |
| C_{min} | Minimum MIS capacitance, thermal equilibrium | F |
| C_{ox} | Equivalent oxide capacitance | F |
| C_P | Capacitance perimeter component | F |
| C_{si} | Silicon capacitance | F |
| C_{siFB} | Silicon capacitance at flatband | F |
| D_n | Diffusion constant of electrons | cm^2/s |
| D_p | Diffusion constant of holes | cm^2/s |
| E | Electric field | V/cm |
| E_c | Critical field | V/cm |
| E_p | Peak electric field | V/cm |
| E_g | Energy gap | eV |
| h_{FE} | Large signal transistor gain | --- |
| f_T | Frequency at which $\beta = 1$ | Hz |
| I | Current | A |
| i_A | Leakage current per unit area | A/cm^2 |
| I_C | Collector current | A |
| I_{CBO} | Collector-base leakage current, emitter open | A |

TABLE OF SYMBOLS
(Continued)

| Symbol | Description | Units |
|-----------|--|----------------|
| I_D | Drain current | A |
| I_E | Emitter current | A |
| I_F | Forward current | A |
| I_{FLJ} | Leakage current in field-induced junction | A |
| I_G | Gate current | A |
| I_{gen} | Generation current | A |
| I_L | Leakage current | A |
| I_m | Current due to mobile ions | A |
| I_{MJ} | Leakage current in metallurgical junction | A |
| I_n | Electron current | A |
| I_o | Saturation current | A |
| i_p | Leakage current per unit perimeter | A/cm |
| I_p | Hole current | A |
| I_{PT} | Punch-through current | A |
| I_R | Reverse current | A |
| I_s | Transistor saturation current | A |
| I_s | Substrate current | A |
| I_w | Well current | A |
| j | Current density | A/cm^2 |
| j_G | Gate current density | A/cm^2 |
| j_n | Electron current density | A/cm^2 |
| j_{ni} | Electron current density in intrinsic base | A/cm^2 |
| j_{nc} | Electron current density into base contact | A/cm^2 |
| j_p | Hole current density | A/cm^2 |
| j_{pc} | Hole current density into emitter contact | A/cm^2 |
| j_{pl} | Lateral hole current density | A/cm |
| j_{pv} | Hole current density into substrate | A/cm^2 |
| j_{pv} | Hole current density into buried n^+ layer | A/cm^2 |
| k | Boltzmann constant | $eV/^{\circ}K$ |
| k | Scaling factor | --- |
| L | Channel length | cm |
| L_{eff} | Effective channel length | cm |
| L_D | Extrinsic Debye length | cm |

TABLE OF SYMBOLS

(Continued)

| Symbol | Description | Units |
|----------------|--|------------------|
| L_i | Intrinsic Debye length | cm |
| L_n | Diffusion length of electrons | cm |
| L_p | Diffusion length of holes | cm |
| m | Mass of electron | g |
| M | Multiplication factor | --- |
| n | Electron density | cm ⁻³ |
| n | Ideality factor | --- |
| n_i | Intrinsic carrier concentration | cm ⁻³ |
| n_n | Electron concentration in n-type silicon | cm ⁻³ |
| \bar{n}_n | Equilibrium majority electron concentration | cm ⁻³ |
| n_{no} | Boundary majority electron concentration | cm ⁻³ |
| \bar{n}_{no} | Boundary equilibrium majority electron conc. | cm ⁻³ |
| n_p | Minority Electron concentration | cm ⁻³ |
| \bar{n}_p | Equilibrium minority electron concentration | cm ⁻³ |
| n_{po} | Boundary minority electron concentration | cm ⁻³ |
| \bar{n}_{po} | Boundary equilibrium minority electron conc. | cm ⁻³ |
| n_s | Surface electron concentration | cm ⁻³ |
| N_a | Acceptor concentration | cm ⁻³ |
| N_a^- | Ionized acceptor concentration | cm ⁻³ |
| N_d | Donor concentration | cm ⁻³ |
| N_d^+ | Ionized donor concentration | cm ⁻³ |
| N_{si} | Density of atoms in silicon | cm ⁻³ |
| N_t | Density of traps in silicon | cm ⁻³ |
| N_{ox} | Density of atoms in silicon-dioxide | cm ⁻³ |
| p | Hole concentration | cm ⁻³ |
| P | Power | W |
| P | Perimeter | cm |
| p_n | Minority Hole concentration | cm ⁻³ |
| \bar{p}_n | Equilibrium minority hole concentraton | cm ⁻³ |
| p_{no} | Boundary minority hole concentration | cm ⁻³ |
| \bar{p}_{no} | Boundary equilibrium minority hole concentration | cm ⁻³ |
| p_p | Majority hole concentration | cm ⁻³ |
| \bar{p}_p | Equilibrium majority hole concentration | cm ⁻³ |
| p_{po} | Boundary majority hole concentration | cm ⁻³ |

TABLE OF SYMBOLS

(Continued)

| Symbol | Description | Units |
|----------------|---|-------------|
| \bar{p}_{po} | Boundary equilibrium majority hole conc. | cm^{-3} |
| p_s | Surface hole concentration | cm^{-3} |
| q | Elementary charge | C |
| Q | Charge per unit area | C/cm^2 |
| Q_b | Bulk charge density of ionized impurities | C/cm^2 |
| Q_{eff} | Effective insulator charge density | C/cm^2 |
| Q_f | Fixed oxide charge density | C/cm^2 |
| Q_G | Charge density induced on the gate | C/cm^2 |
| Q_{it} | Interface trap charge density | C/cm^2 |
| Q_m | Mobile ion charge density | C/cm^2 |
| Q_n | Free electron charge density | C/cm^2 |
| Q_{ot} | Oxide trap charge density | C/cm^2 |
| R | Resistance | Ohm |
| R_c | Contact resistance | Ohm |
| R_C | Collector resistance | Ohm |
| R_{ch} | Channel resistance | Ohm |
| r_E | Emitter dynamic resistance | Ohm |
| r_j | Junction curvature | cm |
| R_E | Emitter resistance | Ohm |
| R_p | Projected range of ions | cm |
| R_s | Sheet resistance | Ohm/square |
| R_s | Substrate resistance | Ohm |
| R_w | Well resistance | Ohm |
| s_o | Surface recombination velocity | cm/s |
| t | Time | s |
| t | Thickness | cm |
| t | Temperature | $^{\circ}C$ |
| T | Temperature | $^{\circ}K$ |
| t_f | Fall-time | s |
| t_d | Delay time | s |
| t_{eq} | Equivalent oxide thickness | cm |
| t_i | Insulator thickness | cm |
| t_n | Thickness of silicon-nitride | cm |
| t_r | Rise-time | s |

TABLE OF SYMBOLS (Continued)

| Symbol | Description | Units |
|------------|---------------------------------------|-------------|
| t_s | Storage time | <i>s</i> |
| t_{si} | Thickness of silicon | <i>cm</i> |
| t_{ox} | Oxide thickness | <i>cm</i> |
| v | Velocity | <i>cm/s</i> |
| v_d | Drift velocity | <i>cm/s</i> |
| v_s | Scattering limited velocity | <i>cm/s</i> |
| v_{th} | Thermal velocity | <i>cm/s</i> |
| V | Voltage | <i>V</i> |
| V_b | Built-in voltage | <i>V</i> |
| V_{BE} | Base-emitter voltage | <i>V</i> |
| V_{CB} | Collector-base voltage | <i>V</i> |
| V_D | Drain voltage | <i>V</i> |
| V_G | Gate voltage | <i>V</i> |
| V_H | Most positive voltage | <i>V</i> |
| V_{ox} | Voltage across oxide | <i>V</i> |
| V_{PT} | Punch-through voltage | <i>V</i> |
| V_s | Source to substrate bias | <i>V</i> |
| V_t | Thermal voltage | <i>V</i> |
| V_T | Threshold voltage | <i>V</i> |
| x | Depth | <i>cm</i> |
| x_d | Depletion width | <i>cm</i> |
| x_{dmax} | Maximum field-induced depletion width | <i>cm</i> |
| x_{dn} | Depletion width in n-side | <i>cm</i> |
| x_{dp} | Depletion width in p-side | <i>cm</i> |
| x_{ds} | Depletion width at surface | <i>cm</i> |
| x_j | Junction depth | <i>cm</i> |
| W | Channel width | <i>cm</i> |
| W_b | Base width | <i>cm</i> |
| W_{eff} | Effective channel width | <i>cm</i> |
| W_n | Width of n-type material | <i>cm</i> |
| W_p | Width of p-type material | <i>cm</i> |
| α | Current gain, I_C/I_B | --- |
| α_n | Current gain of npn transistor | --- |
| α_p | Current gain of pnp transistor | --- |

TABLE OF SYMBOLS

(Continued)

| Symbol | Description | Units |
|-----------------|---|-----------------------|
| β | Current gain, I_C/I_B | --- |
| β | IGFET beta, $= \gamma W/L$ | $\Omega^{-1} V^{-1}$ |
| γ | Injection ratio | --- |
| γ | Normalized transconductance | $\Omega^{-1} V^{-1}$ |
| Δ | Small variation | --- |
| ΔR_p | Range straggling | cm |
| ϵ_i | Insulator dielectric constant | --- |
| ϵ_n | Dielectric constant of nitride | --- |
| ϵ_o | Permittivity of free space | F/cm |
| ϵ_{ox} | Dielectric constant of oxide | --- |
| ϵ_{si} | Dielectric constant of silicon | --- |
| μ | Mobility | cm^2/Vs |
| μ_n | Electron mobility | cm^2/Vs |
| $\bar{\mu}_n$ | Effective electron mobility | cm^2/Vs |
| μ_p | Hole mobility | cm^2/Vs |
| ρ | Resistivity | $\Omega - cm$ |
| ρ | Charge density | C/cm^3 |
| σ | Conductivity | $\Omega^{-1} cm^{-1}$ |
| τ | Time constant | s |
| τ_B | Base transit time | s |
| τ_C | Collector time constant | s |
| τ_{FLJ} | Minority lifetime, field-induced junction | s |
| τ_{MJ} | Minority lifetime, metallurgical junction | s |
| τ_n | Electron lifetime | s |
| τ_p | Hole lifetime | s |
| ϕ | Barrier | V |
| ϕ_b | Schottky Barrier height | V |
| ϕ_m | Metal work function | V |
| ϕ_{ms} | Work function difference | V |
| ϕ_{si} | Silicon work function | V |
| χ | Electron affinity | eV |
| ψ_s | Surface potential | V |
| ω | Angular frequency | s^{-1} |

Preface

There was a long felt need for this book in industrial and academic institutions. It provides new engineers, as well as practicing engineers and advanced laboratory personnel in the field of semiconductors a clear and thorough discussion of state-of-the-art silicon devices, without resorting to the complexity of higher mathematics and physics. This difficult task was made possible by detailing the explanation of equations that describe the device operation and characteristics without endeavoring their full derivation. This is reinforced by several problems which reflect practical cases observed in the laboratory. The problems are given after introducing a major equation or concept. They are arranged in the order of the text rather than in the order of difficulty. The answers to most of the problems are given in order to enable the student to "self-check" the method used for the solutions. The illustrations may prove to be of great help to "newcomers" when dealing with the characterization of real devices and relating the measured data to device physics and process parameters. The new engineer will find the book equivalent to "on the job training" and acquire a working knowledge of the fundamental principles underlying silicon devices. For the engineer with theoretical background, it offers a means for direct application of solid state theory to device analysis and synthesis.

The book originated from a set of notes developed for an in-house one-year course in Device Physics, Technology and Characterization at IBM. It is specifically written for the college graduate new in the field of semiconductors. It is also potentially useful to the practicing engineer and scientist who seek to "update" their knowledge on VLSI devices and methods for parameter extractions. It can be used for an introductory course in semiconductors in universities, colleges and technical institutes and may be introduced early in the curriculum because the only prerequisite in mathematics is algebra and elementary calculus. The book consists of six chapters, organized in a logical sequence and covering the range from basic silicon properties to advanced FET and bipolar concepts, including short-channel and narrow-channel effects, and device limitations. There is frequent cross-reference between the chapters. However, occasional

overlapping in material was necessary in order to discuss major sections independently. The units used throughout are not consistent mks units. There is frequent use of the angstrom, micrometer and centimeter as the unit of length and electron-volt as the unit of energy. Furthermore, units have been associated with several equations. It is believed that this approach will help better visualizing the quantities in semiconductors. A table of conversion factors is provided on the inside covers of the book. It was attempted to gradually raise the level from chapter 1 to the more difficult sections in chapter 3 after which the level of difficulty remains fairly constant. In each chapter a qualitative description of the device is first given and then followed by a gradual progression into a deeper understanding of the formulas that describe the relations between device and process parameters.

The book begins with the properties of the silicon crystal. The two-carrier concept is introduced on the basis of localized covalent bond-breaking rather than the band-diagram. The effects of temperature and impurities on the carrier concentrations and transport are discussed in detail. Finally, techniques are described to measure bulk and contact resistances and to relate the data to the impurity profile and temperature.

The second chapter details the description of real pn junctions. The formation of the junction is described, using first a thought experiment and then a simple process sequence. The concepts of built-in voltage, depletion regions and junction capacitance are introduced. Methods are described to characterize the junction at thermal equilibrium and under forward and reverse bias.

The third chapter begins with a qualitative discussion of bipolar action and methods to fabricate typical bipolar devices in the planar technology. The process and design parameters that determine the current-voltage characteristics of the device are then discussed quantitatively. This includes devices operated in forward and reverse, vertical and lateral transistors, low-level and high-level injection, second-order effects and voltage and current limitations. In addition, there is useful information on the characteristics of Schottky-barrier diodes, and their applications.

The analysis of the Metal-Insulator-Silicon (MIS) structure in chapter 4 lays the groundwork for a thorough understanding of Insulated Gate Field Effect transistors (IGFET). The structure is introduced not only as a device that is later extended to an IGFET

but also as a powerful tool for process control and diagnostics. The concepts of accumulation, flatband, weak and strong inversion, and threshold voltage are introduced, and the effects of work function difference and oxide charge on the flatband voltage are discussed in detail. Finally, the pulsed CV and quasistatic techniques are described and used to further characterize the silicon surface, sub-surface and insulator quality.

In chapter 5 a junction is placed under the MIS structure to form a gate-controlled pn junction. This provides a tool to measure surface effects on the junction reverse and forward characteristics and to analyze the parameters that affect the threshold voltage and substrate bias sensitivity (body-effect). Finally, the mechanism and effect of hot-carrier injection and trapping in the insulator are discussed.

The discussion of the Metal Insulator Silicon and gate controlled structures brings out much of the physics needed to describe the fundamentals of IGFET's. Chapter 6 begins with a description of basic processing technologies of typical IGFET's followed by an analysis of the current-voltage characteristics of devices having large dimensions and uniform and nonuniform substrate profiles. Major IGFET reliability considerations are discussed. This includes the mechanism of substrate and channel hot electron effects and transient upsets due to the incidence of single energetic particles. Second-order effects, such as short and narrow channel effects are introduced together with device limitations as the device dimensions are reduced. The chapter concludes with a detailed discussion of Complementary Metal-Oxide-Silicon (CMOS) structures which has added substantial flexibility to VLSI by combining n-channel and p-channel devices on the same chip. The advantages and limitations of CMOS are detailed using a simple inverter. In particular, the SCR action (latch-up) in CMOS is related to the horizontal and vertical device geometries. The different process considerations and trade-offs are discussed and a typical CMOS technology described for illustration.

The authors hope that the book will be useful to new engineers in the field of semiconductors and that this may justify a second edition at a later time. With this in mind, they would appreciate comments from their readers.

Acknowledgements

Several explanations and illustrations were adapted from available publications which we hope to have given proper credit. In particular, we have used in chapters 1, 2 and 3 descriptions from the SEEC series, as referenced in the text.

We thank all the students and colleagues at IBM for their invaluable discussions and suggestions for improving the manuscript and the course. We also wish to express our thanks to Dr. J. Uyemura, Georgia Institute of Technology, and Dr. W. Bidermann, Digital Equipment Corporation for reading all the book prior to publication and helping improve it. In particular, Dr. Uyemura's critical reading of the text has resulted in several changes and improvements.

One of us (BEK) is grateful to Dr. W.P. Noble Jr. (IBM), for not only allowing him to use some of his notes and figures on the short and narrow channel effects but also for carefully reading and correcting the last two chapters, and to R. C. Flaker (IBM) for reading and correcting the chapter on bipolar transistors.

BEK remains deeply grateful to his dear friend and colleague Dr. A.F. Puttlitz (IBM) for patiently and thoroughly reading the entire book in manuscript and then in proof stage and relentlessly solving several problems, checking the numerical accuracy and correcting the errors. We and not he take the full blame for the remaining errors.

For allowing us the adaptation or reprint of their figures and illustrations acknowledgement is due to J. Wiley Publishing Co. for figures 2.25, 2.26 and 2.27, Pergamon Press Inc. for figure 1.16, MC Morgan-Grampian Publishing Co. (Benwill Publishing Corp.) for figures 1.25, 1.26, 1.27 and 1.29, Bell Telephone Labs. for the nomograph in table 2.1, Tektronix Inc. for figures 3.10, 3.11, 3.13, 3.29 and 3.32, and Academic Press Inc. for figure 6.18.

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BEK, RJB

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CHAPTER 1

RESISTANCES AND THEIR MEASUREMENTS

1.0 Introduction

Electric current is the flow of charged particles. In order to contribute to the current, the charged particles must be free to move. In metals the carriers of electricity are negatively charged free electrons. In semiconductors such as silicon there are two types of carriers, namely free electrons and positive holes. If silicon, a group IV element, is doped with elements of the fifth group, such as arsenic or phosphorus, the concentration of free electrons increases while the concentration of holes decreases. In this case silicon becomes n-type, since it contains electrons as majority carriers and holes as minority carriers. When silicon is doped with elements of the third group, such as boron, it becomes p-type with holes as majority carriers and electrons as minority carriers. At room temperature the carriers have enough thermal energy to keep in constant but random motion as illustrated in figure 1.1.

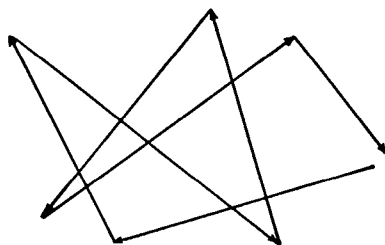


Fig. 1.1 Random motion of a carrier in a crystal. Each arrow represents a random path between collisions. On the average the carrier does not move in a particular direction. At room temperature the carriers fly at a velocity of about 10^7 cm/s between collisions.