1989 IEEE International Conference On Computer-Aided Design

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Digest of Technical Papers

IEEE Computer Society Press

Washington ● Los Alamitos, CA ● Brussels ● Tokyo

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Published by

IEEE Computer Society Press
10662 Los Vaqueros Circle
Los Alamitos, CA 90720-2578

Cover designed by Jack I. Ballestero

IEEE Computer Society Press Order Number 1986
Library of Congress Number 89-81340
IEEE Catalog Number 89CH2805-0
ISBN 0-8186-1986-4 (paper)
ISBN 0-8186-5986-6 (microfiche)
ISBN 0-8186-8986-2 (case)

Additional copies may be ordered from:

IEEE Computer Society
Terminal Annex
P.O. Box 4699
Los Angeles, CA 90080

IEEE Service Center
445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331

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13, Avenue de l'Aquilon
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Foreword

On behalf of the Executive and Technical Program Committees, it is our pleasure to welcome the participants of the Seventh IEEE International Conference on Computer-Aided Design, and to present to you this Digest of Technical Papers.

This year the task of selecting 126 papers out of 415 submissions was extremely challenging due to the high quality of the submissions. We sincerely appreciate the efforts of the world-wide CAD community and are convinced that you will agree that the technical program is excellent. We received papers from 20 countries, which confirms the international nature of the conference. More than one-third of the papers came from industry.

To be able to handle full paper submissions, we expanded the Technical Committee to 68 world-renowned experts. The committee was divided into nine subcommittees with at least seven members in each subcommittee. There was one representative from Europe and one from Asia in each subcommittee. The committee worked extremely hard -- not only at paper selection, but also at providing authors with substantial feedback on their submissions.

To complement the technical sessions, we are including in the program two excellent panel discussions with international representation, and four excellent tutorials taught by experts in their respective fields. Please note that we have moved the tutorials to Thursday.

As in past years, we would like to promote and encourage professional interaction outside of the technical sessions by providing daily breakfasts and lunches, plus a cocktail party and dinner banquet, for all conference attendees. (All of these functions are included in the conference registration fee.) This year's banquet will feature a chamber music group as opposed to the traditional invited speaker.

We are looking forward to yet another successful conference and hope to see you in Santa Clara. Thank you for participating in ICCAD-89.

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Tutorial: New Trends in Testing and Verification

Srinivas Devadas, *MIT*
Kurt Keutzer, *AT&T Bell Laboratories*
A. Richard Newton, *University of California, Berkeley*

Background: It is suggested that participants have some background in switching and automata theory and/or the basics of logic design. A familiarity with logic synthesis also will be helpful.

Due to smaller design rules and greater levels of integration, each improvement in IC technology eases the difficulty of designing a circuit that achieves given performance and area requirements. On the other hand, the problems of design verification, implementation verification, and manufacture testing become much more difficult because of the increase in functionality per chip, increased levels in the design hierarchy, and decreased observability at the pins of the chip.

In this tutorial we explore new solutions to these verification problems. First, we consider the problem of design verification—verifying that the original design meets its specification—and will discuss non-simulation approaches to this problem, such as formal verification and symbolic simulation. We then consider new techniques in implementation verification—verifying that the design remains correct across the hierarchical boundaries as it progresses from function to logic to layout. Here we consider algorithms for formally verifying the equivalence of two sequential machines described at the register-transfer, state table or logic level. Finally, we will consider the problem of manufacture test and will treat current work in the area of synthesis for testability showing how novel synthesis approaches can produce combinational and sequential circuits with unprecedented levels of testability.

Tutorial: Mixed Analog/Digital Simulation

Karem Sakallah, *University of Michigan*
Resve Saleh, *University of Illinois, Urbana*

Background: Tutorial participants should be familiar with the use of circuit and logic simulators. Knowledge of the underlying algorithms is desirable but not necessary.

Mixed analog/digital simulators were introduced over 10 years ago to complement circuit and logic simulators in the verification of VLSI circuits. By combining analog (electrical) and digital (logic) models in one simulation framework, mixed-mode simulators can succeed in verifying chips for which detailed electrical simulation is too expensive (infeasible), and for which the accuracy of logic simulation is inadequate. The demand for mixed-mode simulation has accelerated over the past couple of years because of the rapid growth in the number of hybrid analog/digital chips in many application areas (automotive, telecommunication, etc.).

This tutorial covers the theory and application of mixed-mode simulation. The tutorial is organized in four parts. Part 1 introduces the concept of mixed analog/digital simulation, and provides the necessary theoretical background for the remaining parts. Part 2 covers the various algorithms for circuit-, logic-, and switch-level timing simulation and their associated implementation issues. Multi-level interfacing issues such as signal mapping, event scheduling, and feedback handling are addressed in Part 3. The tutorial concludes by looking at the available commercial and academic software for mixed-mode simulation, and by providing some directions for future work in this area, including fault simulation and parallel processing.

Tutorial: Multi-Level Logic Synthesis

Robert K. Brayton, *University of California, Berkeley*

Background: This tutorial should be appropriate for people who have some knowledge of digital logic design, who would like a more global perspective of this emerging and important field, or who are considering pursuing or assessing these topics in more depth later. Knowledge of testing, two-level minimization, combinatorial optimization techniques, timing analysis and verification is useful but not necessary.

In this tutorial, we will survey the synthesis techniques that have been established as having practical significance as well as some theoretical developments which we judge promising for the future. The tutorial will be confined to combinational logic, although relations to emerging research areas in sequential logic synthesis will be referenced. We will begin by exploring the role that multi-level logic synthesis plays in the transformation from a high-level description to layout.

The techniques to be presented can be classified into two groups: those used for decomposition of logic functions yielding a multi-level structure, and those which perform optimizations on this structure. The first group of algorithms includes the algebraic methods which have been used in many commercial products and production codes because of their speed and relative effectiveness. Also included is the important area concerning restructuring for meeting timing constraints. The second group can as well be called don't care based methods since a common theme is the use of don't cares to achieve the optimizations. These methods include ones based on two-level minimization applied to the multi-level environment, but also techniques such as global flow, transduction, and ATPG based methods.

The methods mentioned above are considered technology independent. These are usually followed by technology-dependent methods which do the final mapping of the optimized structure into a given library of available gates. These include rule-based methods and technology mapping. We survey this area and include some recent techniques for optimally trading area for delay.

Tutorial: Analog VLSI CAD

Phillip Allen, Martin Brooke, and Giorgio Casinovi
Georgia Institute of Technology

Background: A familiarity with integrated circuits and analog integrated circuit design is recommended.

Analog integrated circuits have evolved into a format which combines both digital and analog circuits according to cost and performance criteria. This result is due to the development of analog design methodologies suitable for digital integrated circuit technologies. Such integrated circuits represent a growing segment of the IC market and offer many challenges. This tutorial addresses the anticipated problems and potential solutions to enable analog IC design to be a viable solution for the 1990s.

This tutorial will first survey design methodologies which will maintain and enhance performance and speed in submicron VLSI technologies. Automated methods of designing and physically defining analog circuits and systems will be reviewed and compared. The subject of hierarchical analog modeling having adjustable accuracy capability will be described. Specialized analog simulators for discrete time circuits, mixed analog-digital circuits/systems, and nonlinear frequency analysis will be discussed. Finally, the tutorial will look at the present state of analog testability, the problems that need to be solved, and possible solutions.

Panel Session 1: CAD Directions: Is Anyone Steering?

Moderator
Michael R. Lightner, *University of Colorado, Boulder*

Panelists
Y. Hatano, *Fujitsu*
W. Lattin, *Logic Automation*
M. Vanzi, *SGS-THOMSON Microelectronics*
C. Goldstein, *Apple Computer, Inc.*
J. Toole, *DARPA*

Initially, CAD tools were completely motivated by designer needs to get a particular job done. This not only created an industry but initiated guided research funding from government sources to research laboratories and universities. The panel will discuss the current motivating forces selecting the future directions of CAD development. The concern is that the direction more closely resembles a random walk than a guided march! Who should or could be supplying this direction?

Panel Session 2: 10x, 100x, and 1000x Speed-ups in Computers: What Constraints Change in CAD?

Moderator
Tom Blank, *MasPar Computer Corporation*

Panelists
A.R. Newton, *University of California, Berkeley*
T. Adachi, *NTT*
J. Costello, *Cadence Design Systems, Inc.*
H.G. Adshead, *ICL*
M. Butts, *Mentor Graphics Corporation*

In the next five years, computers will have significant price/performance improvements ranging from 10x to 1000x over what is available today. Currently, many CAD programs and methodologies are severely limited by performance. The panel will discuss the implications of these new computing engines in CAD. What constraints are removed? What new paradigms are possible? What pitfalls will be encountered making the changes?

Acknowledgments

The Executive Committee of ICCAD-89 would like to extend its deepest gratitude to the following persons for all efforts on behalf of the Conference and its publications.

Shirley Farinella *(Carnegie Mellon University)*	Handled all communications for the General Chair.
Kathy Samudovsky *(Carnegie Mellon University)*	Produced camera-ready copy for the technical sessions of the Advance and Final Programs. Supervised and coordinated the manuscript recording procedures for the Program Chair.
Flora Oviedo *(University of California, Berkeley)*	Assisted with the manuscript recording procedures and handled all communications for the Program Chair.
Michael Haggerty *(IEEE Computer Society Press)*	Coordinated the production of the Digest and mailing of authors' kits.
Anne Marie Kelly *(IEEE Computer Society)*	Coordinated the manuscript receipt and mailing procedures for conference submissions. Special thanks for her extraordinary dedication.
Nancy Shoupp Regina Pistilli *(MP Associates, Inc.)*	Assisted with the coordination and production of the Advance and Final Programs.

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(Moderators: G. De Micheli, *Stanford University;* A. Parker, *University of Southern California*)

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(Moderators: R. Bryant, *Carnegie Mellon University;* T. Kozawa, *Hitachi Ltd.*)

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(Moderators: H. De Man, *IMEC and K.U. Leuven;* Y. Nakamura, *NTT*)

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(Moderators: K. Kundert, *Cadence Design Systems, Inc.;* J. White, *MIT*)

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(Moderators: U. Lauther, *Siemens AG;* E.J. Yoffa, *IBM Corporation*)

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(Moderators: J. Allen, *MIT;* G. De Micheli, *Stanford University*)

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(Moderators: M. Lightner, *University of Colorado, Boulder;* R. McGeer, *University of California, Berkeley)*

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(Moderators: A.E. Dunlop, *AT&T Bell Laboratories;* S.M. Kang, *University of Illinois, Urbana*)

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