Semiconductor Circuit Design

Vol. II

Edited by: Bryan Norris, Manager, Applications Laboratory, Texas Instruments Limited

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TEXAS INSTRUMENTS
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Preface

Encouraged by the success last year of our publication, *Semiconductor Circuit Design*, I have compiled, under the same title, this second volume of additional circuit designs using a wide range of semiconductor devices.

The book is divided into three sections, Digital Integrated Circuits, Operational Amplifiers and Optoelectronics, and each one is preceded by an introductory chapter.

The first section, Digital I.C.s, describes in its second chapter Schottky transistor-transistor logic considered to be of future major importance especially in its Low Power form. The section continues by adequately covering interface devices, counters, selectors, decoders, converters etc. and concludes with a chapter describing a means of performing high speed multiplication using read-only memories.

The second section, Operational Amplifiers, continues the pattern of introductory chapter followed by applications and ends with a chapter on Stereo Amplifiers—in response to the enthusiasm with which the audio section in Volume One was received.

The introductory chapter to the third section, Optoelectronics, attempts to illuminate the theory and practical considerations that apply when making these new and interesting semiconductor devices.

I wish to thank all my colleagues for their help and especially David Bonham and Bob Parsons, who not only wrote a number of the chapters, but acted as my technical specialist consultants throughout the preparation of this book.

Also, I thank the editors of *Practical Wireless* for their kind permission to use articles from the May, June, July and August 1972 issues, as a basis for Chapter XVI.

BRYAN NORRIS

Applications Manager
Texas Instruments Limited
April 1973

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I INTRODUCTION TO TTL

by David A Bonham

Modern TTL is the result of more than a decade of evolution from early attempts to produce integrated circuits instead of discrete component circuits. It is interesting to look back at the history of digital integrated circuits and examine the ways that they evolved to appreciate the virtues of TTL.

The first commercially available integrated circuits Texas Instruments produced in 1959 were the SN502 series. They featured mesa construction and wire interconnections as shown in Figure 1. This approach is feasible where a limited number of circuits are required; but it is not economic where one wishes to attain volume production. The first true catalogue lines of integrated circuits were resistor-transistor logic, RTL, and Series 51 resistor-capacitor-transistor logic, RCTL shown in Figure 2. These were now monolithic in construction and planar diffused. However, from a circuit point of view, they suffered by having poor fan-out, about three or four, and a low dc noise margin. They did feature low power, about 2 to 7 mW/gate, depending upon the supply rail chosen.

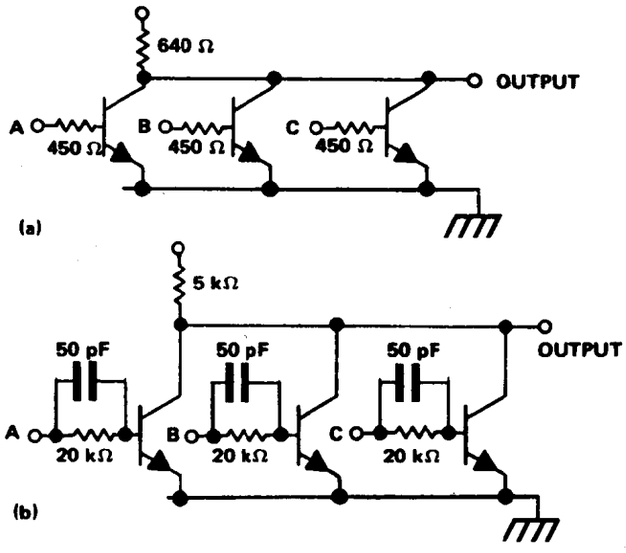


FIGURE 2. Basic Schematics of: (a) RTL Integrated Circuit, and (b) Series 51 RCTL Integrated Circuit

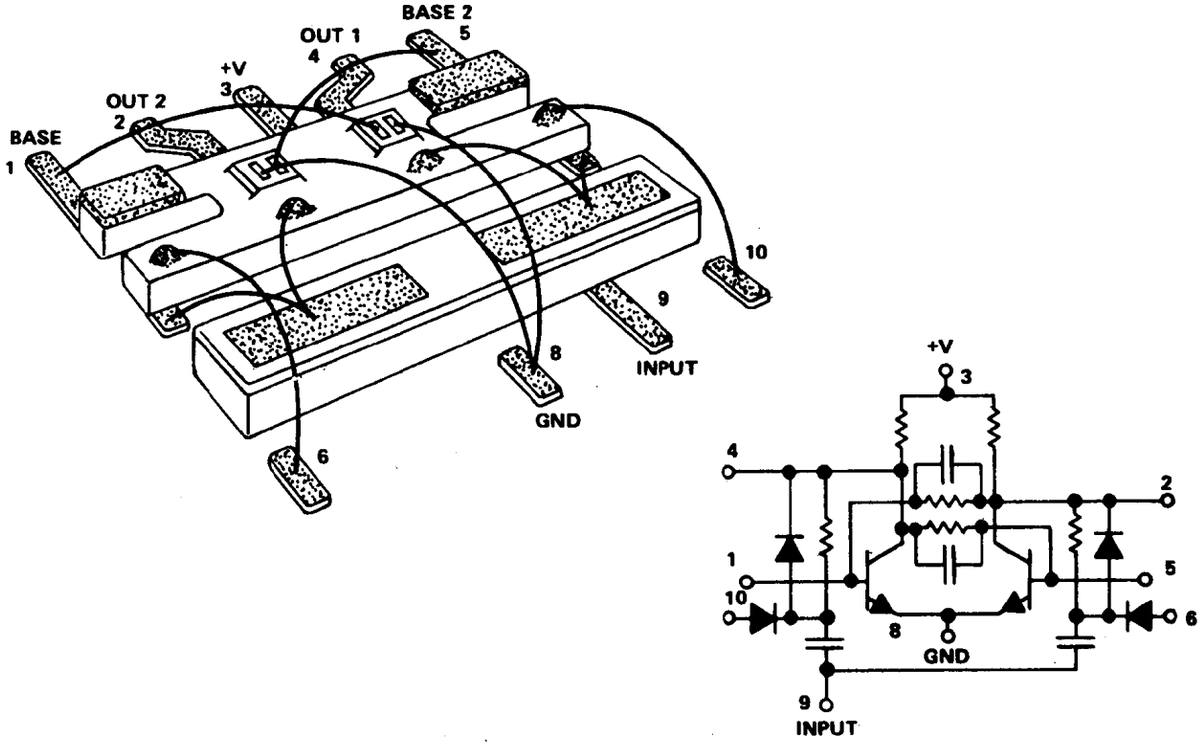


FIGURE 1. SN502 Series Integrated Circuit, Mesa Construction

The next advance was diode-transistor logic, DTL, as shown in Figure 3(a). This had a good fan-out and a good noise immunity. However, it suffered from poor yields, due to the design allowing only a small variation of component values. Another disadvantage was the requirement of a negative supply which in turn took an extra pin on the package. So far the designs had been a mere translation of discrete circuits into a monolithic form. To keep down the cost of logic, cheap components are used where possible.

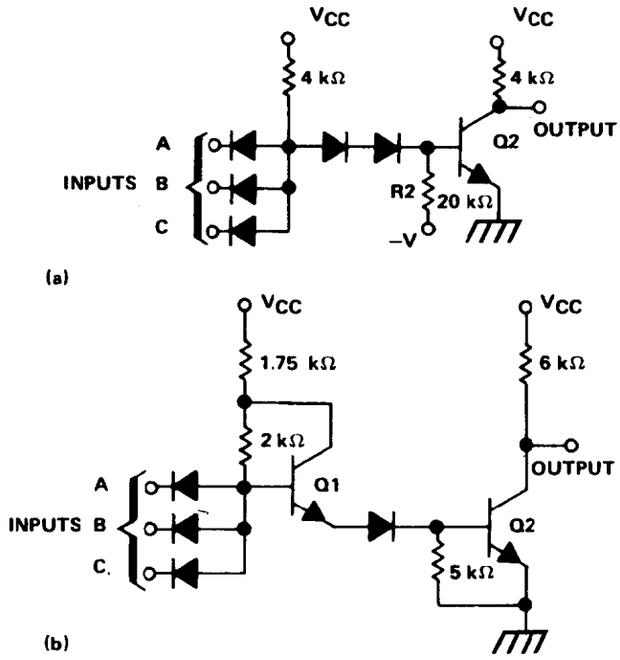


FIGURE 3. Basic Schematics of: (a) DTL and (b) Modified DTL Integrated Circuits

However, when one turns to making monolithic devices, the cost also depends upon the yields obtained. It costs very little more to make a transistor in an integrated circuit than it does to make a diode, and yet by incorporating the transistor one can probably obtain better performance. This was the philosophy that led to the introduction of modified DTL. A transistor is used in place of one of the diodes. If one compares Figures 3(a) and 3(b) one will see that transistor Q1 provides more current for transistor Q2 than the original diode arrangement. Because more current is now available, one can both use a smaller pull-down resistor on the base of transistor Q2 and have a wide range of current gain, h_{FE} and still get a correctly operating gate. This gives a higher production yield and a lower cost per gate.

Next, instead of replacing just one diode, transistors were used in place of all the diodes. This logic family, the basic NAND gate of which is shown in Figure 4(a) was called Series 53/73. A pnp transistor has replaced each input diode so that the input current is divided by the h_{FE} of the transistor. Because the substrate is p type material, it is only necessary to diffuse an n region as the base, or input terminal, and a p region within this as the emitter as shown in Figure 4(b). There is another advantage that is gained from monolithic construction on a p type substrate.

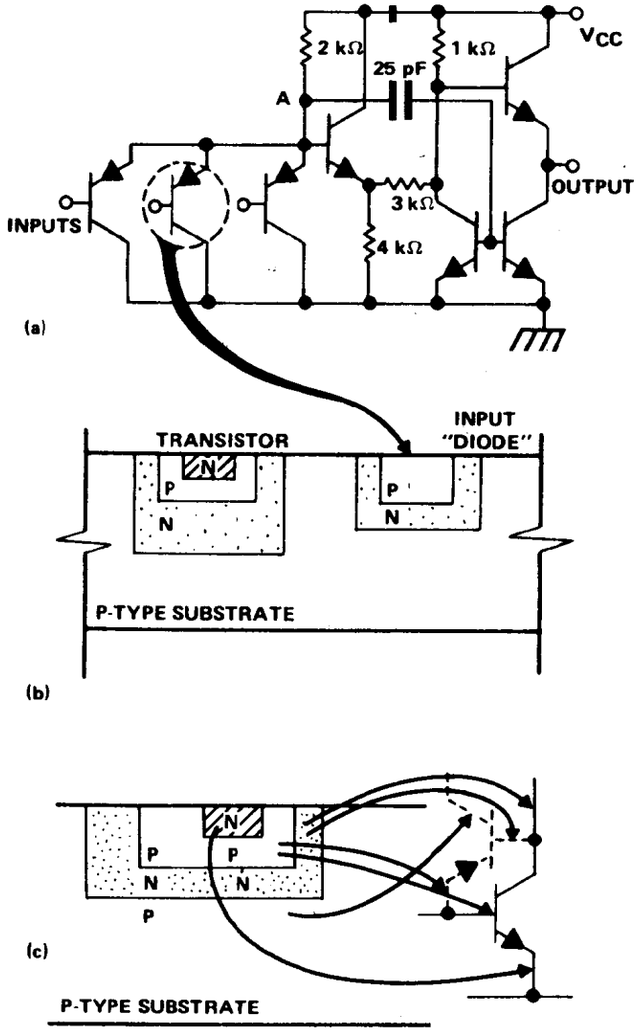


FIGURE 4. Series 53/73 Integrated Circuits: (a) Basic NAND Gate, (b) Cross-Section of Transistor and Input "Diode", (c) Formation of an npn Transistor in the Substrate Also Produces a pnp Transistor

Forming a npn transistor in the substrate also produces a pnp as shown in Figure 4(c). When the npn transistor would normally be driven hard into saturation the pnp comes into conduction and shunts excess base current into the substrate. This reduces stored base charge and thus improves the switching time of the npn transistor. The Series 53/73 devices have a fan out of 10, thanks to the pnp input transistors, a low impedance output in both logical states, and are easy to use. However, they require seven transistors to a basic gate occupying a large area so that the cost could never be really low, and the noise margin could be rather small. Notice the output circuit arrangement, with its one transistor above another. This is

known as a totem-pole configuration and can provide i.e. 'source', or accept, i.e. sink, current.

The next circuit advance was to use a multi-emitter transistor, instead of diodes or transistors, forming a gate at the input. This resulted in the transistor-transistor logic circuit shown in Figure 5 with its planar construction as shown in Figure 6. The advantages of the multi-emitter transistor are that it takes less area than the equivalent number of diodes and that it has a faster speed. The speed of TTL is in fact about twice that of DTL.

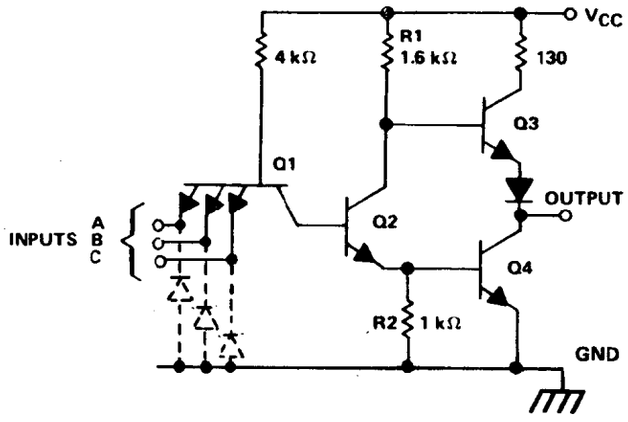


FIGURE 5. Typical TTL Circuit

Another advantage of TTL lies in its totem-pole output. This gives low impedance drive in both high and low output states providing high speed with the ability to drive capacitive loads. In general, the totem pole outputs cannot be wired together (Wire-OR). So to allow Wire-OR, open collector gates are made, which are the same as the totem pole gate but without the upper output transistor. Totem poles and Wire-OR (or, more correctly, Wire-AND) will be described in greater detail in later sections. Although it is not usually shown on the circuit diagram, there is a diode from a point on the 4 kΩ resistor to the collector of the input transistor. The purpose of this diode is to limit the base current into the multi-emitter transistor so that it only just saturates when the input is low. It also limits the base current when the inputs are high. This has the effect of keeping stored charge in the transistor down to a minimum thereby giving optimum switching times for this input transistor.

To the standard range of TTL, which was introduced in 1964, have been added Low Power, High Speed, Schottky and Low Power Schottky ranges. All have the same basic circuit configuration and are compatible with each other in such things as supply and logic voltages. However, there is a compromise between speed and power. This is because to achieve higher speed and lower propagation delays the circuit resistor values have to be reduced. This reduces all the time constants with base capacitances, stored charge, stray and load capacitances, thus giving a faster propagation of the signal through the gate. Of course, reducing the resistor values means a higher power consumption. Thus it happens that the product of power and speed for a family is approximately constant. So if one plots Low Power, Standard TTL and High Speed, as in Figure 7, they lie on the same hyperbolic curve. Adding Schottky clamp diodes improves the speed of the family without increasing power, so the two Schottky families lie on a better curve. One could design a family to lie anywhere along the curves. The different powers and speeds of the families are shown in Table 1.

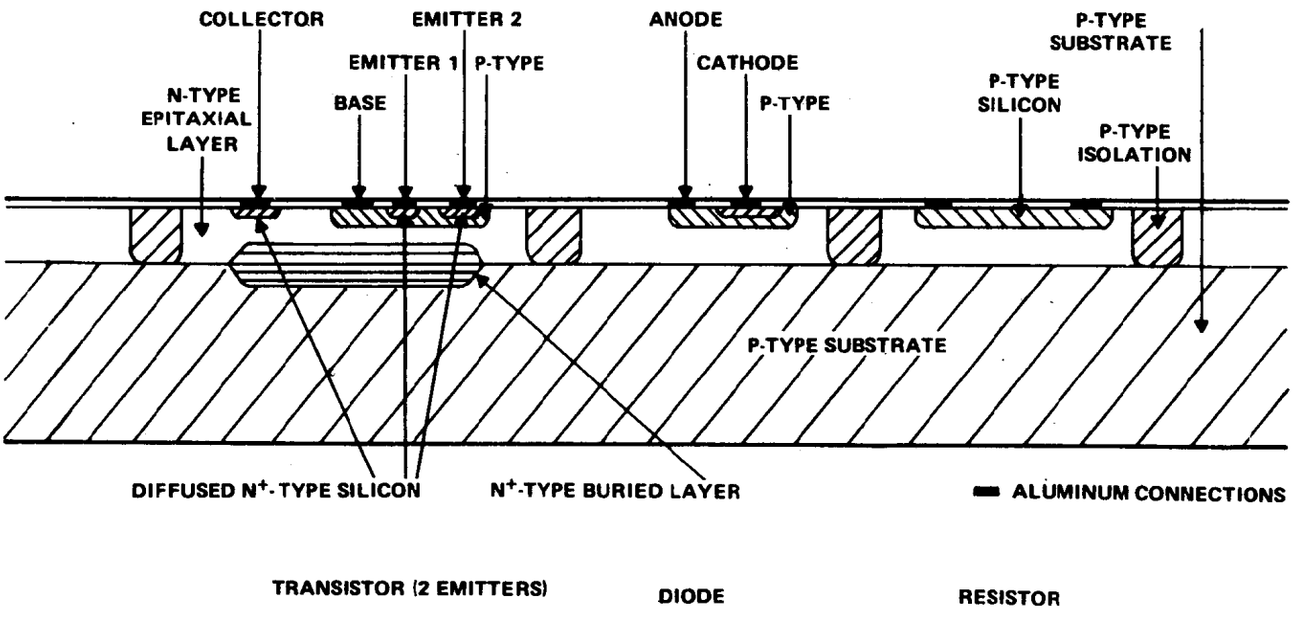


FIGURE 6. Cross Section Showing Planar Construction of Typical TTL Circuit

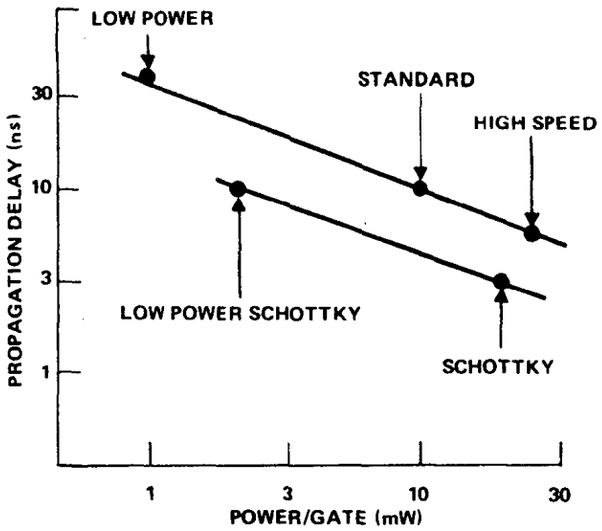


FIGURE 7. Power-Speed Compromise of the Various Types of TTL Circuits

Table 1.

Type Of TTL	Speed ns	Power mW	Product pJ
Low Power	33	1	33
Low Power Schottky	10	2	20
Standard	10	10	100
High Speed	6	23	138
Schottky	3	19	57

THE DATA SHEET

Before studying the data sheet it is useful to examine the philosophy behind it.

Worst-Case Worst-Case Philosophy

The data sheet limits are not all given for a typical value of supply voltage and room temperature. Each maximum or minimum parameter meets the data sheet value at the worst supply voltage for that parameter. Thus two different parameters may be measured at different supply voltages: one with the maximum positive tolerance and the other with the maximum negative tolerance. Additionally, both parameters are guaranteed over the whole of the temperature range. Therefore, every data sheet limit is for the worst combination of supply and temperature. The advantage of this is that any device will connect correctly to another device, which may be in another part of an equipment, with a different supply voltage and ambient temperature.

This worst-case worst-case method of specifying device characteristics is most important as it removes from the designer the need to check, either mathematically or physically, if devices will interconnect correctly. Apart from observing voltage, temperature and fan out ranges, there is normally no need to study the data sheet. However, the data sheet does tell one how to interface the logic with external inputs and outputs.

There are two further points which should be examined here. The first is that, in general, Positive Logic is used. This means that a logical '1' is a high voltage and logical '0' is a low voltage. On the data sheet, high and low voltage conditions are often abbreviated to H and L.

The second point is concerned with device numbering. Each integrated circuit is known by perhaps seven or eight characters, such as SN7400N. The device is listed under this name rather than its logic function which is, in this case, a quad two input NAND gate. How the group of characters is made up and their relevance, is explained in the next section on symbolization.

Symbolization (Device Recognition)

SN54H102N

The above is a typical TTL device symbolization. It can be divided into distinct parts each of which tell us something about the device.

SN/54/H/102/N

SN This is the standard prefix for a Semiconductor Network. There are variations such as: RSN; BL; and SNX; which indicate a Radiation Hardened Circuit, a Beam Lead constructed device, or an Experimental Circuit respectively.

54 TTL is available to meet three temperature ranges. Prefixes 54, 64, and 74 distinguish them

Series 54 =	−55 to + 125°C	Military
Series 64 =	−40 to + 85°C	
Series 74 =	0 to + 70°C	Industrial

There is also a difference in the supply voltage range.

Series 54 =	4.5 V to 5.5 V
Series 64 and 74 =	4.75 V to 5.25 V

H Indicates a High Speed device.
The letter(s) might have been:

L : Low Power
or S : Schottky
or LS : Low Power Schottky.

or there might have been no letter which would indicate a Standard family device.

102 The next two or three numbers show the device function (102 = JK Flip Flop).

N This letter is the package type. There are 11 possibilities shown in the data book but N is the most widely used.

N = 14, 16 or 24 pin dual-in-line plastic.

SN54H102N. It should now be apparent that the above example is a High Speed J-K Flip Flop meeting the military temperature range.

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7.0 V
Input Voltage, V_{IN} 5.5 V

There may be electrical breakdown and irreversible damage if the V_{CC} is raised above 7.0 V. This does not imply that one gets correct logical operation for all voltages below 7.0 V.

The Input Voltage with respect to ground (or the most negative input) must not be greater than 5.5 V. The input will tolerate a maximum current into the gate of about 2 mA. Thus where inputs do not go to an output but to the supply rail, then a current limiting resistor should be included if it is possible that there may be transients on the rail, or negative undershoots on other inputs to that input transistor.

Basic Data Sheet

A line-by-line examination of the data sheet for the basic gate shown in Figure 8 will show what relevance the parameters have for the user.

1. Title. Data sheets are usually for both Series 54 and 74 devices. Apart from pin connections, data sheet parameters are the same regardless of the package.

2. Schematic. Resistor values are nominal and may vary by ± 20%.

Pin Configuration. Note that the pin connections for flat package are not necessarily the same as dual in line.

The logic symbols, which are used in both data sheets and application reports, are shown with their meaning in Figure 9 (positive logic).

3. Although the devices will operate outside the stated limits of voltage and temperature, some of the parameters may then be outside the data sheet limits.

4. and 5. Voltage ranges over which the series are specified. Series 64 is the same as Series 74.

6. Fan-Out is the number of standard loads (standard inputs) that the circuit outputs will drive correctly, i.e., with full noise margin. See section on Fan-Out.

7. and 8. Temperature ranges over which the series are specified. Series 64 is specified for the temperature range of −40 to +85°C. In all other respects however, it is identical to Series 74.

9. The table following is of typical and worst-case worst-case characteristics.

10. and 13. When the input voltage is greater than 2.0 V, the output will be less than 0.4 V even when sinking 16 mA, and even when V_{CC} is the minimum applicable value as in 4 and 5.

11. and 12. When the input voltage is less than 0.8 V, the output will be greater than 2.4 V even when sourcing 400 μA, and even when V_{CC} is the minimum applicable value as in 4 and 5.

14. When the input is taken down to 0.4 V the input will source a maximum of 1.6 mA even at the maximum supply. This is due to current flowing from the V_{CC} rail via the base resistor of the input transistor as shown in Figure 10.

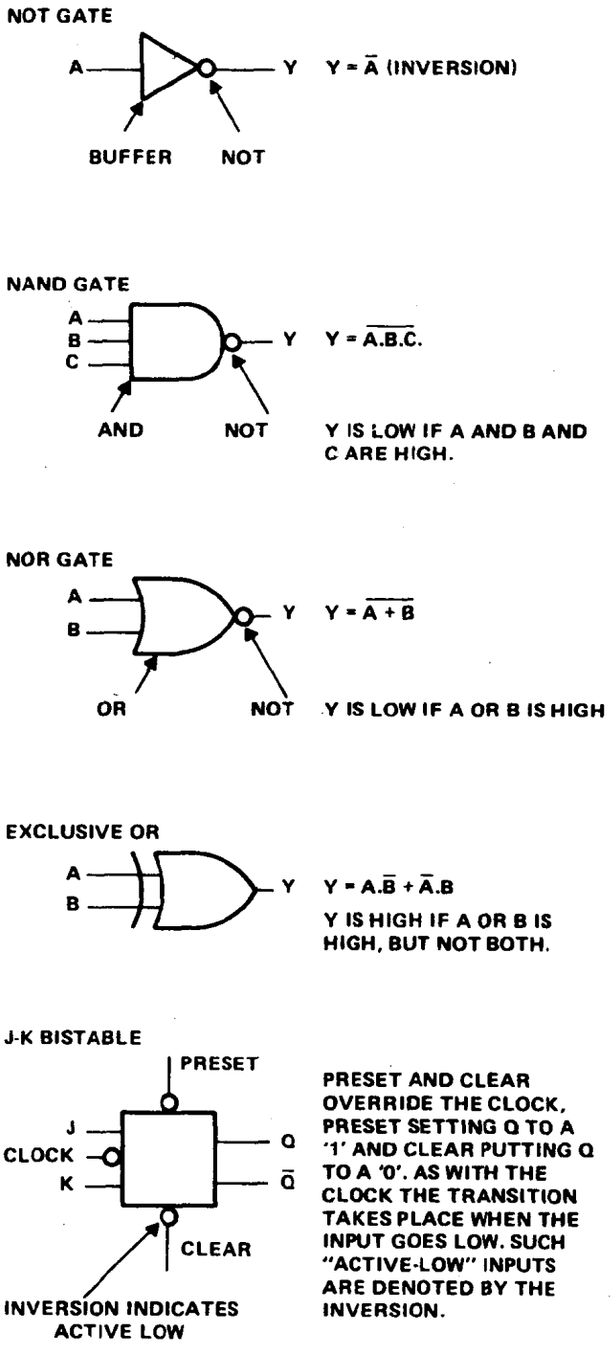


FIGURE 9. Logic Symbols (Positive Logic)

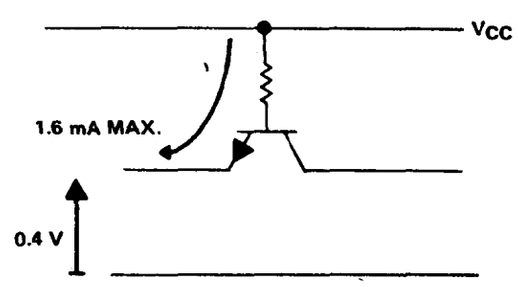
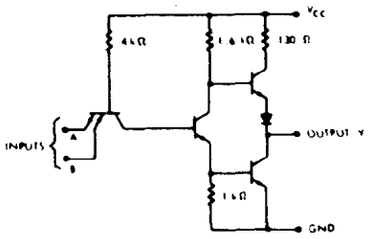


FIGURE 10. Input Current (Logical '0')

CIRCUIT TYPES SN5400, SN7400
QUADRUPLE 2-INPUT POSITIVE NAND GATES

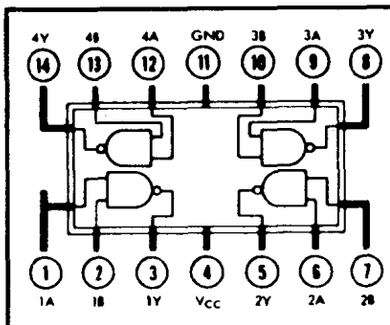
(1)

schematic (each gate)

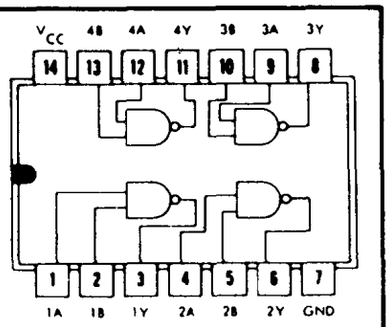


NOTE: Component values shown are nominal.

W FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



(2)

positive logic: $Y = \overline{AB}$

recommended operating conditions

		MIN	NOM	MAX	UNIT	
Supply Voltage V_{CC}:	SN5400 Circuits	4.5	5	5.5	V	(3) (4)
	SN7400 Circuits	4.75	5	5.25	V	(5)
Normalized Fan-Out From Each Output, N				10		(6)
Operating Free-Air Temperature Range, T_A:	SN5400 Circuits	−55	25	125	°C	(7)
	SN7400 Circuits	0	25	70	°C	(8)

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

(9)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT	
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 level at output	1			2			V	(10)
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 level at output	2					0.8	V	(11)
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V	(12)
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V	(13)
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA	(14)
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA	(15)
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA	(16)
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN5400	−20		−55	mA	(17)
				SN7400	−18		−55		(18)
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			12	22	mA	(19)
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0			4	8	mA	(20)

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		7	15	ns	(21)
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		11	22	ns	(22)

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

FIGURE 8. Data Sheet for TTL Circuit Types SN5400 and SN7400

15. When the input is taken up to 2.4 V it will sink up to 40 μA even when the supply is the maximum. (14 and 15 define the standard load)

16. If the input is taken to 5.5 V, it will sink a maximum of 1 mA even at the maximum supply. This is a breakdown condition.

17. and 18. If the output terminal is taken down to ground when the gate output is in the logical '1' state, this is the current which will flow out of the output terminal.

19. and 20. This is the total current taken by the package at typical and worst case supply and inputs.

21. and 22. Propagation delays measured using a circuit as in Figure 11 to simulate 10 standard loads.

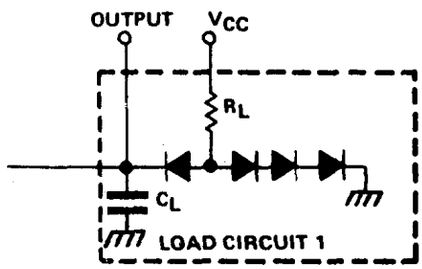


FIGURE 11. Circuit Used to Measure Propagation Delays

For thoroughness, a test figure is given for each of the lines 10 to 20 showing the configuration in which the parameter is measured.

The user should not allow himself to be intimidated by the above explanation of the data sheet. All that one needs to remember is the following:

> A gate (or any other function) can adequately drive up to 10 inputs, be they to gates or complex functions.

This statement is the basis of the following section on Fan-Out.

Fan-Out

As stated previously, in line 6, fan-out is the number of standard (or normalized) loads that can be driven by an output. For each load an output may have to sink 1.6mA when it is low and source 40μA when it is high. As lines 13 and 12 respectively state in the example of the SN7400, the output of the gate can sink 16 mA before the saturation voltage of the output transistor exceeds 0.4 V and it can source 400 μA before the output voltage drops below 2.4 V.

logical '0' = 16/1.6 = 10, fan-out logical '1' = 400/40 = 10. fan-out

Therefore, the SN7400 has a fan-out of 10 in both logical states.

All new devices are being tested at 800 μA at logical '1' instead of the 400 μA. This gives a fan-out of 20 in the logical '1' state.

When an unused input is paralleled with a used one, it is necessary to sink a maximum of 1.6 mA from the input transistor, or source 40 μA maximum into each of the inputs. Thus, two inputs of the same gate paralleled presents a load of 1 in the logical '0' state and 2 in the logical '1' state.

Thus, a total of 10 unused inputs can be paralleled with used inputs, without exceeding the fan-out capability of the output. Eventually all devices will be specified at 800 μA. Actually the difference between 400 μA and 800 μA, with an output impedance of 150 Ω, represents a drop in output voltage of only 60 mV anyway.

DC Characteristics

The Transfer Characteristics of the gates of all the families are very similar in terms of voltage. They look like the curve in Figure 12.

The input and output characteristics of standard TTL will now be examined with reference to the data sheet limits. They are shown in Figures 13 and 14. The importance of various parts of the characteristics is given on the figure. The circled numbers correspond to the relevant line of the data sheet.

The input and output characteristics of the other TTL families are all contained in the Bergeron diagrams in a later section. Although to differing scales of current, they are all the same basic shape.

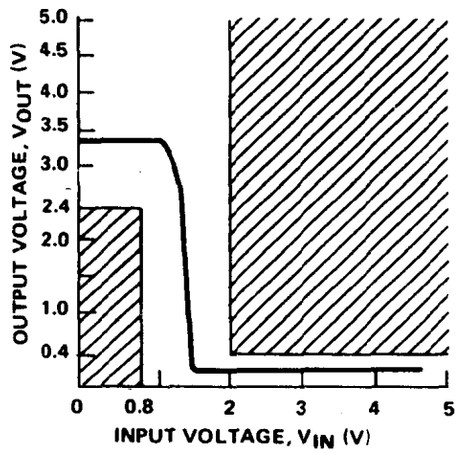


FIGURE 12. Transfer Characteristics of a Gate

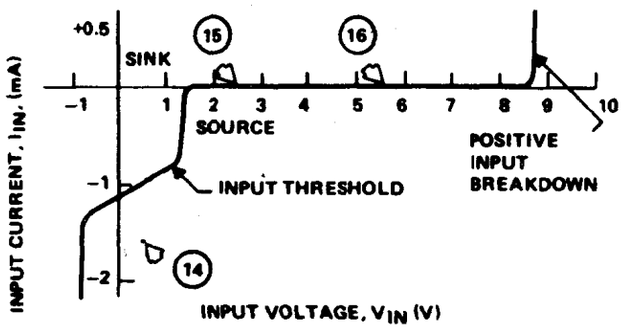


FIGURE 13. Input Characteristics of Standard TTL

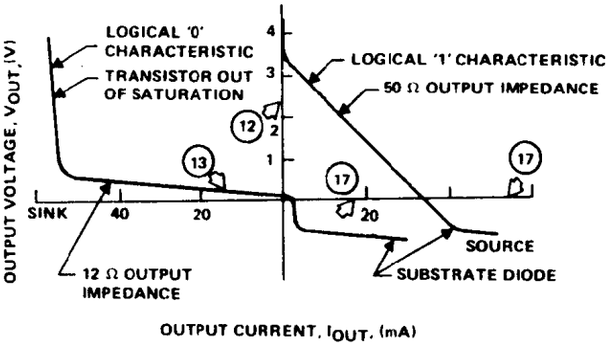


FIGURE 14. Output Characteristics of Standard TTL

LOGIC GATES AND FLIP FLOPS

Standard Input and Output

Each input to a function is one standard TTL load. There are occasional exceptions: for example, clock inputs are sometimes two loads. Each output of a function is one standard output.

The standard input is usually of the configuration shown in Figure 15 and the standard output is as in Figure 16.

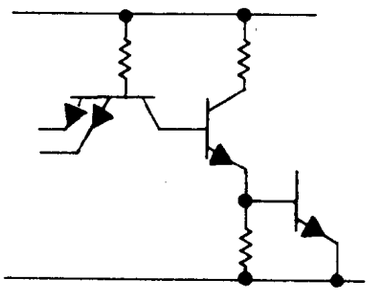


FIGURE 15. Standard Input

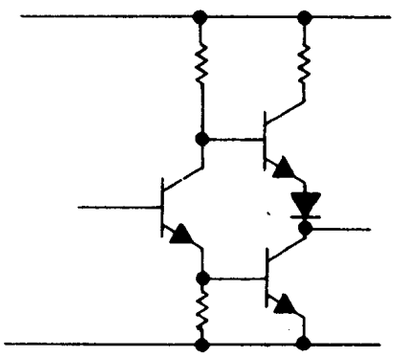


FIGURE 16. Standard Output

Combining Figures 15 and 16 gives the basic NAND gate.

NAND Logic and Karnaugh Maps

As the logic is of the NAND form, it facilitates the realization of Karnaugh maps. The latter provide a diagramatic view of all the logical terms (Yes, No and "don't care" terms) required in an expression. They allow one to obtain the simplest and most economical expression necessary. An example is shown in Figure 17. The expression can then be realized using NAND gates as in Figure 18. Karnaugh maps are explained in many books on logic and Boolean algebra.[1]

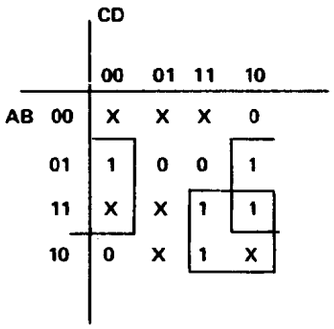


FIGURE 17. A Karnaugh Map

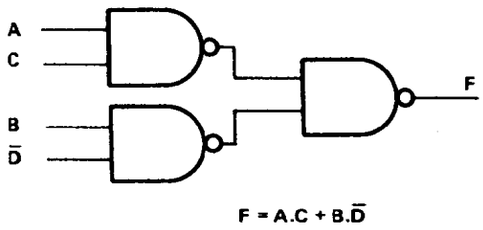


FIGURE 18. Realization of the Expression With NAND Gates

Flip-Flops

Flip-flop is a term which has come to mean a function which can be triggered into either of two stable states, i.e., a bistable element. The simplest of these is the bistable latch. This is usually made from cross coupled NAND gates but other variations are possible as shown in Figure 19. Latches can be used as memory elements.

The NAND gate version has the truth table shown in Table 2.

Table 2.

R	S	Q	$\bar{Q}$
1	1	Q	$\bar{Q}$
0	1	1	0
1	0	0	1
0	0	1	1

In line 1 of Table 2 the outputs are as they were before the R and S inputs changed. Lines two and three show the new output states which occur immediately either R or S is taken to a zero. The new state is remembered when R or S returns to a logical '1'. Line 4 can occur, but it

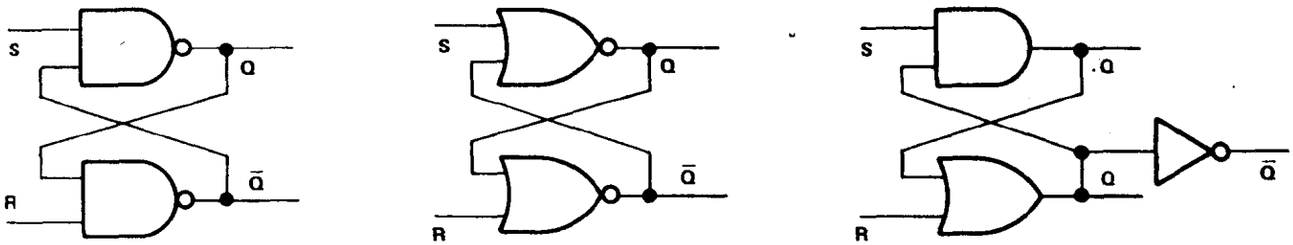


FIGURE 19. Variations of Latch Possible

is not remembered, as either R or S changes before the other, and it is this intermediate state that is remembered.

Any change in the output of a latch occurs at the same time as the input data change. This is known as 'asynchronous' operation. A 'synchronous' flip-flop is one in which the outputs change in accordance with the input data but at a time determined by a separate 'clock' input. The simple latch shown above operates asynchronously. More complex logic is required to turn a latch into a synchronous flip-flop or bistable.

There are various configurations of clocked bistable and various clock mechanisms. The three clock mechanisms will be considered first.

Ac Coupled. The clock pulse is capacitively coupled into the bistable. A fast rise is necessary to ensure propagation of this pulse. Currently none of the TTL flip-flops has this type of clock.

Dc or Edge-Triggered. Edge triggered should not be confused with ac coupled. Edge triggered is the same as level triggered. It is this, the change in dc level, that triggers the flip-flop. Either a positive or a negative transistion will clock, but not both. Although clocking is relatively independent of rise and fall times, noise immunity decreases if they are longer than about 50 ns.

Master-Slave. In this type of input the data is not immediately transferred from the data inputs to the output. It is first put into a master latch. This occurs when the clock goes high. When the clock comes low again the inputs are first disconnected from the master and then the state of the master sets a slave latch which gives the output.

Theoretically any of these three types of clocking can be used in the following bistable forms.

D-type Bistable. The data present at the input just before the clock edge is transferred to the outputs on the same edge. The SN7474 is an example of a dual D-type bistable that is positive edge triggered.

There is a variation usually called a D-type latch. With this function the data at the D input is transferred to the Q output while the clock is high and, if the data changes, Q is changed in sympathy. However, while the clock is low, the Q output retains the state it had prior to the negative edge. They are useful for data storage. The SN7475 is a quad D type latch.

T-type flip-flop. The T-type flip-flop has two inputs clock and T. It changes state (or toggles) when clocked, if the data input, T, is a logical '1'. If it is a logical 'O' there is no change. When cascaded, these devices divide by two, and, although they are not available as separate entities, they are used within such things as binary counters.

R-S Flip-flop. The outputs follow a similar truth table, shown in Table 3 to the set-reset latch. The notation used is that Q_n represents the state of the Q output before the clock pulse and Q_{n+1} after the clock pulse. The disadvantage of the R-S latch is that the output state is not predictable if R = S = 1 at clocking. From the truth table one can see that it is not always necessary to control both R and S to get the desired output. For instance if Q = O and one wishes it to remain at logical 'O' then, providing S = O, R may be a logical '1' or 'O'. It will make no difference. This is useful as it simplifies the logic design and implementation of such things as counters.

Table 3

R	S	Q_{n+1}
0	0	Q_n
1	0	0
0	1	1
1	1	Indeterminate

J-K Flip-flop. This is similar to the R-S except that the indeterminate state has been removed, and both data inputs, now called J and K, are logical '1'. The truth table, shown in Table 4, is now defined for all four combinations

Table 4

J	K	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\bar{Q}_n$

of J and K and it is no longer necessary to avoid the J = K = 1 input condition. Again, like the R-S flip-flop, one can get the desired output change by using only one of the data inputs. These are tabulated in Table 5. (Note X is the symbol used to represent a 'don't care' i.e., 'O' or '1').

Table 5

Q_n	Q_{n+1}	J K
0	0	0 X
0	1	1 X
1	0	X 0
1	1	X 1