

# VLSI DESIGN '98

**VLSI FOR SIGNAL PROCESSING**

**PROCEEDINGS OF  
THE 11th INTERNATIONAL CONFERENCE ON VLSI DESIGN**

Chennai, India  
January 4-7, 1998

**Sponsored by**



VLSI SOCIETY OF INDIA (VSI)  
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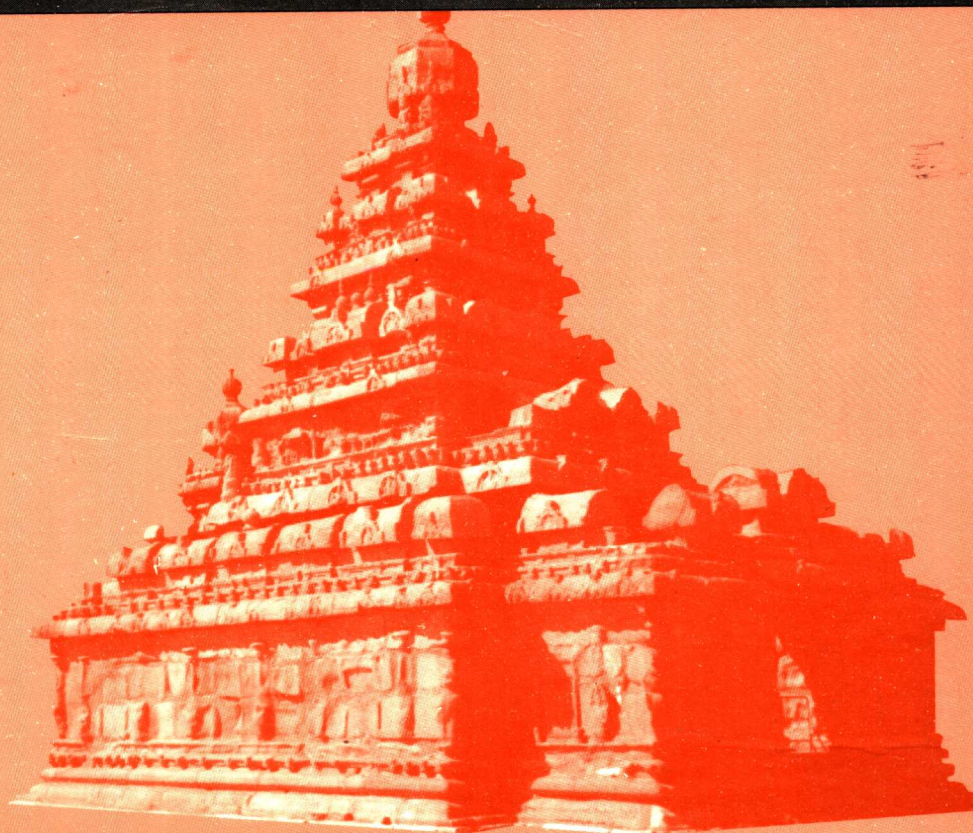
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Proceedings

# **Eleventh International Conference on VLSI Design**

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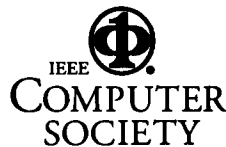
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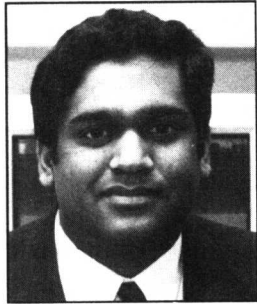
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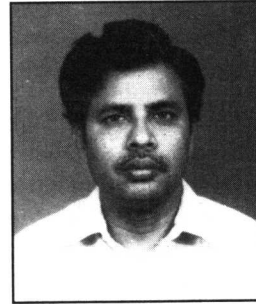
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## Program Chairs' Message



A. Chandrakasan



S. Srinivasan

Welcome to the Eleventh International Conference on VLSI Design (VLSI Design '98). This year, as in previous years, we have an exciting technical program that includes a combination of invited papers, contributed papers, panel, embedded tutorials, and regular tutorials.

Leading this year's technical program are a keynote talk and five invited plenary talks. The keynote will address future opportunities in DSP for the "networked society". Plenary presentations cover important and emerging areas such as wireless computing, low-power design, reconfigurable computing, signal processing, and system design.

We received a total of 123 contributed paper submissions (72 to the U.S. Program Chair and 51 to the Indian Program Chair). From this, we have selected 57 papers for regular presentations and 30 for short presentations. The submitted papers were reviewed by members of the Program Committee as well as external experts in different areas. Each paper submitted to the U.S. chair was sent to six reviewers and each paper received six reviews. Each paper submitted to the Indian chair was sent to five reviewers and on average, four reviewers responded. In addition, each submitted paper was cross reviewed. That is, a paper submitted to the U.S. chair was sent to a reviewer in India and vice-versa. All papers submitted in India received reviews in the U.S. whereas 77% of the papers submitted in the U.S. received reviews in India. We would like to thank the program committee members and reviewers for the outstanding job of reviewing the papers in a short period of time.

A rank ordered list consisting of papers submitted to both Program Chairs was used in the selection of papers for the technical program. The program committee meeting was first held in India at IIT Madras, and then in the U.S. at Rutgers University. The rank ordered list provided a first cut on the program, but each accepted and rejected paper was discussed in detail and the comments from all reviewers were considered.

In addition to these papers, we have six invited embedded tutorials. Each tutorial will be the first paper in the respective session and will provide a critical overview of specific areas relevant to that session. These tutorials will help the participants understand the material in the sessions.

A panel session on the second day will address some of the key considerations for future systems-on-chip. This will include design methodologies, testing and CAD tools for a variety of domains such as DSP, processor design, and mixed-signal design. It should be a stimulating event of interest to all attendees.

The final two days of the program are dedicated to six full-day tutorials. These tutorials are given by experts in the field and are meant for someone entering a field. Tutorials at the Conference have been a valuable educational experience for participants in the past. Yervant Zorian, the Tutorials Chair, received a large

number of proposals. Inputs from the program committee members both in India and abroad were used in making the selection.

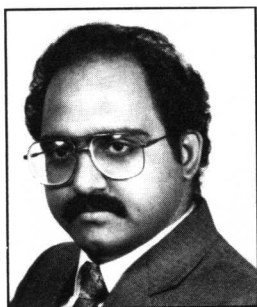
This year, nine contributed papers are being considered for the best paper award and best student paper award. Two honorable mention awards will also be given. Mike Bushnell from Rutgers University is the chair of the Awards Committee and has formed an international committee of experts to evaluate these papers. We thank him for coordinating this effort.

We acknowledge the assistance provided by several people in the preparation of the technical program. From MIT, several graduate students including Seong Hwan Cho, James Goodman, Debashis Saha, and Thucydides Xanthopoulos helped in all aspects of constructing the technical program. Special thanks to Elizabeth Chung from MIT for entering the papers submitted to the U.S. chair into the database and providing general administrative support. At IIT Madras, graduate students S. Venkatesh, C.F. Prince, B. Srikanth and Rajesh Rajaram helped in all aspects of the work of the Program Chair. H. Renganathan, M. Sathyabama, P. Anand, R. Sumathy and A. Jayakumar of IIT Madras provided excellent administrative support. We would like to thank Mircea Stan from University of Virginia and Raju Venkataramana of University of South Florida for their assistance with the conference WEB page. We thank Mike Bushnell for the facilities at Rutgers University. We would like to thank Vishwani Agrawal, the Steering Committee Chair, for his valuable suggestions and help with all aspects of the program construction. We are grateful for the guidance and support from the General Chairs, N. Ranganathan and N. Venkateswaran. The production of this proceedings was coordinated by Srimat Chakradhar, the Publications Chair, Regina Spencer Sipple and Ian Torwick of the IEEE Computer Society Press.

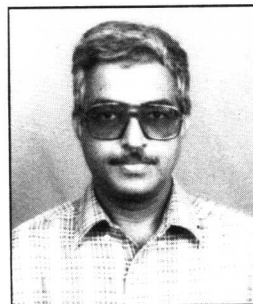
A. Chandrakasan  
Massachusetts Institute of Technology

S. Srinivasan  
Indian Institute of Technology

## General Chairs' Message



N. Ranganathan



N. Venkateswaran

The increasing demands of high speed, throughput and overall performance in modern computing applications such as multimedia, wireless communication, HDTV, video and teleconferencing necessitate the need for high performance signal processing. Microelectronics has made possible the siliconization of high performance computer systems thus becoming a major focus of attention for university, industry and government throughout the world. The International Conference on VLSI Design provides a forum for exchange of ideas related to the various aspects of VLSI design through technical papers, posters, tutorials, panel discussion and exhibits.

Welcome to VLSI Design 1998, the eleventh in a series of annual meetings held in India. The first meeting was held at IIT-Madras (Chennai) during 1985. It was organized as a workshop at a small scale. With each year, the meeting has grown steadily and has developed into a major international conference attracting researchers, scientists and engineers around the globe for presenting their research works. The conference is sponsored by the VLSI Society of India and Department of Electronics (Government of India) in cooperation with the ACM, SIGDA, IEEE Circuits and Systems Society and IEEE Computer Society's technical committees, DATC and VLSI-TC. The proceedings of VLSI Design '98 are published by the IEEE Computer Society Press.

The theme of this year's conference is *VLSI for Signal Processing* and a strong technical program has been assembled by the program co-chairs A. Chandrakasan and S. Srinivasan. The technical sessions cover a wide range of topics related to the theme of the conference and includes several invited talks and tutorials. We would like to acknowledge the efforts of the tutorial chair, Y. Zorian for the selection of the six tutorials to be given by leading experts in the various topics. The proceedings chair, S.T. Chakradhar has played a crucial role in the publication of this proceedings. The publicity chairs S. Basu, V. Krishna, B. Courtois and T. Yanagawa deserve commendations for their extensive efforts. The design contest is coordinated by M. Sambhandam, the exhibits coordinated by R. Vijayarajeswaran and the finance handled by A. Krishnan. We would like to acknowledge the efforts of R. Venkataramana, P.S. Ranganathan and M. Stan for their help with the web pages for the conference. Thanks to many students from Sri Venkateswara College of Engineering and the University of South Florida for helping us with several stages of the organization of the conference. A special mention is to be made about Vijay Krishnan, G. Chandramouli, Niranjan Prabhu and Alladi Venkateswaran.

The conference steering committee has been awarding fellowships to students and professors from the various Indian universities to enable them to attend the conference. A fellowship recipient receives financial support to cover conference and tutorial registrations, travel and lodging expenses. The fellowship program is an important program initiated by V.D. Agrawal and this year's effort is coordinated by D.R. Seetharaman. We would like to thank J.A. Chowdary and Parameswaran of VSNL for providing email

accounts and internet access at the conference. Also, we acknowledge the services of S. Seth, ACM Liaison, Y.K. Malaiya, IEEE Liaison, and A. Prabhakar, VSI Liaison.

The success of an international conference of this magnitude depends a lot on the organizing committee and a number of volunteers not mentioned here by their names. We would like to express our appreciation to them. Also, we record our sincere gratitude to V.D. Agrawal, the steering committee chair without whose leadership and guidance this event would not have been successful. He has led this conference through the years since its inception.

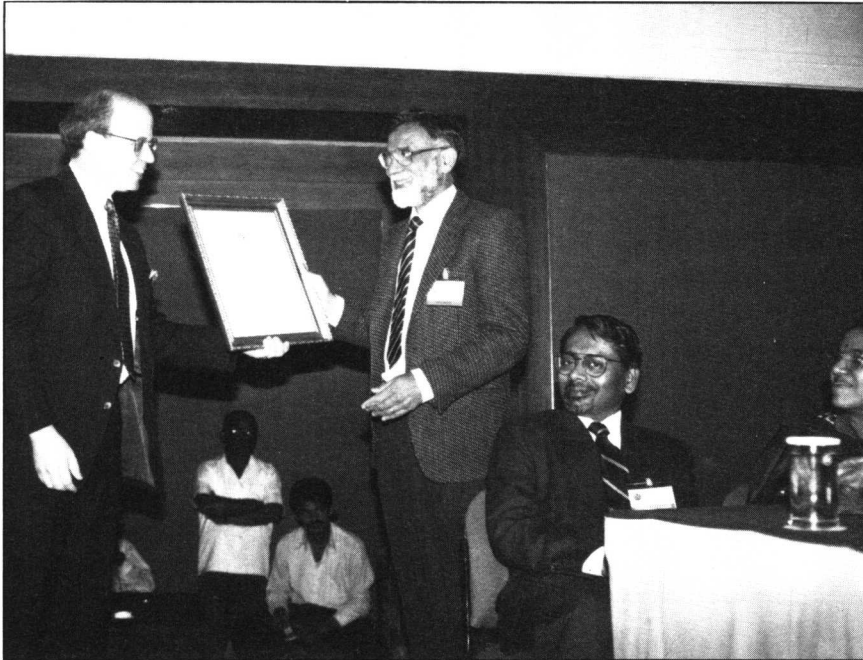
Finally, we would like to thank all referees, authors, participants, sponsors and the members of various committees for making this conference a success. On behalf of the steering committee and the conference committee, we welcome you to Chennai and to VLSI Design '98!

N. Ranganathan  
University of South Florida

N. Venkateswaran  
University of Madras

## 1997 IEEE Fellow Award

We are honored that the following individual decided to receive his IEEE Fellow Award during the 10th International Conference on VLSI Design, 1997.



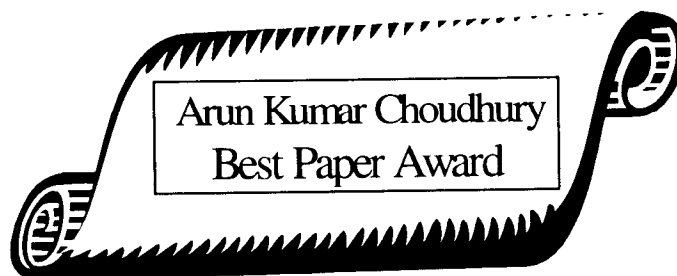
Professor Sharad Seth (right) of the University of Nebraska-Lincoln receiving his 1997 IEEE Fellow Certificate from Walden Rhines (left), President and CEO of Mentor Graphics, at the 10th International Conference on VLSI Design, 1997.

**Citation:**

For contributions to testing of digital electronic circuits.



## 1997 Conference Awards



The following two winning papers shared the cash award of  
Rs. 12,000 (about US\$400.00):

***A Hierarchical Technique for Minimum-Width Layout of Two-Dimensional CMOS Cells***

**A. Gupta**, Intel Corporation, Santa Clara, CA

**J.P. Hayes**, University of Michigan, Ann Arbor, MI

***FAMAS: Fault Modeling via Adaptive Simulation***

**H. Jin, R.K. Iyer, M.C. Hsueh**, University of Illinois, Urbana-Champaign, IL

### **Honorable Mention Award**

***Delay-Insensitive Carry-Lookahead Adders***

**F.-C. Cheng, S.H. Unger, and M. Theobald**, Columbia University, New York, NY

### **Best Student Paper Award**

***A New Methodology for the Design of Asynchronous Digital Circuits***

**K. Nanda, S.K. Desai, S.K. Roy**, Indian Institute of Technology, Kanpur, India

### **Design Contest Award**

**GF(2<sup>8</sup>) Finite Field Calculator**

**T. Rajani**, Signion Systems Pvt. Ltd., Hyderabad, India

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