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TABLE OF CONTENTS

PLENARY SESSION 1

Monday, December 12, 9:00 a.m.
Continental Ballroom

Invited Papers

Chairman: Rick Sivan, Motorola

1.1 **Bioelectronics, Three-Dimensional Memories and Hybrid Computers**, R. Birge, D. Govender, R. Gross, A. Lawrence, J. Stuart, J. Tallent, E. Tan and B. Vought, *Syracuse University, Syracuse, N.Y.* 3

1.2 **Future DRAM Development and Possibility of Ferroelectric Memories,** Y. Tarui, *Waseda University, Tokyo, Japan* 7

1.3 **Multimedia Markets: The Stakes and the Players,** T. Swanenburg, *Philips Corporate Research, Eindhoven, The Netherlands* 17

Session 2: Vacuum Electronics—Vacuum Microelectronics and Ferroelectric Cathode 21

Monday, December 12, 1:30 p.m.
Continental Ballroom 1-3

Co-Chairmen: Tayo Akinwande, Honeywell Technology Center
John Pasour, Mission Research Corporation

1:30 p.m.
Introduction

1:35 p.m.
2.1 **New Structure Si Field Emitter Arrays with Low Operation Voltage,** K. Koga, K. Morimoto and Y. Hori, *Matsushita Electric Industrial Co., Ltd., Osaka, Japan,* S. Kanemaru and J. Itoh, *Electrotechnical Laboratory, Ibaraki, Japan* 23

2:00 p.m.
2.2 **Field Emission Diodes Using Sharp Vertical Edge Structure,** S. Zurn, P. Schiller, D. Glumac, Q. Mei and D. Polla, *University of Minnesota, Minneapolis, MN* 27

2:25 p.m.
2.3 **A New Cathode for Vacuum Microelectronic Devices: Silicon Tip Avalanche Cathode,** S. Jo, S. Kwon* and J. Lee, *Seoul National University, Seoul, Korea and * Kyungwon University, Kyunggi-do, Korea* 31

2:50 p.m.
2.4 **Experimental Studies of the Ferroelectric Cathode,** B. Jang, G. Kirkman, I. Yampolsky and N. Reinhardt, *Integrated Applied Physics, Inc., Torrance, CA* †

3:15 p.m.
2.5 **Investigation of Electron Emission from Bulk (Pb,La)(Zr,Ti)O_3 Ferroelectric Ceramics,** T. Cavazos, W. Wilbanks, C. Fleddermann and D. Shiffler, *University of New Mexico, Albuquerque, NM* 35

3:40 p.m.
2.6 **Electron Emission from Ferroelectric Crystals and Thin Ceramics,** D. Averty, S. Lanteri and D. Le Bihan, *Universite de Nantes, Nantes, France*

SESSION 3: Integrated Circuits — FMT-Flash Memory Technology 39

Monday, December 12, 1:30 p.m.
Continental Ballroom 4

Co-Chairmen: Joel Hartmann, LETI
Kuniyoshi Yoshikawa, Toshiba

1:30 p.m.
Introduction

1:35 p.m.
3.1 **A Novel Band-to-Band Tunneling Induced Convergence Mechanism for Low Current, High Density Flash EEPROM Applications (Invited Paper),** D. Shum, C. Swift, J. Higman, W. Taylor, K.T. Chang, K.M. Chang and J. Yeargain, *Motorola, Austin, TX* 41

2:00 p.m.
3.2 **Read-Disturb Degradation Mechanism due to Electron Trapping in the Tunnel Oxide for Low-Voltage Flash Memories,** M. Kato, N. Miyamoto*, H. Kume, A. Satoh, T. Adachi, M. Ushiyama and K. Kimura, *Hitachi, Ltd., Tokyo, Japan and *Chiba, Japan* 45

2:25 p.m.
3.3 **A New Write/Erase Method for the Reduction of the Stress-Induced Leakage Current Based on the Deactivation of Step Tunneling Sites for Flash Memories,** T. Endoh, K. Shimizu, H. Iizuka, S. Watanabe and F. Masuoka, *Toshiba R & D Center, Kawasaki, Japan* 49

2:50 p.m.
3.4 **New Erase Scheme for DINOR Flash Memory Enhancing Erase/Write Cycling Endurance Characteristics,** N. Tsuji, N. Ajika, K. Yuzuriha, Y. Kunori, M. Hatanaka and M. Miyoshi, *Mitsubishi Electric Corporation, Itami, Japan* 53

3:15 p.m.
3.5 **A Dual-bit Split-Gate EEPROM (DSG) Cell in Contactless Array for Single-Vcc High Density Flash Memories,** Y. Ma, C. Pang, K. Chang, S. Tsao, J. Pathak and J. Frayer, Bright Microelectronics, Santa Clara, CA and T. Kim, K. Jo, J. Kim, I. Choi, and H. Park, *Hyundai Electronics Industries, Ichon-Kun, Korea* 57

3:40 p.m.
3.6 **A 0.67μm^2 Self-Aligned Shallow Trench Isolation Cell (SA-STI Cell) for 3V-Only 256Mbit NAND EEPROMs,** S. Aritome, S. Satoh, T. Maruyama, H. Watanabe, S. Shuto, G. Hemink, R. Shirota, S. Watanabe and F. Masuoka, *Toshiba R&D Center, Kawasaki, Japan* 61

SESSION 4: CMOS Devices and Reliability — Advanced CMOS Device Optimization 65

Monday, December 12, 1:30 p.m.
Continental Ballroom 5

Co-Chairmen: Martin Manley, National Semiconductor
Hee-Gook Lee, Goldstar Electron Co.

1:30 p.m.
Introduction

1:35 p.m.
4.1 **0.15μm CMOS Process for High Performance and High Reliability,** S. Shimizu, S. Kusunoki, M. Kobayashi, T. Yamaguchi, T. Kuroi, T. Fujino, H. Maeda, T. Tsutsumi, Y. Hirose, M. Inuishi and N. Tsubouchi, *Mitsubishi Electric Corporation, Hyogo, Japan* 67

2:00 p.m.
4.2 **A Study of Design/Process Dependence of 0.25μm Gate Length CMOS for Improved Performance and Reliability,** M. Rodder, A. Amerasekera, S. Aur and I. Chen, Texas Instruments, Dallas, TX 71

2:25 p.m.
4.3 **A 0.1μm CMOS Technology with Tilt-Implanted Punch-through Stoppers (TIPS),** T. Hori, *Matsushita Elec. Ind. Co., Ltd., Kyoto, Japan* 75

2:50 p.m.
4.4 **Design Methodology for Low-Voltage MOSFETs,** T. Andoh, A. Furukawa and T. Kunio, *NEC Corporation, Kanagawa, Japan* 79

3:15 p.m.
4.5 **FOND (Fully Overlapped Nitride-etch Defined Device): A New Device Architecture for High-Reliability and High-Performance Deep Submicron CMOS Technology,** J.-P. Mieville, G. Van den bosch, L. Deferm, R. Bellens, G. Groeseneken, H. Maes and W. Schoenmaker, *IMEC, Leuven, Belgium* 83

3:40 p.m.
4.6 **Pass Transistor Designs Using Pocket Implant to Improve Manufacturability for 256Mbit DRAM and Beyond,** A. Chatterjee, J. Liu, S. Aur, P. Mozumder, M. Rodder and I. Chen, *Texas Instruments, Dallas, TX* 87

4:05 p.m.
4.7 **Submicron Large-Angle-Tilt Implanted Drain Technology for Mixed-Signal Applications,** H. Chen, J. Zhao, C. Teng, L. Moberly and R. Lahri, *National Semiconductor Corp., Santa Clara, CA* 91

SESSION 5: Device Technology — Advanced Multilevel Interconnect Technologies 95

Monday, December 12, 1:30 p.m.
Continental Ballroom 6

Co-Chairmen: Mehrdad Moslehi, CVC Products
Shyam Murarka, Rensselear Polytechnic Institute

1:30 p.m.
Introduction

1:35 p.m.
5.1 **Progression of Multilevel Metalization Beyond 0.35 Micron Technology (Invited Paper),** F. Pintchovski, *Motorola, Austin, TX* 97

2:00 p.m.
5.2 **Aluminum-Germanium-Copper Multilevel Damascene Process Using Low Temperature Reflow Sputtering and Chemical Mechanical Polishing,** K. Kikuta, Y. Hayashi, T. Nakajima, K. Harashima and T. Kikkawa, *NEC Corp., Kanagawa, Japan* 101

2:25 p.m.
5.3 **A Novel High Pressure Low Temperature Aluminum Plug Technology for Sub-0.5μm Contact/Via Geometries,** G. Dixit, M. Chisholm, M. Jain, T. Weaver, L. Ting, S. Poarch, K. Mizobuchi*, R. Havemann, C. Dobson**, A. Jeffreys**, P. Holverson**, P. Rich**, D. Butler**, and J. Hems**, *Texas Instruments, Dallas, TX, and *Miho, Japan, and ** Thornbury Laboratories, Bristol, UK* 105

2:50 p.m.
5.4 **A Novel Al-Reflow Process Using Surface Modification by the ECR Plasma Treatment and Its Application to the 256 Mbit DRAM,** I. Park, Y. Wee, W. Jung, G. Choi, C. Park, S. Park, S. Lee, S. Ahn and M. Lee, *Samsung Electronics Co., Ltd., Kyungki-do, Korea and* Y. Kim and R. Reynolds, *Varian, Palo Alto, CA* 109

3:15 p.m.
5.5 **Discussion Session**

3:40 p.m.
5.6 **New Contact Process Using Soft Etch for Stable Ohmic Characteristics and its Application to 0.1μm CMOS Devices,** H. Sumi, T. Yanagida and Y. Sugano, *Sony Corp., Kanagawa, Japan and* J. Sasserath, *Materials Research Corp., Orangeburg, NY* 113

4:05 p.m.
5.7 **Novel Self-Planarizing CVD Oxide for Interlayer Dielectric Applications,** M. Matsuura, Y. Hayashide, H. Kotani, T. Nishimura*, H. Iuchi*, C. Dobson**, A. Kiermasz**, K. Beekmann** and R. Wilby**, *Mitsubishi, Hyogo, Japan and *Ryoden Semi. Eng. Corp., Hyogo, Japan and **Electrotech Int'l Ltd., Bristol, United Kingdom* 117

4:30 p.m.
5.8 **Interconnection Scheme for Improved High Speed ICs,** A. Plettner, K. Haberger, A. Englmaier, K. Neumeier, and H. Hartmann, *Fraunhofer Institute for Solid State Technology, Munich, Germany* 121

SESSION 6: Detectors, Sensors and Displays — Micromachined and Magnetic Sensors 125

Monday, December 12, 1:30 p.m.
Continental Ballroom 7-9

Co-Chairmen: Denice Denton, University of Wisconsin
Arokia Nathan, University of Waterloo

1:30 p.m.
Introduction

1:35 p.m.
6.1 **Micromachined Sensors Using Polysilicon Sacrificial Layer Etching Technology (Invited Paper),** S. Sugiyama, O. Tabata, K. Shimaoka and R. Asahi, *Toyota Central R&D Laboratories, Inc., Aichi-ken, Japan* 127

2:00 p.m.
6.2 **Novel Integrated Thermal Pressure Gauge and Read-out Circuit by CMOS IC Technology,** O. Paul, A. Haberli, P. Malcovati and H. Baltes, *ETH Hoenggerberg, Zurich, Switzerland* 131

2:25 p.m.
6.3 **An Integrated CMOS Polysilicon Coil-Based Micro-Pirani Gauge with High Heat Transfer Efficiency,** N. Swart and A. Nathan, *University of Waterloo, Waterloo, Ontario, Canada* 135

2:50 p.m.
6.4 **Theoretical and Experimental Studies of a Micromachined Hot-Wire Anemometer,** F. Jiang and Y. Tai, Caltech, Pasadena, CA and C. Ho, *UCLA, Los Angeles, CA* 139

3:15 p.m.
6.5 **A Highly-Sensitive and Low Power SOI Lateral Thyristive Magnetometer,** J. Lau, C. Nguyen, P. Ko and P. Chan, *The Hong Kong University of Science and Technology, Hong Kong* 143

3:40 p.m.
6.6 **Magnetotransistors in SOI Technology,** R. Castagnetti, C. Riccobene, M. Schneider, G. Wachutka* and H. Baltes, *ETH Zurich, Zurich, Switzerland and * Technische Universitat Munchen, Munich, Germany* 147

SESSION 7: Modeling and Simulation — Compact Modeling of MOSFETs 151

Monday, December 12, 1:30 p.m.
Imperial Ballroom A

Co-Chairmen: Mohamed Darwish, Siliconix, Inc.
Zhiping Yu, Stanford University

1:30 p.m.
Introduction

1:35 p.m.
7.1 TCAD Strategy for Predictive VLSI Memory Development, H. Masuda, H. Sato, K. Tsuneno, K. Aoyama, T. Nakamura, H. Kunitomo, and K. Kajigaya, *Hitachi, Tokyo, Japan* 153

2:00 p.m.
7.2 An EEPROM Model for Low Power Circuit Design and Simulation, T. Yu, J. Higman, C. Cavins, K. Chang and M. Orlowski, *Motorola, Austin, TX* 157

2:25 p.m.
7.3 Interface Trap Induced Thermionic and Field Emission Current in Off-State MOSFETs, T. Wang, T. Chang and C. Huang, *National Chaio-Tung University, Taiwan, Rep. of China* 161

2:50 p.m.
7.4 A New Analog/Digital CAD Model for Sub-Halfmicron MOSFETs, T. Skotnicki, C. Denat, P. Senn, G. Merckel and B. Hennion, *CNET-CNS, Meylan, France* 165

3:15 p.m.
7.5 A Relaxation Time Approach to Model the Non-Quasi-Static Transient Effects in MOSFETs, M. Chan, K. Hui, R. Neff, C. Hu and P. Ko, *University of California, Berkeley, CA* 169

3:40 p.m.
7.6 The High-Frequency Analogue Performance of MOSFETs, R. Vanoppen, J. Geelen and D. Klaassen, *Philips Research Laboratories, Eindhoven, The Netherlands* 173

4:05 p.m.
7.7 Model for 1/f Noise in MOSFETs and Interconnects, D. Wolters, A. Zegers-van Duijnhoven and R. Augur, *Philips Research Laboratories, Eindhoven, The Netherlands* 177

SESSION 8: Quantum Electronics and Compound Semiconductor Devices — Heterojunction Bipolar Transistors 181

Monday, December 12, 1:30 p.m.
Imperial Ballroom B

Co-Chairmen: Chuck Weitzel, Motorola, Inc.
Yi-Ching Pao, Litton Solid State

1:30 p.m.
Introduction

1:35 p.m.
8.1 Aluminum Graded-Base AlGaAs/GaAs PNp HBT with 37GHz Cut-Off Frequency, A. Kameyama, and A. Massengale, C. Dai, and J. Harris, Jr., *Stanford University, Stanford, CA* 183

2:00 p.m.
8.2 Characterization of Bias-Stressed Carbon-Doped GaAs/AlGaAs Power Heterojunction Bipolar Transistors, T. Henderson, D. Hill, W. Liu, D. Costa, H. Chau, T. Kim and A. Khatibzadeh, *Texas Instruments, Dallas, TX* 187

2:25 p.m.
8.3 High-Reliability InGaP/GaAs HBTs Fabricated by Self-Aligned Process, T. Takahashi, S. Sasa, A. Kawano, T. Iwai and T. Fujii, *Fujitsu Laboratories, Ltd., Atsugi, Japan* 191

2:50 p.m.
8.4 3.5V, 1W High Efficiency AlGaAs/GaAs HBTs with Collector Launcher Structure, Y. Tateno, H. Yamada, S. Ohara, S. Kato, H. Ohnishi, T. Fujii and J. Fukaya, *Fujitsu, Ltd., Kawasaki, Japan* 195

3:15 p.m.
8.5 Microwave/Millimeter-Wave Power HBTs with Regrown Extrinsic Base Layers, Y. Amamiya, C.W. Kim, N. Goto, S. Tanaka, N. Furuhata, H. Shimawaki and K. Honjo, *NEC Corp., Ibaraki, Japan* 199

3:40 p.m.
8.6 E-Beam Re-Aligned HBTs and a New Broadband MMIC Power Amplifier Using Bathtub as Heat Sink, L. Yang, J. Komiak, M. Kao, D. Houston, D. Smith and K. Norheden *Martin Marietta Laboratories, Syracuse, NY* 203

SOFTWARE SHOWCASE 207

Tuesday, December 13, 9:00 a.m.–5:00 p.m.
Franciscan Rooms B&C

Software Showcase Presentations:

Layout-Based Extraction of IC Electrical Behavior, K. Wang, F. Rotella, T. Chen, D. Yang, A. Lee, Z. Yu, R. Knepper, J. Watt, and R. Dutton, *Stanford University, Stanford, CA* 209

Next-Generation Stanford TCAD-PISCES 2ET and SUPREM 007, S. Beebe, F. Rotella, Z. Sahul, D. Yergeau, G. McKenna, L. So, Z. Yu, K. Wu, E. Kan, J. McVittie and R. Dutton, *Stanford University, Stanford, CA* 213

mcplotgl: Graphics for the DAMOCLES Program, S. Laux and M. Fischetti, *T.J. Watson Research Center, IBM Research Division, Yorktown Heights, NY* 217

MOS Device Reliability Studies Under a LabVIEW Environment, M. Martin, R. Paulsen, and M. White, *Sherman Fairchild Center for Solid State Studies, Lehigh University, Bethlehem, PA* 221

VIDS: Visual Interpretation for Device Simulations, E. Farrell, *Scientific Visualization Systems, IBM Research Center, Hawthorne, NY* 225

Circuit Simulation of Resonant Tunneling Devices Using NDR-SPICE, S. Mohan, P. Mazumder and G. Haddad, *University of MIchigan, Ann Arbor, MI* 229

Visualization of Ionizing Radiation and Hot-Carrier Stress Response of Polysilicon Emitter BJT's, D. Schmidt, R. Graves, S. Kosier, A. Wei, R.Schrimpf and K. Galloway, *University of Arizona, Tuscon, AZ* 233

SESSION 9: Vacuum Electronics — Fast Wave Devices 237

Tuesday, December 13, 9:00 a.m.
Continental Ballroom 1-3

Co-Chairmen: Ken Kreischer, Massachusetts Institute of Technology
Wes Lawson, University of Maryland

9:00 a.m.
Introduction

9:05 a.m.
9.1 Development of a High Power and Long Pulse Gyrotron with Collector Potential Depression, A. Kasugai, K. Sakamoto, M. Tsuneoka, K. Takahashi, S. Maebara, T. Imai, T. Kariya*, Y. Okazaki*, K. Hayashi**, Y. Mitsunaka** and Y. Hirata**, *Japan Atomic Energy Res. Inst., Ibaraki-ken, Japan, *Toshiba, Tochigi-ken, **Toshiba, Kawasaki-shi, Japan* 239

9:30 a.m.
9.2 Operation of a Megawatt 110 GHz Gyrotron with an Internal Mode Converter, K. Kreischer, M. Blank, B. Danly, T. Kimura and R. Temkin, *Massachusetts Institute of Technology, Cambridge, MA* 243

9:55 a.m.
9.3 Theoretical and Experimental Investigation of Gyrotron Amplifiers for Collider Applications, W. Lawson, J. Calame, J. Cheng, M. Castle, P. Latham, B. Hogan, V. Granatstein and M. Reiser, *University of Maryland, College Park, MD* 247

10:20 a.m.
9.4 Beamstick for a 95 GHz Harmonic Gyroklystron, T. Bemis, G. Scheitrum, T. Hargreaves and L. Higgins, *Litton Electron Devices, San Carlos, CA* 251

10:45 a.m.
9.5 Operational Two-Stage Tapered Gyro-TWT Amplifier, G.Park*, J.Choi, *SAIC, McLean, VA,* S.Park, *Pohang Inst.Sci.&Tech., Pohang, Korea,* C.Armstrong, *Northrop Corp., Rolling Meadow, IL,* A.Ganguly*, K.Nguyen, *KN Res., Silver Spring, MD,* R.Kyser, *B-K Sytems, Rockville, MD,* R.Parker, *NRL, Wash. DC, *Omega-P, Inc., New Haven, CT* 255

11:10 a.m.
9.6 Experimental Study of Quasi-Optical Mode Converters for High Order Mode Gyrotrons, M. Blank, K. Kreischer and R. Temkin, *MIT Plasma Fusion Center, Cambridge, MA* 259

11:35 a.m.
9.7 Theoretical Investigation of Axially-Modulated, Cusp-Injected Large-Orbit Gyrotrons, W. Lawson and W. Destler, *University of Maryland, College Park, MD* 263

SESSION 10: *Integrated Circuits* — *Microprocessor and Programmable Logic Technologies* 267

Tuesday, December 13, 9:00 a.m.
Continental Ballroom 4

Co-Chairmen: Lal Sood, Motorola
Luan Tran, Micron

9:00 a.m.
Introduction

9:05 a.m.
10.1 Microprocessor Technology Trends (Invited Paper), T. Fletcher, *Intel Corporation, Hillsboro, OR* 269

9:30 a.m.
10.2 A High Performance 0.35μm Logic Technology for 3.3V and 2.5V Operation, M. Bohr, S. Ahmed, L. Brigham, R. Chau, W. Hargrove, R. Gasser, R. Green, E. Lee, R. Natter, S. Thompson, K. Weldon and S. Yang, *Intel Corp., Hillsboro, OR* 273

9:55 a.m.
10.3 Mixed-Voltage-Interface ESD Protection Circuits for Advanced Microprocessors in Shallow Trench and LOCOS Isolation CMOS Technologies, S. Voldman, *IBM, Essex Junction, VT* **and** G. Gerosa, *Motorola, Inc., Austin, TX* 277

10:20 a.m.
10.4 Reliable Metal-to-Metal Oxide Antifuse, G. Zhang, C. Hu and P. Yu, *University of California, Berkeley, CA* and S. Chiang, S. Eltoukhy and E. Hamdy, *Actel Corp., Sunnyvale, CA* 281

10:45 a.m.
10.5 Most Promising Metal-to-Metal Antifuse Based 10nm-thick p-SiNx Film for High Density and High Speed FPGA Application, Y. Tamura and H. Shinriki, *Kawasaki Steel Corporation, Chiba, Japan* 285

SESSION 11: CMOS Devices and Reliability — Hot-Carrier Reliability in Flash EPROM and CMOS 289

Tuesday, December 13, 9:00 a.m.
Continental Ballroom 5

Co-Chairmen: Werner Weber, Siemens
Toshiuki Tsuchiya, NTT

9:00 a.m.
Introduction

9:05 a.m.
11.1 Failure Mechanisms of Flash Cell in Program/Erase Cycling (Invited Paper), P. Cappelletti, R. Bez, D. Cantarelli and L. Fratin, *SGS-Thomson Microelectronics, Milan, Italy* 291

9:30 a.m.
11.2 Flash EPROM Endurance Simulation Using Physics-Based Models, J. Peng, S. Haddad, H. Fang, C. Chang, S. Longcor, D. Liu, Y. Tang, B. Ho, Y. Sun, J. Hsu, S. Luan, and J. Lien, *Advanced Micro Devices, Sunnyvale, CA* 295

9:55 a.m.
11.3 High-Frequency AC Hot-Carrier Degradation in CMOS Circuits, V. Chan, T. Kopley*, P. Marcoux* and J. Chung, *MIT, Cambridge, MA and * Hewlett-Packard Company, Palo Alto, CA* 299

10:20 a.m.
11.4 Charcterization and Model of the Hot-Carrier-Induced Offset Voltage of Analog CMOS Differential Stages, R. Thewes, K. Goser* and W. Weber, *Siemens AG, Munich, Germany and *Universitat Dortmund, Dortmund, Germany* 303

10:45 a.m.
11.5 Bias and Temperature Dependence of Gate and Substrate Currents in n-MOSFETs at Low Drain Voltage, D. Esseni, L. Selmi, R. Bez*, E. Sangiorgi** and B. Ricco, *University of Bologna, Bologna, Italy and * SGS-Thomson Microelectronics, Brianza, Italy and ** University of Udine, Udine, Italy* 307

11:10 a.m.
11.6 Hot-Hole-Induced Negative Oxide Charges in n-MOSFETs, W. Weber, M. Brox and R. Thewes, *Siemens Corporate R&D, Munich, Germany* and N. Saks, *Naval Research Laboratory, Washington, DC* 311

11:35 a.m.
11.7 Full Analysis of Alternating Injection in SOI Transistors: Comparison to Bulk Transistors, E. Guichard, S. Cristoloveanu*, G. Reimbold and G. Borel**, *LETI, Grenoble Cedex, France and *LPCS ENSERG, Grenoble Cedex, France and **Thomson TCS, Saint-Egreve, France* 315

SESSION 12: Device Technology — Advanced Gate Dielectrics 319

Tuesday, December 13, 9:00 a.m.
Continental Ballroom 6

Co-Chairmen: S.C. Sun, National Chiao Tung University
John Lowell, AMD

9:00 a.m.
Introduction

9:05 a.m.
12.1 *Improvement of Thin Oxide Quality by Hydrogen Annealed Wafer (Invited Paper),* Y. Matsushita, S. Samata, M. Miyashita and H. Kubota, *Toshiba Corp., Kawasaki, Japan* 321

9:30 a.m.
12.2 Impact of Boron Diffusion Through O_2 and N_2O Gate Dielectrics on the Process Margin of Dual-Poly Low Power CMOS, K. Krisch, L. Manchanda*, F. Baumann*, M. Green, D. Brasen, L. Feldman and A. Ourmazd*, *AT&T Bell Laboratories, Murray Hill, NJ and *Holmdel, NJ* 325

9:55 a.m.
12.3 Performance and Hot-Carrier Reliability of N- and P-MOSFETs with Rapid Thermally NO-Nitrated SiO_2 Gate Dielectrics, M. Bhat, D. Wristers, J. Yan, L. K. Han, D. Kwong and J. Fulford*, *University of Texas, Austin, TX and *Advanced Micro Devices, Austin, TX* 329

10:20 a.m.
12.4 A Novel Approach for Leakage Current Reduction of LPCVD Ta_2O_5 and TiO_2 Films by Rapid Thermal N_2O Annealing, S. Sun and T. Chen, *Chiao Tung University, Taiwan, Rep. of China* 333

10:45 a.m.
12.5 Impact of Post Processing Damages on the Performance of High Dielectric Constant PLZT Thin Film Capacitors for ULSI DRAM Applications, R. Khamankar, J. Kim, B. Jiang, C. Sudhama*, P. Maniar**, R. Moazzami**, R. Jones**, and J. Lee, *University of Texas, Austin, TX, and * Motorola, Mesa, AZ, and ** Motorola, Austin, TX* 337

SESSION 13: Emerging Technology Session 341

Tuesday, December 13, 9:00 a.m.
Continental Ballroom 7-9

Chairman: Martin Schmidt, Massachusetts Institute of Technology

9:00 a.m.
Introduction

9:05 a.m.
13.1 Micromechanical Resonators for Frequency References and Signal Processing, R.T. Howe and C.T.-C. Nguyen, *Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA* 343

9:55 a.m.
13.2 Grating Light Valves for High Resolution Displays, D.M. Bloom, *Edward L. Ginzton Laboratory, Stanford University, Stanford, CA* 343

10:45 a.m.
13.3 Erbium Doped Silicon Light Emitters, J. Michel and L. Kimerling, *Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, MA* 344

SESSION 14: Modeling and Simulation — Electronic Transport Modeling in Submicron Devices 345

Tuesday, December 13, 9:00 a.m.
Imperial Ballroom A

Co-Chairmen: Isik Kizilyalli, AT&T Bell Labs
Luca Selmi, University of Bologna

9:00 a.m.
Introduction

9:05 a.m.
14.1 Application of Semiclassical Device Simulation to Trade-Off Studies for Sub-0.1μm MOSFETs (Invited Paper), C. Fiegna, H. Iwai*, M. Saito* and E. Sangiorgi**, *University of Ferrara, Ferrara, Italy and *Toshiba Co., Kawasaki, Japan and **University of Udine, Udine, Italy* 347

9:30 a.m.
14.2 Novel Transport Simulation of Vertically-Grown MOSFETs by Cellular Automaton Method, A. Rein, G. Zandler, M. Saraniti, P. Lugli and P. Vogl, Technical University of Munich, Garching, Germany 351

9:55 a.m.
14.3 Monte Carlo Study of Impact Ionization Phenomena in Small Geometry MOSFETs (Invited Paper), K. Taniguchi, M. Yamaji, K. Sonoda, T. Kunikiyo and C. Hamaguchi, *Osaka University, Osaka, Japan* 355

10:20 a.m.
14.4 Solution of the Boltzmann Transport Equation in Two Real-Space Dimensions using a Spherical Harmonic Expansion in Momentum Space, K. Rahmat, J. White and D. Antoniadis, *M.I.T., Cambridge, MA* 359

10:45 a.m.
14.5 A Combined Transport-Injection Model for Hot-Electron and Hot-Hole Injection in the Gate Oxide of MOS Structures, A. Ghetti, L. Selmi, E. Sangiorgi*, A. Abramo and F. Venturi**, *University of Bologna, Bologna, Italy, and *University of Udine, Udine, Italy and **University of Parma, Parma, Italy* 363

SESSION 15: Solid State Devices — SiGe and Novel Devices 367

Tuesday, December 13, 9:00 a.m.
Imperial Ballroom B

Co-Chairmen: Steve Mittleman, USAF Rome Laboratory
K.L. Wang, UCLA

9:00 a.m.
Introduction

9:05 a.m.
15.1 Optimized Ge Channel Profiles for VLSI Compatible Si/SiGe p-MOSFETs, S. Voinigescu and C. Salama, J. Noel* and T. Kamins**, *University of Toronto, Ontario, Canada and * National Research Council Canada, Ontario, Canada and **Hewlett-Packard Laboratories, Palo Alto, CA* 369

9:30 a.m.
15.2 Strain Dependence of the Performance Enhancement in Strained-Si N-MOSFETs, J. Welser, J. Hoyt, S. Takagi and J. Gibbons, *Stanford University, Stanford, CA* 373

9:55 a.m.
15.3 Multi Emitter Finger SiGe-HBTs with f_{max} up to 120 GHz, A. Schuppen, A. Gruhle,. U. Erben*, H. Kibbel and U. Konig, *Daimler Benz AG, Ulm Germany and *University of Ulm, Ulm, Germany* 377

10:20 a.m.
15.4 A Novel High Speed, High Density SRAM Cell Utilizing a Bistable GeSi/Si Tunnel Diode, T. Carns, X. Zheng and K. Wang, *University of California, Los Angeles, CA* 381

10:45 a.m.
15.5 Charge Injection Transistors and Logic Elements in $Si/Si_{1-x}GE_x$ Heterostructures, M. Mastrapasqua, C. King, P. Smith and M. Pinto, *AT&T Bell Laboratories, Murray Hill, NJ* 385

11:10 a.m.
15.6 High-Temperature GaN/SiC Heterojunction Bipolar Transistor with High Gain, J. Pankove, Astralux, Inc., Boulder, CO and S. Chang*, H. Lee*, R. Molnar**, T. Moustakas** and V. Van Zeghbroech*, *University of Colorado, Boulder, CO and **Boston University, Boston, MA* 389

SESSION 16: Solid State Devices — Power Devices and ICs 393

Tuesday, December 13, 2:15 p.m.
Continental Ballroom 1-3

Co-Chairmen: T. Paul Chow, Rensselaer Polytechnic Institute
Sophie Verdonckt-Vandebroek, Xerox WCRT

2:15 p.m .
Introduction

2:20 p.m.
16.1 New (Super) Self Aligned MOS Controlled Thyristors, (S)SAMCTs, Switching 20A at 4kV, H. Dettmer and W. Fichtner, *Swiss Federal Institute of Technology, Zurich, Switzerland and F. Bauer, ABB Semiconductors, Ltd., Lenzburg, Switzerland* 395

2:45 p.m.
16.2 Optimized Complementary 40V Power LDMOS-FETs Use Existing Fabrication Steps in Submicron CMOS Technology, T. Efland, T. Keller, S. Keller and J. Rodriguez, *Texas Instruments, Dallas, TX* 399

3:10 p.m.
16.3 Integration of High-Voltage NMOS Devices into a Submicron BiCMOS Process Using Simple Structural Changes, Y. Li, C. Salama, M. Seufert*, P. Schvan* and M. King*, *University of Toronto, Ontario, Canada and *Northern Telecom, Ontario, Canada* 403

3:35 p.m.
16.4 Device Integration for ESD Robustness of High Voltage Power MOSFETs, C. Duvvury, J. Rodriguez, C. Jones and M. Smayling, *Texas Instruments, Dallas, TX* 407

4:00 p.m.
16.5 Vertical Schottky Barrier Diodes on 3C-SiC Grown on Si, P. Shenoy, B. Baliga, A. Moki and D. Alok, *North Carolina State University, Raleigh, NC,* K. Wongchotigul, and M. Spencer, *Howard University, Washington, DC* 411

4:25 p.m.
16.6 Switching Characteristics of a High-Temperature 6H-SiC Thyristor, K. Xie, W. Buchwald and J. Zhao, *Rutgers University, Piscataway, NJ,* J. Flemish, T. Burke, L. Kingsley, M. Weiner and H. Singh, *US Army Research Laboratory, Fort Monmouth, NJ* 415

4:50 p.m.
16.7 Epitaxial Diamond Schottky Barrier Diode with On/Off Current Ratios in Excess of 10^7 at High Temperatures, W. Ebert, A. Vescan, T. Borst and E. Kohn, *University of Ulm, Ulm, Germany* 419

5:15 p.m.
16.8 Field-Effect Transistors and Circuits Fabricated From Semiconducting Diamond Thin Films, D. Dreifus, J. Holmes, *Kobe Steel USA Inc., Research Triangle Park, NC* 423

SESSION 17: Integrated Circuits — Specialized IC Technologies 427

Tuesday, December 13, 2:15 p.m.
Continental Ballroom 4

Co-Chairmen: Toshiro Hiramoto, University of Tokyo
Hans Stork, Hewlett-Packard

2:15 p.m.
Introduction

2:20 p.m.
17.1 Technology Trends of Silicon-On-Insulator: Its Advantages and Problems to be Solved (Invited Paper), M. Yoshimi, M. Terauchi, A. Murakoshi, M. Takahashi, K. Matsuzawa, N. Shigyo and Y. Ushiku, *Toshiba Corporation, Kawasaki, Japan* 429

2:45 p.m.
17.2 Effect of Substrate Material on Crosstalk in Mixed Analog/Digital Integrated Circuits, R. Merrill, W. Young and K. Brehmer, *National Semiconductor, Santa Clara, CA* 433

3:10 p.m.
17.3 A 200 mm SiGe-HBT Technology for Wireless and Mixed Signal Applications, D. Harame, J. Cressler*, M. Gilbert, R. Groves, G. Hueckel, S. Jeng, C. Kermarrec**, J. Malinowski, B. Meyerson, D. Nguyen-Ngoc, K. Schonenberg, T. Tice**, K. Walter, G. Berg, D. Colavito, J. Comfort, E. Crabbe, B. Cunningham, G. Fitzgibbons, N. Greco, T. Houghton, T. Kebede, K. Stein, S. Subbana and K. Tallman, *IBM, Yorktown Heights, NY and *Auburn Univ. and **Analog Devices Inc.* 437

3:35 p.m.
17.4 Process Integration Technology for sub-30ps ECL BiCMOS using Heavily Boron Doped Epitaxial Contact (HYDEC), Y. Kinoshita, K. Imai, H. Yoshida, H. Suzuki, T. Tatsumi and T. Yamazaki, *NEC Corp., Kanagawa, Japan* 441

4:00 p.m.
17.5 Josephson-CMOS Integrated Circuits, U. Ghoshal, D. Hebert and T. Van Duzer, *University of California, Berkeley, CA* 445

4:25 p.m.
17.6 Flash-Based Programmable Nonlinear Capacitor for Switched-Capacitor Implementations of Neural Networks, A. Kramer, M. Sabatini, R. Canegallo, M. Chinosi, P. Rolandi and P. Zabberoni, *SGS-Thomson Microelectronics, Milano, Italy* 449

SESSION 18: CMOS Devices and Reliability — Device Reliability and Characterization 453

Tuesday, December 13, 2:15 p.m.
Continental Ballroom 5

Co-Chairmen: Ron Schrimpf, University of Arizona
Reinout Woltjer, Philips Research Laboratories

2:15 p.m.
Introduction

2:20 p.m.
18.1 Electrothermal Behavior of Deep Submicron nMOS Transistors Under High Current Snapback (ESD/EOS) Conditions, A. Amerasekera and J. Seitchik, *Texas Instruments, Dallas, TX* 455

2:45 p.m.
18.2 Degradation of I/O Devices due to ESD-Induced Dislocations, C. Hashimoto, *Hitachi ULSI Engineering Corp., Tokyo, Japan* and K. Okuyama, K. Kubota and H. Ishizuka, *Hitachi, Ltd., Tokyo, Japan* 459

3:10 p.m.
18.3 Real Time Measurement of Transients and Electrode Edge Effects for Plasma Charging Induced Damage, S. Ma and J. McVittie, *Stanford University, Stanford, CA* 463

3:35 p.m.
18.4 Plasma-Induced In-Line Charging and Damage in Non-Volatile Memory Devices, H. Fang, S. Haddad, C. Chang and J. Lien, *Advanced Micro Devices, Sunnyvale, CA* 467

4:00 p.m.
18.5 AC Frequency-Resolved Measurements for Direct Extraction of the Parasitic Resistance of Individual MOSFETs, L. Selmi, A. Alfieri and B. Ricco, *University of Bologna, Bologna, Italy* 471

4:25 p.m.
18.6 A Comprehensive Study of MOSFET Electron Mobility in Both Weak and Strong Inversion Regimes, J. Koga, S. Takagi and A. Toriumi, *Toshiba Corporation, Kawasaki, Japan* 475

4:50 p.m.
18.7 Saturation Velocity and Velocity Overshoot of Inversion Layer Electrons and Holes, F. Assaderaghi, D. Sinitsky, H. Gaw*, J. Bokor, P. Ko and C. Hu, *University of California, Berkeley, CA and *Intel Corp., Santa Clara, CA* 479

SESSION 19: Device Technology — Advanced Device Design 483

Tuesday, December 13, 2:15 p.m.
Continental Ballroom 6

Co-Chairmen: Akira Toriumi, Toshiba
Rajeeva Lahri, National Semiconductor

2:15 p.m.
Introduction

2:20 p.m.
19.1 A 0.05μm CMOS with Ultra Shallow Source/Drain Junctions Fabricated by 5KeV Ion Implantation and Rapid Thermal Annealing, A. Hori, H. Nakaoka, H. Umimoto, K. Yamashita, M. Takase, N. Shimizu, B. Mizuno and S. Odanaka, *Matsushita Electric Ind., Co., Osaka, Japan* **485**

2:45 p.m.
19.2 Low Threshold Voltage CMOS Devices with Smooth Topography for 1 Volt Applications, D. Yu* and K. Lee*, **AT&T Bell Labs, Allentown, PA* and H. Lin, *AT&T Bell Labs, Holmdel, NJ* and C. McAndrew, *AT&T Bell Labs, Cedar Crest, PA* **489**

3:10 p.m.
19.3 Self-Aligned Tungsten Strapped Source/Drain and Gate Technology Realizing the Lowest Sheet Resistance for Sub-quarter Micron CMOS, M. Sekine, K. Inoue, H. Ito, I. Honma, H. Miyamoto, K. Yoshida, H. Watanabe, K. Mikagi, Y. Yamada and T. Kikkawa, *NEC Corp., Kanagawa, Japan* **493**

3:35 p.m.
19.4 W/WNx/Poly-Si Gate Technology for Future High Speed Deep Submicron CMOS LSIs, K. Kasai, Y. Akasaka, K. Nakajima, S. Suehiro, K. Suguro, H. Oyamatsu, M. Kinugawa and M. Kakumu, *Toshiba Corporation, Kawasaki, Japan* **497**

4:00 p.m.
19.5 Supression of MOSFET Reverse Short Channel Effect by N_2O Gate Poly Reoxidation Process, P. Tsui, H. Tseng, M. Orlowski, S. Sun, P. Tobin, K. Reid and W. Taylor, *Motorola, Austin, TX* **501**

4:25 p.m.
19.6 Improved Electrical Characteristics of Thin-Film Transistors Fabricated on Nitrogen-Implanted Polysilicon Films, C. Yang, T. Lei and C. Lee, *National Chiao Tung University, Taiwan, Rep. of China* **505**

4:50 p.m.
19.7 The Role of Point Defect Sources in the Formation of Boron Polyemitters, A. Berthold, A. vom Felde, M. Biebl and H. von Philipsborn, *Siemens AG, Munich, Germany* **509**

SESSION 20: Detectors, Sensors and Displays — Displays and Radiation Sensors **513**

Tuesday, December 13, 2:15 p.m.
Continental Ballroom 7-9

Co-Chairmen: Toshihisa Tsukada, Hitachi
Russel Martin, Xerox PARC

2:15 p.m.
Introduction

2:20 p.m.
20.1 Physics and Applications of Low-Dimensional Organic Thin-Film Transistors, A. Dodabalapur, H. Katz and L. Torsi, *AT & T Bell Laboratories, Murray Hill, NJ* **515**

2:45 p.m.
20.2 Reliability Improvement in Low-Temperature Processed Poly-Si TFTs for AMLCDs, K. Yuda, K. Sera, F. Uesugi*, I. Nishiyama* and F. Okumura, *NEC Corporation, Kanagawa, Japan and *NEC Corporation, Ibaraki, Japan* **519**

3:10 p.m.
20.3 ECR Plasma Oxidation Effects on Performance and Stability of Polysilicon Thin Film Transistors, J.Y. Lee, C. H. Han and C.K. Kim, *Korea Advanced Institute of Science & Technology, Taejon, Korea* **523**

3:35 p.m.
20.4 CMOS-Based Technology for Integrated Opto-Electronics: A Modular Approach, E. Fullin, G. Voirin, M. Chevroulet, A. Lagos and J. Moret, *Centre Suisse D'Electronique et de Microtechnique SA, Neuchatel, Switzerland* **527**

4:00 p.m.
20.5 CMOS Membrane Infrared Sensor and Improved TMAHW Etchant, R. Lenggenhager, D. Jaeggi*, P. Malcovati*, H. Duran*, H. Baltes* and E. Doering, *Cerberus, Schwerzenbach, Switzerland and *ETH Zurich, Zurich, Switzerland* **531**

4:25 p.m.
20.6 Design and Test at Room Temperature of the First Silicon Drift Detector With On-Chip Electronics, R. Hartmann, D. Hauff, S. Krisch, P. Lechner, G. Lutz, R. Richter, H. Seitz and L. Struder, *Inst. fur Physik und Ext. Physik, Munich, Germany* and G. Bertuccio, L. Fasoli, C. Fiorini, A. Gatti, A. Longoni, E. Pinotti and M. Sampietro, *Politecnio de Milano, Milano, Italy* **535**

SESSION 21: Modeling and Simulation — Equipment Modeling **539**

Tuesday, December 13, 2:15 p.m.
Imperial Ballroom A

Co-Chairmen: John Brews, University of Arizona
Tetsunori Wada, Toshiba

2:15 p.m.
Introduction

2:20 p.m.
21.1 Comprehensive RTP Modeling and Simulation Including Thermal Stress Analysis and Feature Size Optical Effects, A. Kolpakov, T. Makhviladze, A. Panjukhin, O. Volchek, and A.F. Erofeev, *Russian Academy of Sciences, Moscow, Russia,* and M. Orlowski, *Motorola Inc., Austin, TX* **541**

2:45 p.m.
21.2 3D Modeling of Rapid Thermal Processors for Design Optimization of a New Flexible RTP System, Y. Chen, L. Booth, C. Schaper, B. Khuri-Yakub and K. Saraswat, *Stanford University, Stanford, CA* **545**

3:10 p.m.
21.3 A Multiple Target Sputter System with Enhanced Wafer Uniformity, Lifetime Uniformity, and Wafer Scaleability, D. Bang, K. Saraswat and J. McVittie, *Stanford University, Stanford, CA* and Z. Krivokapic, *Advanced Micro Devices, Sunnyvale, CA* **549**

3:35 p.m.
21.4 Practical Monte Carlo Sputter Deposition Simulation with Quasi-Axis-Symmetrical (QAS) Approximation, H. Yamada, T. Shinmura, Y. Yamada and T. Ohta, *NEC Corporation, Kanagawa, Japan* **553**

4:00 p.m.
21.5 Surface Melting Model for Al Reflow into Submicron Contact-Holes and Vias, K. Hirose, K. Kikuta and T. Yoshida, *NEC Corp., Kanagawa, Japan* **557**

4:25 p.m.
21.6 Analysis of Parameter Extraction Techniques for VLSI Interconnect Reliability Studies Using Microscopic Computer Simulation, J. Trattles, A. O'Neill and B. Mecrow, *University of Newcastle upon Tyne, Newcastle upon Tyne, United Kingdom* **561**

SESSION 22: Quantum Electronics and Compound Semiconductor Devices — Photonic Devices 565

Tuesday, December 13, 2:15 p.m.
Imperial Ballroom

Co-Chairmen: Stephen Chou, University of Minnesota
Nick Bottka, Office of Naval Research

2:15 p.m.
Introduction

2:20 p.m.
22.1 High-Power InGaN/AlGaN Double-Heterostructure Blue-Light-Emitting Diodes (Invited Paper), S. Nakamura, *Nichia Chemical Industries, Ltd., Tokushima, Japan* 567

2:45 p.m.
22.2 Resonant Cavity Organic Electroluminescent Devices, L. Rothberg, A. Dodabalapur and T. Miller, *AT&T Bell Laboratories, Murray Hill, NJ* 571

3:10 p.m.
22.3 8 X 8 Array of Cascadable Optical Thyristor Devices for Free-Space Parallel Optical Interconnects, P. Heremans, M. Kuijk*, B. Knupfer and G. Borghs, *IMEC, Leuven, Belgium and *Vrije Universiteit Brussel, Brussels, Belgium* 575

3:35 p.m.
22.4 Direct Measurement of Transit Time Effects in MODFETs, J. Sheridan, B. Nechay and D. Bloom, *Stanford University, Stanford, CA,* and P. Solomon, *IBM Watson Research Lab, Yorktown Heights, NY,* and Y. Pao, *Litton Solid State Division, Santa Clara, CA* 579

4:00 p.m.
22.5 Modelling of Breakdown Voltage and Its Temperature Dependence in SAGCM InP/InGaAs Avalanche Photodiodes, C. Ma and M. Deen, *Simon Fraser University, British Columbia, Canada* and L. Tarof and J. Yu, *Bell-Northern Research Ltd, Ontario, Canada* 583

SESSION 23: 1994 IEDM Evening Panel Discussion 587

Tuesday, December 13, 8:00 p.m.
Continental Ballroom 4

Broadband and Wireless Communication: The New Technology Battleground

PANEL MODERATOR:

Armin Weider
Siemens
Munich, Germany

SESSION 24: 1994 IEDM Evening Panel Discussion 589

Tuesday, December 13, 8:00 p.m.
Continental Ballroom 5

Will Flash Memory Replace Hard Disk Drive?

PANEL MODERATOR:
Genda Hu
Cypress Semiconductor
San Jose, CA

SESSION 25: CMOS Devices and Reliability — Ultra-Thin Dielectrics 591

Wednesday, December 14, 9:00 a.m.
Continental Ballroom 1-3

Co-Chairmen: Ih-Chin Chen, Texas Instruments
Jack Lee, The University of Texas

9:00 a.m.
Introduction

9:05 a.m.
25.1 *Tunneling Gate Oxide Approach to Ultra-High Current Drive in Small-Geometry MOSFETs,* H. Momose, M. Ono, T. Yoshitomi, T. Ohguro, S. Nakamura, M. Saito and H. Iwai, *Toshiba Corp., Kawasaki, Japan* 593

9:30 a.m.
25.2 *Efficient Gate Oxide Defect Screen for VLSI Reliability,* J. King, W. Chan and C. Hu, *University of California, Berkeley, CA* 597

9:55 a.m.
25.3 Reliability Characteristics and Surface Preparation Technique for Ultra-thin (33Å-87Å) Oxides and Oxynitrides, M. Hao, K. Lai, W. Chen and J. Lee, *University of Texas, Austin, TX* 601

10:20 a.m.
25.4 Quasi-Breakdown of Ultrathin Gate Oxide Under High Field Stress, S. Lee, B. Cho, J. Kim and S. Choi, *Hyundai Electronics Industries, Co., Ltd., Kyoungki-do, Korea* 605

10:45 a.m.
25.5 Reliability of Thin SiO_2 at Direct-Tunneling Voltages, K. Schuegraf, *Micron Semiconductor, Inc., Boise, ID* and D. Park and C. Hu, *University of California, Berkley, CA* 609

11:10 a.m.
25.6 Determination of Ultra-Thin Gate Oxide Thicknesses for CMOS Structures Using Quantum Effects, R. Rios and N. Arora, *Digital Equipment Corporation, Hudson, MA* 613

11:35 a.m.
25.7 Polarity Dependence of Dielectric Breakdown in Scaled SiO_2, L. Han, M. Bhat, D. Wristers, J. Fulford*, and D. Kwong, *The University of Texas, Austin, TX and *Advanced Micro Devices, Austin, TX* 617

SESSION 26: Integrated Circuits — Advanced DRAM and SRAM Devices 621

Wednesday, December 14, 9:00 a.m.
Continental Ballroom 4

Co-Chairmen: Chang Hwang, Samsung
Takomitsu Kunio, NEC

9:00 a.m.
Introduction

9:05 a.m.
26.1 *A Symmetric Vss Cross-Under Bitcell Technology for 64Mb SRAMs,* J. Pfiester, J. Hayden, M. Thompson, F. Miller, J. Lin, M. Blackwell, K. Mocala, Y. Ku, C. Subramanian, W. Waldo, S. Ajuria, B. James and B. Martino, *Motorola, Austin, TX* 623

9:30 a.m.
26.2 Impact of the Minority Carrier Outflow (MCO) Effect on the α-Particle-Induced Soft Error of Scaled DRAMs, Y. Oowaki, K. Mabuchi, T. Hasegawa, S. Manabe, S. Watanabe, K. Ohuchi and F. Masuoka, *Toshiba, Kawasaki, Japan* 627

9:55 a.m.
26.3 Triple Density DRAM Cell with Si Selective Growth Channel and NAND-Structure, M. Aoki, M. Noguchi, T. Hamamoto, S. Tokano, Y. Saito, T. Hoshi and S. Watanabe, *Toshiba, Kawasaki, Japan* 631

10:20 a.m.
26.4 Highly Manufacturable Process Technology for Reliable 256 Mbit and 1Gbit DRAMs, H. Kang, K. Kim, Y. Shin, I. Park, K. Ko, C. Kim, K. Oh, S. Kim, C. Hong, K. Kwon, J. Yoo, Y. Kim, C. Lee, W. Paick, D. Suh, C. Park, S. Lee, S. Ahn, C. Hwang and M. Lee, *Samsung, Kyungki-do, Korea* 635

10:45 a.m.
26.5 1GDRAM Cell with Diagonal Bit-Line (DBL) Configuration and Edge Operation MOS(EOS) FET, K. Shibahara, H. Mori, S. Ohnishi, R. Oikawa, K. Nakajima, Y. Kojima, H. Yamashita, K. Itoh, S. Kamiyama, H. Watanabe, T. Hamada and K. Koyama, *NEC Corporation, Kanagawa, Japan* **639**

SESSION 27: CMOS Devices and Reliability — SOI Devices **643**

Wednesday, December 14, 9:00 a.m.
Continental Ballroom 5

Co-Chairmen: Mitsu Koyanagi, Tohoku University
Jacques Gautier, LETI

9:00 a.m.
Introduction

9:05 a.m.
27.1 Extremely Thin Film (10nm) SOI MOSFET Characteristics Including Inversion Layer to Accumulation Layer Tunneling, J.H. Choi, Y. Park and H. Min, *Seoul National University, Seoul, Korea* **645**

9:30 a.m.
27.2 Tradeoffs of Current Drive VS Short-channel Effect in Deep-Submicrometer Bulk and SOI MOSFETs, L. Su, H. Hu, J. Jacobs, M. Sherony, A. Wei and D. Antoniadis, *MIT, Cambridge, MA* **649**

9:55 a.m.
27.3 Effect of the Back Gate Conduction on 0.25μm SOI Devices, J. Pelloie, *LETI, Grenoble, France* and D. Sadana, H. Hovel, G. Shahidi, J. Warnock, J. Sun and B. Davari, *IBM, Yorktown Heights, NY* **653**

10:20 a.m.
27.4 A New Approach to Implement 0.1μm MOSFET on Thin-Film SOI Substrate with Self-Aligned Source-Body Contact, V. Chen and J. Woo, *University of California, Los Angeles, CA* **657**

10:45 a.m.
27.5 Photon Emission from SOI MOSFET with Body Terminal, M. Koyanagi, T. Matsumoto, T. Shimatani, F. Balestera*, Y. Hiruma**, M. Okabe** and Y. Inoue***, *Tohoku University, Sendai, Japan and *LPCS/ENSERG, Grenoble, France and **Hamamatsu Photonics K.K. and ***Mitsubishi Electric Co.* **944**

11:10 a.m.
27.6 Dynamic Floating-Body Instabilities in Partially Depleted SOI CMOS Circuits, D. Suh and J. Fossum, *University of Florida, Gainesville, FL* **661**

11:35 a.m.
27.7 Dynamic Performance and Leakage Current Characteristics of 1/4-Micron-Gate Ultra-Thin CMOS/SIMOX Gate Array, Y. Kado, T. Ohno, Y. Sakakibara, Y. Kawai, E. Yamamoto, A. Ohtaka and T. Tsuchiya, *NTT LSI Laboratories, Kanagawa, Japan* **665**

SESSION 28: Device Technology — CMOS Advanced Process: Isolation, Silicides **669**

Wednesday, December 14, 9:00 a.m.
Continental Ballroom 6

Co-Chairmen: Michel Haond, France Telecom CNET
Shuji Ikeda, Hitachi

9:00 a.m.
Introduction

9:05 a.m.
28.1 Characteristics of CMOS Device Isolation for the ULSI Age (Invited Paper), A. Bryant, *IBM Microelectronics Div., Essex Junction, VT* and W. Hansch, *Siemens Components, Inc., Iselin, NJ* and T. Mii, *IBM Microelectronics, Hopewell Junction, NY* **671**

9:30 a.m.
28.2 Self-Aligned LOCOS/Trench (SALOT) Combination Isolation Technology Planarized by Chemical Mechanical Polishing, S.J. Ahn, T. Park, J. Ko, C. Hong, J. Kim, S.T. Ahn and M. Lee, *Samsung Electronics Co., Ltd., Kyungki-do, Korea* **675**

9:55 a.m.
28.3 A Highly Practical Modified LOCOS Isolation Technology for the 256 Mbit DRAM, D. Ahn, S.J. Ahn, P. Griffin*, M. Hwang, W. Lee, S.T. Ahn, C. Hwang and M. Lee, *Samsung Electronics Co., Ltd., Kyungki-Do, Korea and *Stanford University, Stanford, CA* **679**

10:20 a.m.
28.4 Nitrogen In-Situ Doped Poly Buffer LOCOS: Simple and Scalable Isolation Technology for Deep-Submicron Silicon Devices, T. Kobayashi, S. Nakayama, M. Miyake and Y. Okazaki, *NTT LSI Laboratories, Atsugi-shi, Japan* **683**

10:45 a.m.
28.5 Discussion Session

11:10 a.m.
28.6 A Novel Salicide Process (SEDAM) for Sub-Quarter Micron CMOS Devices, *T. Mogami, H. Wakabayashi, Y. Saito, T. Matsuki, T. Tatsumi and T. Kunio,* NEC Corporation, Kanagawa, Japan **687**

11:35 a.m.
28.7 A Novel $CoSi_2$ Thin Film Process with Improved Thickness Scalability and Thermal Stability, W. Chen, J. Lin and J. Lee, *University of Texas, Austin, TX* **691**

12:00 p.m.
28.8 200 mm Process Integration for a 0.15μm Channel-Length CMOS Technology Using Mixed X-Ray/Optical Lithography, S. Subbanna, E. Ganin, E. Crabbe, J. Comfort, S. Wu, P. Agnello, B. Martin, M. Moncord, H. Ng, T. Newman, P. McFarland, J. Sun, J. Snare, A. Acovic, A. Ray, R. Gehres, R. Schulz, S. Greco, K. Beyer, L. Liebman, R. DellaGuardia, and A. Lamberti, *IBM, Hopewell Junction, NY* **695**

SESSION 29: Detectors, Sensors and Displays — Image Sensors **699**

Wednesday, December 14, 9:00 a.m.
Continental Ballroom 7-9

Co-Chairmen: Young-June Yu, GoldStar Electron
Robert Wisnieff, IBM T.J. Watson Research Center

9:00 a.m.
Introduction

9:05 a.m.
29.1 Mega Pixel CCD Image Sensor Technology (Invited Paper), S. Chamberlain, S. Kamasz, C. Smith, W. Washkurak, and M. Farrier, *Dalsa Inc., Ontario, Canada* **701**

9:30 a.m.
29.2 A Low Driving Voltage CCD with Single Layer Electrode Structure for Area Image Sensor, N. Tanaka, N. Nakamura, Y. Matsunaga, S. Manabe and O. Yoshida, *Toshiba Corporation, Kawasaki, Japan* **705**

9:55 a.m.
29.3 A 1/4" True Progressive Scan 640(H)* 480(V) Ft-CCD for Multimedia Applications, J. Bosiers, E. Roks, H. Peek, Y. Boersma, J. van der Heyden, *Philips Imaging Technology, Eindhoven, The Netherlands* **709**

10:20 a.m.
29.4 A Flattened-Pear Shaped Photodiode Structure for Low Smear and High Sensitivity CCD Image Sensors, M. Furumiya, Y. Kawakami, I. Murakami, M. Morimoto, N. Mutoh, K. Orihara, K. Hatano, S. Suwazono, K. Arai, N. Teranishi and Y. Hokari, *NEC Corporation, Kanagawa, Japan* 713

10:45 a.m.
29.5 An Infrared-Bi-Color Schottky-Barrier Infrared CCD Image Sensor for Precise Thermal Image, K. Konuma, Y. Asano, K. Masubuchi, H. Utsumi, S. Tohyama, T. Endo, H. Azuma, and N. Teranishi, *NEC Corporation, Kanagawa, Japan* 717

11:10 a.m.
29.6 Voltage-Controlled Spectral Response in n-SnO_2/a-SiC_x/Metal Photodetector, M. Rossi, R. Vincenzoni and F. Galluzzi, *University of Rome, Rome Italy* 721

SESSION 30: Modeling and Simulation — Simulation of Novel Devices 725

Wednesday, December 14, 9:00 a.m.
Imperial Ballroom A

Co-Chairmen: Jean-Pierre LeBurton, University of Illinois
Paco Leon, Intel

9:00 a.m.
Introduction

9:05 a.m.
30.1 First Three-Dimensional Numerical Analysis of Magnetic Vector Probe, C. Riccobene, K. Gartner*, G. Wachutka, H. Baltes and W. Fichtner*, *ETH-Honggerberg, Zurich, Switzerland and * ETH-Zentrum, Zurich, Switzerland* 727

9:30 a.m.
30.2 Mobility Simulation in Si/SiGe Heterostructure FETs, A. Abramo, J. Bude, F. Venturi* and M. Pinto, *AT&T Bell Laboratories, Murray Hill, NJ and *University of Parma, Parma, Italy* 731

9:55 a.m.
30.3 Quantum Mechanical Modeling of the Charge Distribution in a Si/$Se_{1-x}Ge_x$/Si P-Channel MOS FET, M. Hargrove and A. Henning, *Dartmouth College, Hanover, NH* and J. Slinkman, *IBM Microelectronics Division, Essex Junction, VT* and J. Bean, *AT&T Bell Laboratories, Murray Hill, NJ* 735

10:20 a.m.
30.4 Anomalies in the Output Conductance of SiGe HBTs, H. M. Rein and M. Friedrich, *Ruhr-University Bochum, Bochum, Germany* 739

10:45 a.m.
30.5 Modelling and Simulation of High Speed, High Voltage Bipolar SOI Transistor with Fully Depleted Collector, T. Arnborg, *Ericsson Components, Stockholm, Sweden* 743

11:10 a.m.
30.6 Design and Performance Considerations for Sub-0.1μm Double-Gate SOI MOSFETs, H. Wong, D. Frank, Y. Taur and J. Stork, *IBM, Yorktown Heights, NY* 747

11:35 a.m.
30.7 Experiment and Modeling of Thermal Crosstalk in Semiconductor Laser Arrays, N. Bewtra, D. Suda, M. Dion*, F. Chatenoud* and J. Xu, *University of Toronto, Toronto, Canada and *National Research Council, Ottawa, Canada* 751

SESSION 31: Quantum Electronics and Compound Semiconductor Devices — Semiconductor Lasers 755

Wednesday, December 14, 9:00 a.m.
Imperial Ballroom B

Co-Chairmen: Connie Chang-Hasnain, Stanford University
Philip Pitner, SiBond

9:00 a.m.
Introduction

9:05 a.m.
31.1 Long-wavelength Vertical-Cavity Lasers (Invited Paper), D. Babic, J. Dudley, R. Mirin, J. Bowers and E. Hu, *University of California, Santa Barbara, CA* 757

9:30 a.m.
31.2 Self-Aligned Integration of 8 x 1 Micromachined Micro-Fresnel Lens Arrays and 8 x 1 Vertical Cavity Surface Emitting Laser Arrays for Free-Space Optical Interconnect, S. Lee, L. Lin, K. Pister, M. Wu, H. Lee* and P. Grodzinski*, *UCLA, Los Angeles, CA and *Motorola, Inc., Phoenix, AZ* 761

9:55 a.m.
31.3 Novel Vertical-Cavity Surface-Emitting Lasers with Integrated Optical Beam Router for Massively Free-Space Interconnection, L. Fan, M. Wu, H. Lee* and P. Grodzinski*, *UCLA,Los Angeles, CA and *Motorola, Phoenix, AZ* 765

10:20 a.m.
31.4 680nm Band High-Power Individually Addressable Two-Beam Lasers with Low Thermal Interference, A. Takamori, M. Mannoh and K. Ohnaka, *Matsushita Electric Industrial Co., Ltd., Osaka, Japan* 769

10:45 a.m.
31.5 151 Channel AM-FDM Transmission Using 1.3μm Strained-Layer MQW-DFB Laser with High Optical Output Power Operation, N. Takenaka, M. Kito, K. Fujihara, N. Otsuka, M. Ishino, M. Tanabe and Y. Matsui, *Matsushita Electric Ind. Co., Ltd., Osaka, Japan* 773

SESSION 32: Vacuum Electronics — Linear Beam Devices 777

Wednesday, December 14, 1:30 p.m.
Continental Ballroom 1-3

Co-Chairmen: Jim Hickey, Teledyne ET
Gerard Kantorowicz, Thomson-CSF

1:30 p.m.
Introduction

1:35 p.m.
32.1 Progress in Microminiature Thermionic Vacuum Tube Devices, L. Sadwick, D. Schaeffer, Y. Zhang, D. Petelenz, S. Holmes, R. Hwu and G. Sandquist, *University of Utah, Salt Lake City, UT* 779

2:00 p.m.
32.2 The Cassini Mission Ka-Band TWT, A. Curren, J. Dayton, Jr.,R. Palmer, K. Long and D. Force, *NASA Lewis Res. Ctr, Cleveland, OH* and C. Weeder and Z. Zachar, *Hughes Aircraft Co., Torrance, CA* and W. Harvey, *Jet Propulsion Lab, Pasadena, CA* 783

2:25 p.m.
32.3 A Microwave Power Module for Phased Arrays, G. Groshart, *Northrop Grumman, Rolling Meadows, IL* †

2:50 p.m.
32.4 Satellite TWT-Amplifiers Using the Microwave Power Module Concept and Radiation Cooled Collectors, G. Kornfeld, *AEG, Ulm, Germany* 787

3:15 p.m.
32.5 Multi-Stage Pasotron™ Experiments, E. Garland-Ponti, J. Butler, J. Santoru and D. Goebel, *Hughes Research Laboratories, Malibu, CA,* R. Eisenhart, *Hughes Missile Systems Co., Canoga Park, CA* 791

3:40 p.m.
32.6 Twystrode Experiments with Tapered Helices, M. Kodis, N. Vanderplaats, H. Freund* and E. Zaidman, *Naval Research Laboratory, Washington, DC and *Science Applications Int'l Corp., McLean, VA* and B. Goplen and D. Smithe, *Mission Research Corp., Newington, VA* 795

4:05 p.m.
32.7 The Design and Performance of 150-MW S-Band Klystrons, D. Sprehn, R. Phillips, and G. Caryotakis, *Stanford Linear Accelerator Center, Stanford, CA* 799

4:30 p.m.
32.8 Thermomechanical Factors in Molybdenum Field Emitter Operation and Failure, M. Ancona, *Naval Research Laboratory, Washington, DC* 803

SESSION 33: Solid State Devices — SOI and Bipolar Technology 807

Wednesday, December 14, 1:30 p.m.
Continental Ballroom 5

Co-Chairmen: Emmerich Bertagnolli, Siemens
Nobuo Sasaki, Fujitsu

1:30 p.m.
Introduction

1:35 p.m.
33.1 A Dynamic Threshold Voltage MOSFET (DTMOS) for Ultra-Low Voltage Operation, F. Assaderaghi, D. Sinitsky, S. Parke*, J. Bokor, P. Ko and C. Hu, *University of California, Berkeley, CA and *IBM Corporation, East Fishkill, NY* 809

2:00 p.m.
33.2 Comparison of Self-Heating Effects in Bulk-Silicon and SOI High-Voltage Devices, E. Arnold, H. Pein and S. Herko, *Philips Electronics North America Corporation, Briarcliff Manor, NY* 813

2:25 p.m.
33.3 Recent Advances in SOI Technology (Invited Paper), J. Colinge, *Universite Catholique de Louvain, Louvain-la-Neuve, Belgium* 817

2:50 p.m.
33.4 Discussion Session

3:15 p.m.
33.5 A 47 GHz Bipolar Process with an Ultra Shallow Ion Implanted Base of 35nm, R. Mahnkopf, M. Bianco and H. Klose, *Siemens AG, Munich, Germany* 821

3:40 p.m.
33.6 18 ps ECL-Gate Delay in Laterally Scaled 30 GHz Bipolar Transistors, A. Pruijmboom, C. Timmering and J. Hageraats, Philips Research Laboratories, Eindhoven, The Netherlands 825

SESSION 34: Device Technology — Memory Technology 829

Wednesday, December 14, 1:30 p.m.
Continental Ballroom 6

Co-Chairmen: Pierre Fazan, Micron Semiconductor
Sung Tae Ahn, Samsung Electronics

1:30 p.m.
Introduction

1:35 p.m.
34.1 A Gbit-Scale DRAM Stacked Capacitor Technology with ECR MOCVD $SrTiO_3$ and RIE Patterned RuO_2/TiN Storage Nodes, P. Lesaicherre, S. Yamamichi*, H. Yamaguchi*, K. Takemura*, H. Watanabe, K. Tokashiki, K. Satoh, T. Sakuma*, M. Yoshida*, S. Ohnishi, K. Nakajima, K. Shibahara, Y. Miyasaka* and H. Ono, *NEC, Sagamihara, Japan and *NEC Corp., Kawasaki, Japan* 831

2:00 p.m.
34.2 Ta_2O_5 Capacitors for 1Gbit DRAM and Beyond, K. Kwon, I. Park, D. Han, E. Kim, S. Ahn and M. Lee, *Samsung Electronics Co., Ltd., Kyungki-do, Korea* 835

2:25 p.m.
34.3 Low-Temperature Integrated Process Below 500°C for Thin Ta_2O_5 Capacitor for Giga-Bit DRAMs, Y. Takaishi, M. Sakao, S. Kamiyama, H. Suzuki and H. Watanabe, *NEC Corporation, Kanagawa, Japan* 839

2:50 p.m.
34.4 A Half-Micron Ferroelectric Memory Cell Technology with Stacked Capacitor Structure, S. Onishi, K. Hamada, K. Ishihara, Y. Ito, S. Yokoyama, J. Kudo and K. Sakiyama, *Sharp Corporation, Nara, Japan* 843

3:15 p.m.
34.5 The Solution of Over-Erase Problem Controlling Poly-Si Grain Size Modified Scaling Principles for FLASH Memory, S. Muramatsu, T. Kubota, N. Nishio, H. Shirai, M. Matsuo, N. Kodama, M. Horikawa, S. Saito, K. Arai and T. Okazawa, *NEC Corp., Kanagawa, Japan* 847

3:40 p.m.
34.6 Short-Channel Vertical NMOSFETs for High Density Fast SRAMs, A. Perera, C. Lage, J. Hayden, J. Lin, R. Rodriguez and S. Ajuria, *Motorola, Austin, TX* 851

4:05 p.m.
34.7 Dual Polycide Gate and Dual Buried Contact Technologies Achieving a 0.4μm nMOS/pMOS Spacing for a 7.65μm² Full-CMOS SRAM Cell, H. Koike, Y. Unno, K. Ishimaru, F. Matsuoka and M. Kakumu, *Toshiba Corp., Kawasaki, Japan* 855

SESSION 35: Modeling and Simulation — Process Modeling 859

Wednesday, December 14, 1:30 p.m.
Imperial Ballroom A

Co-Chairmen: Mark Law, University of Florida
Martin Giles, Intel

1:30 p.m.
Introduction

1:35 p.m.
35.1 Device Implications of Enhanced Diffusion Caused by the Electrical Deactivation of Arsenic, P. Rousseau, P. Griffin , S. Kuehne, and J. Plummer, *Stanford University, Stanford, CA* 861

2:00 p.m.
35.2 Two-Dimensional Transient Enhanced Diffusion and Its Impact on Bipolar Transistors, M. van Dort, W. van der Wel, J. Slotboom, N. Cowern, M. Knuvers, H. Lifka, and P. Zalm, *Philips Research Laboratories, Eindhoven, The Netherlands* 865

2:25 p.m.
35.3 A Continuous and General Model for Boron Diffusion During Post-Implant Annealing Including Damaged and Amorphizing Conditions, B. Baccus and E. Vandenbossche, *IEMN-ISEN, Lille, France* 869

2:50 p.m.
35.4 A New Boron Diffusion Model Incorporating the Dislocation Loop Growth, K. Uwasawa, T. Uchida, T. Ikezawa, M. Hane, T. Matsuki, H. Kato and K. Ishida, *NEC Corporation, Kanagawa, Japan* **873**

3:15 p.m.
35.5 An Advanced Calibration Method for Modelling Oxidation and Mechanical Stress in Sub-Micron CMOS Isolation Structures, S. Jones, A. Poncet*, I. De Wolf**, M. Ahmed and W. Rothwell***, *GEC-Marconi Materials, Northants, UK and *CNET/CNS, Meylan, France and **IMEC, Leuven, Belgium and ***BT-DPTD, Ipswich, UK* **877**

3:40 p.m.
35.6 Simulation of Advanced Field Isolation Using Calibrated Viscoelastic Stress Analysis, V. Senez, D. Collard, P. Ferreira and B. Baccus, *IEMN-ISEN, Lille, France* **881**

4:05 p.m.
35.7 Three-Dimensional Mechanical Stress Analysis of Trench Isolation Along {111} Gliding Planes, S. Matsuda, C. Yoshino, H. Nakajima, K. Inou, S. Yoshitomi, Y. Katsumata and H. Iwai, *Toshiba Corp., Kawasaki, Japan* **885**

SESSION 36: Quantum Electronics and Compound Semiconductor Devices — Compound Semiconductor Field Effect Transistors **889**

Wednesday, December 14, 1:30 p.m.
Imperial Ballroom B

Co-Chairmen: Ilesanmi Adesida, University of Illinois
Gerald Witt, AFORSR/NE

1:30 p.m.
Introduction

1:35 p.m.
36.1 First High Performance InAlAs/InGaAs HEMTs on GaAs Exceeding That on INP, K. Higuchi, M. Kudo, M. Mori and T. Mishima, *Hitachi, Ltd., Tokyo, Japan* **891**

2:00 p.m.
36.2 Highly-Efficient 6.6W 12GHz HJFET for Power Amplifier, K. Matsunaga, Y. Okamoto and M. Kuzuhara, *NEC Corporation, Shiga, Japan* **895**

2:25 p.m.
36.3 2V Operation Pseudomorphic Power HEMT with 62% Power-Added Efficiency for Cellular Phones, H. Ono, Y. Umemoto, H. Ichikawa, M. Mori, M. Kudo, O. Kagaya and Y. Imamura, *Hitachi, Ltd., Tokyo, Japan* **899**

2:50 p.m.
36.4 A 3.6 GHz Dual Modulus Prescaler IC Using Optimal Pseudomorphic HEMT Structure on Si Substrates, H. Suehiro, T. Ohori, Y. Nakasha, T. Miyata, Y. Watanabe, S. Kuroda and M. Takikawa, *Fujitsu Laboratories, Ltd., Atsugi, Japan* **903**

3:15 p.m.
36.5 An Extremely Low-Noise InP-Based HEMT with Silicon Nitride Passivation, M. Kao, K. Duh, P. Ho and P. Chao, *Martin Marietta Laboratories, Syracuse, NY* **907**

3:40 p.m.
36.6 Accurate Modeling of GaAs MESFET Sidegating Effects by Trapping Simulation, Y. Liu, Z. Yu, R. Dutton and M. Deal, *Standford University, Stanford, CA* **911**

LATE NEWS **915**

†This manuscript unavailable for publication.

SESSION 1

PLENARY SESSION

Monday, December 12, 9:00 a.m.
Continental Ballroom

Chairman: John Aitken, IBM Microelectronics

INVITED PAPERS

Chairman: Rick Sivan, Motorola

A diverse set of exciting topics highlights the 1994 IEDM Plenary Session. This year's speakers are established in their areas of expertise, possess substantial experience in industry and academia, and represent Asia, Europe and North America.

The Plenary Session opens with Professor Robert Birge (W.M. Kech Center for Molecular Electronics, Syracuse University), who describes his research into the field of Bioelectronics. Biological materials with specific optical properties are being exercised in order to assess their suitability as substitutes for today's inorganic electronic materials. Systems fabricated from such materials may provide a natural pathway to scale massively parallel computer systems and dense, three-dimensional memories.

Professor Yasuo Tarui (School of Science and Engineering, Waseda University) is our second speaker. Professor Tarui's interest in memory technology has spanned the economics of DRAM scaling to fundamental research into ferroelectric materials. Aspects of the technical challenges and opportunities afforded by the application of ferroelectric materials to non-volatile memories as well as the potential that such memories offer with respect to known economic scaling rules are described.

Dr. Teun J.B. Swanenburg (Philips Corporate Research) presents his views of the hot topics of multimedia and the information highway. A continuing rapid decrease of the cost/performance ratio brings new levels of capability to the consumer market place. Existing, established businesses and systems may be transformed radically as new functionality and performance levels are achieved.

NOTES

Bioelectronics, Three-Dimensional Memories and Hybrid Computers

Robert R. Birge, Deshan S.K. Govender, Richard B. Gross, Albert F. Lawrence,
Jeffrey A. Stuart, Jack R. Tallent, Eric Tan and Bryan W. Vought

W.M. Keck Center for Molecular Electronics, and
Departments of Chemistry, Physics & Electrical and Computer Engineering
Syracuse University, Syracuse, New York 13244 USA

Abstract

The promise of new architectures and more cost-effective miniaturization has prompted interest in hybrid molecular and semiconductor computers. Nature has already optimized some molecules for such applications. We examine here the use of the protein bacteriorhodopsin in associative and three-dimensional memories and the potential for making hybrid computer systems which combine semiconductor and biomolecular components.

Introduction

Molecular electronics is broadly defined as the encoding, manipulation and retrieval of information at a molecular or macromolecular level. This approach contrasts with current techniques, in which these functions are accomplished via lithographic manipulation of bulk materials to generate integrated circuits. A key advantage of the molecular approach is the ability to design and fabricate devices from the "bottom-up", on an atom-by-atom basis. Lithography can never provide the level of control available through organic synthesis or genetic engineering. Biomolecular electronics is a subfield of molecular electronics that investigates the use of native as well as modified biological molecules (chromophores, proteins, etc.) in electronic or photonic (i.e. light-activated) devices. Because natural selection processes have often solved problems of a similar nature to those that must be solved in harnessing organic compounds, and because self-assembly and genetic engineering provide sophisticated control and manipulation of large molecules, biomolecular electronics has shown considerable promise. The subject has recently been reviewed from a variety of perspectives (1).

The two most commonly stated rationales for exploring molecular electronics are size and speed. A molecular computer could, in principle, be one-thousand times smaller and one-thousand times faster than a present day semiconductor computer composed of a comparable number of logic gates. However, current projections suggest that semiconductor device sizes will approach the molecular domain around 2030 (2). If size and speed were the only rationale for investigating molecular electronics, the field would have limited commercial potential. The opportunity to explore new architectures is one of the key aspects of molecular electronics that has prompted enthusiasm. For example, optical associative memories and three-dimensional memories can be implemented conveniently by using molecular electronics. Implementation of these memories within hybrid systems is anticipated to have near-term application. Before we examine various systems in more detail, we should note that liquid crystal display technology is a prime example of a hybrid molecular-semiconductor technology that has achieved wide-spread success. It is only a beginning, however.

There are many different approaches to molecular electronics that could be explored here, but we will concentrate on one approach that has achieved recent success due to a major international effort involving research groups in the U.S., Canada, Europe and Japan. The interest dates back to the early 1970s and the discovery of a bacterial protein that has unique photophysical properties (3). The protein is called bacteriorhodopsin and it is grown by a salt-loving bacterium that populates salt marshes. A light absorbing group (called the chromophore) imbedded inside the protein matrix converts the light energy into a complex series of molecular events that pump a proton. The proton gradient that is generated is used by the organism to convert ADP to ATP, and is a source of energy. Scientists using the protein for bioelectronic devices exploit the fact that this complex series of thermal reactions results in dramatic changes in the optical and electronic properties of the protein (Fig. 1). The excellent holographic properties of the protein derive from the large change in refractive index that occurs following light activation. Furthermore, bacteriorhodopsin converts light into a refractive index change with remarkable efficiency (approximately 65%). The size of the protein is ten times smaller than the wavelength of light which means that the resolution of the thin film is determined by the diffraction limit of the optical geometry rather than the "graininess" of the film. Also, the protein can absorb two photons simultaneously with an efficiency that far exceeds other materials. This latter capability allows the use of the protein to store information in three dimensions by using

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