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A NEW HIGH FREQUENCY NPN SILICON TRANSISTOR

by

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INTRODUCTION

In 1956, the Semiconductor Products Department of the General Electric Co., released for large-scale production the first of a new line of NPN silicon transistors.* These transistors are designed for operation in either amplifier or switching circuit applications over an extended range of frequency and temperature. This newly-developed silicon transistor is made by a diffused-meltback process, developed by Dr. I. A. Lesk of the GE advanced Semiconductor Laboratory. This process offers a degree of uniformity and control in junction formation not seen by other known methods in use today. Furthermore, the process affords maximum economic utilization of costly single crystal silicon, since the base regions are formed directly in individually diced bars.

Using a combination of the principle of impurity segregation and solid-state diffusion, the diffused-meltback technique can produce base widths as thin as 2 microns with relative ease. The base layers are characterized with graded impurity distributions which enhances the frequency response by the drift-field effect. Alpha-cutoffs as high as 200 megacycles have been seen. Also, the collector region is characterized with a short high resistivity "Plateau" followed by a heavily-doped n-type region. This combination provides low output capacitances per unit area, high avalanche breakdown voltages, and virtually eliminates any "punch-thru"effects, without introducing high collector series resistances. One of the outstanding features of this silicon transistor is its low saturation resistance, which is nominally rated at 40 ohms.

In the following sections of this paper, the electrical characteristics and a description of the diffused-meltback process and device fabrication are given. Also, the parameter variations with respect to frequency, bias, and temperature are presented.

*Developed under U.S. Air Force Contracts, Research and Development AF 33(600)17793 and Production Refinement AF 33(600)28956 issued out of AMC, Dayton, Ohio.

TYPICAL ELECTRICAL CHARACTERISTICS

To properly describe the general performance characteristics of the silicon diffused-meltback transistor, designated as GE type 4JD4A, it would be best to indicate the typical values of the more pertinent parameters for the production units. These are listed in Table I, grouped for both high-frequency and DC characteristics.

Under the high-frequency characteristics, the alpha-cutoff frequency distribution centers at 25 megacycles, with all units exceeding 15 megacycles. A good portion of the cut-off distribution is in excess of 50 megacycles. High-frequency power gain is measured in an unneutralized matched-input tuned-output circuit at a frequency of 5 megacycles. The typi al value is 13 decibels, measered at I_E = -2 ma. and V_C = 10 volts. For those units having a beta-cutoff greater than 1 megacycles, the power gain is in excess of 15 db. The colledtor output capacitance, C_{ob}, measured at 1 megacycle and V_C = 5 volts, is typically 14 uuf. Lastly, the high-frequency reverse foltage feedback factor, h'_{rb}, is 60 x 10^{-3} at 1 megacycle.

For the DO characteristics, in Table I, the typical common-emitter current gain is 30 measured at I_E = -2 ma. and V_C = 5 volts. This corresponds to an alpha of .968. All 4JD4A transistors are tested to assure a minimum current gain of 9, corresponding to an alpha of .9. Of utmost importance, particularly for switching applications, is the low series resistance of the collector for which 40 ohms is the typical value. This is measured in a forced-beta circuit, which puts the transistor well into saturation. The reverse-biased collector current, I_{CO}, measured at 5 volts, has a low nominal value of 10 millimicroamperes. Finally, all the breakdown voltages specified are limited by the avalanche effect and are measured at a current of 1 milliampere, which is well within the sharp breakdown region for silicon, Because of the unique impurity distribution of this transistor (to be described in a later section), the collector-junction barrier spreading will extend much deeper into the collector, rather than into the base. This eliminates the occurrance of voltage "punch-thru", in spite of the extremely thin base. Emitter-to-base breakdown is nominally at 7 volts and the distribution range is quite narrow. This relatively high voltage rating makes the transistor very suitable for switching applications, where it is required to turn off with large reverse voltages.

DIFFUSED-MELTBACK PROCESS

It has been rapidly recognized by the transistor industry, that the principle of solid-state diffusion of impurities offers the most promise of achieving uniformly the thin base regions necessary for very high frequency transistor performance. Because the diffusion cycle usually taked place over a period of several hours, the need for split-second accuracy is eliminated, thereby affording a high degree of process control. Moreover, by diffusing impurities which are already within the solid rather than on the surface, one gains another advantage in that the process is not affected by variations in surface properties and concentrations. It is for these reasons that the diffused-meltback process becomes so attractive as a means of making high-frequency NPN silicon transistors.

The process begins with the growth of a large single-crystal of silicon, which is intentionally doped with both n-type donor and p-type acceptor impurities. The doping concentrations are such that the crystal grows uniformly n-type of low resistivity, corresponding to the emitter region of the final transistor. The crystal is then sawed into wafers and each wafer is then diced into bars approximately 1/8" long and .020" square. In (a) of Figure 1, the relative impurity concentrations within the bar of silicon are shown. At this step, the bar is everywhere homogenously n-type. One full-grown silicon crystal will yield thousands of these bars, each (after subsequent processing) corresponding to a unit transistor. The fact that almost all of the initial crystal is utilized, affords an economic advantage in that the silicon material costs are kept quite low.

The second step of the process is called "meltback", in which one end of the bar is remelted or melted-back, and then solidified again[2]. This forms the tear-drop shape shown in (b) of Figure 1. Because the impurities are less soluble in the solid silicon than in the liquid, the impurities will segregate as the melted-portion freezes, forming the distributions shown in (b). Just at the liquid-solid interface, the initial impurity concentrations drops sharply to very low values determined by the concentrations and segregation coefficients of the initial impurities. In this region, the conductivity is still n-type, but the resistivity is much higher in the order of an ohm-cm or more. It should be noted that this high resistivity plateau extends only for a few thousandths of an inch, whereupon the resistivity drops quickly throughout the remainder of the meltback region. It should be emphasized that after melt-back, we have not as yet formed the base region, but simply a junction between two n-type regions of different resistivity.

The last step of the diffused-meltback process is when the base region is formed, thereby establishing the final npn transistor structure. This is accomplished by subjecting the melt-back bar to a long, high-temperature heating cycle, which lasts for many hours. Under the conditions, the impurities on the high concentration side of the meltback junction diffuse within the solid semiconductor into the "plateau" region of lower concentration. The final distribution of impurities after diffusion is shown in (c) of Figure 1, where the diffused distributions are given by the error-function relationship, viz.,

$$C(x,t) = \frac{C_o}{2}\left[1 - erf\left(\frac{x}{2\sqrt{Dt}}\right)\right] cm^{-3} \qquad (1)$$

In equation (1), C_o is the net concentration difference of the respective impurities before diffusion, D is the diffusivity in cm^2/sec for the impurity in silicon at the cycle temperature, and t is the diffusion cycle time in seconds. Thus, C(x, t) represents the final concentrations as a function of distance and time. The significant point to note here is that the p-type impurity has the property of diffusing almost 20 times faster than the n-type impurity in silicon. Therefore, on the "plateau" side of the junction, there results an excess of p-type impurities over the n-type, corresponding to a thin, p-type base region. By proper choice of the initial impurity concentrations and the time and temperature of the diffusion cycle, heavily-doped bases as thin as 2 microns are obtained with relative ease.

The final overall impurity distribution of the silicon diffused-meltback bar is shown in Figure 2, where the net impurity concentrations are plotted as a function of distance. The emitter region corresponds to the low-resistivity, undisturbed portion of the original silicon bar. Just at the emitter junction, the conductivity is slightly more n-type because of the depletion of the p-type impurities that diffused from the region. The junction from emitter-to-base is quite abrupt, since the diffusion of the n-type impurities is relatively negligible. This abrupt junction makes for good injection efficiency into the base. Because of the predominant diffusion of the p-type acceptors, the base layer is characterized by a graded impurity distribution approximating an error function. This introduces a "built-in" drift field which decreases the minority-carrier transit time, thereby increasing alpha-cutoff[3]. If we assume a minumum increase of at least a factor of two, then the theoretical alpha-cutoff is given by[4]

$$\omega_{CO} = 2\left(\frac{2.43 D_n}{W^2}\right) \qquad (2)$$

where D_n is the diffusion constant for electrons, and W is the base width. Letting D_n = 20 cm^2/sec for p-type silicon and W = 2.5 microns, equation (2) yields an alpha-cutoff frequency equal to 248 megacycles. The effects of emitter and collector capacitances and base resistance, however, limit the measured frequency cutoffs to lower values.

Also, in reference to Figure 2, the effect of the higher resistivity "plateau" in the collector region adjacent to the base is to cause the collector space-charge barrier to spread more into the collector than into the base. As a result, it is a good assumption that both the collector barrier capacitance and breakdown voltage are determined primarily by the collector resistivity. Although the latter is in the order of an ohm-cm. or so, the overall series collector resistance is kept low because of the rapid decrease of resistivity beyond the "plateau".

DEVICE FABRICATION

After the diffusion cycle the silicon npn bars are usually covered with a p-type "skin" due to the diffusion of the p-type acceptors to the surface. This is removed easily by chemical etching (CP4), which also prepares the bar for lead attachment. Ohmic emitter and collector contacts are made to the bar by alloying donor-doped gold at each end, backed up by metal ribbon for rigid mechanical support of the bar. The end lead configuration is clearly shown in the photograph of Figure 3, which is a view of the completed transistor before capping. The base connection consists of a thin, aluminum ribbon which is alloyed directly on the p-region. The aluminum, being an acceptor impurity, makes a p-type contact and therefore does not short out the transistor. Ribbon is used to provide a line contact for reduced base resistance, and great care is applied to minimize overlap on either side of the base. Figure 4 shows a photo-micrograph of a cross-sectioned silicon bar showing also the base connection. Note, in particular, the thick regrowth layer which represents recrystallized silicon, heavily doped with aluminum.

The 4JD4A silicon transistor is packaged in the new, round header shown in the photograph of Figure 3. This header has been designed in accordance with JETEC standards for case dimensions for automatic insertion into printed-board assemblies. The unit is completed with the welding of a steel cap to the header to assure a perfect hermetic seal. The final assembly is painted to withstand 200°C storage temperatures and a 96 hour salt-spray test.

HIGH FREQUENCY CHARACTERISTICS

Two parameters with which the applications engineer are intimately concerned are the common base and common emitter current gains, h_{fb} and h_{fe} respectively. The frequency dependence of alpha is shown in Figure 5. The alpha variation is seen to be markedly dependent upon emitter bias. The greater fall off of alpha with frequency at the lower levels may be attributed to a reduction in the high frequency emitter efficiency due to the emitter junction capacitance. If the emitter efficiency at low frequencies is close to unity then it can be shown that the high frequency emitter efficiency is inversely related to the product of the emitter junction capacitance and AC emitter resistance, kT/qI_E. Since the emitter resistance is also inversely proportional to emitter current, it would be expected that this degradation in emitter efficiency would be less pronounced as the current level is increased. However, as the current level is increased further the modulation of base resistivity significantly influences the emitter efficiency reducing it once more. The observed variation of alpha with frequency and emitter current behaves in the manner suggested by the above argument. This explains the behavior of the alpha cutoff frequency variation with emitter current which increases rapidly with current reaching a maximum in the range of from two to four milliamperes and then slowly falling off.

A typical variation of common emitter current gain, "beta", with frequency for different collector currents is shown in Figure 6. At increased bias currents the fall off of beta with frequency becomes less pronounced. This is understandable when one considers that the beta cut-off frequency is roughly proportional to the alpha cut off frequency divided by the dc beta. As we have shown, f_{ab} increases with emitter current reaching a maximum in the neighborhood of 3 ma and then decreases fairly slowly as the collector current is increased further. Beta on the other hand decreases more rapidly with collector current above 3 ma. Consequently the frequency variation of beta becomes less pronounced with higher collector current.

The behavior of common emitter power gain for both bias and frequency are shown in Figures 7 and 8. Figure 7 shows the dependence of power gain with emitter current. These are measurements made at 5 mc and at a collector voltage of 10 volts. The power gain peaks in a range of from 2 ma to 3 ma. As indicated earlier, the alpha cut off frequency maximized in the same range. It is known that the base spreading resistance, r_b', decreases with emitter current as a result of the base crowding effect which takes place with increasing emitter current. Since the emitter resistance also

decreases with emitter current, both effects tend to increase power gain. However, the reduction in emitter efficiency at higher currents will appreciable affect the power gain and most likely accounts for the power gain reduction observed above 3 ma.

Figure 8 shows the variation of power gain with frequency. As indicated by the measurements above 1 mc. the common emitter power gain varied with frequency at a rate of about 4 db per octave. This is in good agreement with the theoretical behavior of common emitter power gain with frequency which was shown by R. L. Pritchard to be, for a grown junction transistor[5]

$$G_e \approx \frac{.2\,\omega_c^{1/2}}{\omega^{3/2} C_c (r_b' r_e)^{1/2}} \quad \text{for } .2 < \omega/\omega_c < 2 \text{ and } \left[\frac{r_b' \omega}{r_e \omega_c}\right]^{1/2} > 1 \qquad (3)$$

Where ω_c = radian alpha cut off frequency
r_b' = base spreading resistance
r_e = emitter resistance
C_{ob} = collector-base barrier capacitance

and corresponds to a 4.5 db variation per octave. The above expression also points out the important dependence of power gain with r_b'. The collector capacity, C_{ob}, and the high frequency reverse voltage transfer ratio, h_{rb}, provide an index of the frequency capabilities of the device. Measurements of h_{rb} with frequency have shown it to be fairly linear with frequency in the one megacycle range. As a result of this linear behavior, it can be said to be proportional to the product of the base spreading resistance, r_b', and collector capacity, C_{ob}, and may be approximated by the expression

$$h_{rb} \approx j\omega C_{ob} r_b' \qquad (4)$$

Subatituting the typical values of 0.06 for h_{rb} and 14 uuf for C_{ob} into the equation, r_b' is calculated to be in the order of 680 ohms. This value may be somewhat higher than desirable for optimum amplifier performance in that it can limit the power gain to be expected from the transistor. However, this is not an inherent limitation of the device for r_b' can be lowered by one of a number of techniques including heavier doping of the base region, or the widening of the base region.

In examining the distribution of parameters, the common emitter or beta cut-off frequency was found to center at approximately 700 kc. If the units are divided into two groups on the basis of their beta cut-off frequency, those with a $f_{\alpha e}$ greater than one megacycle and those equal to or less than one megacycle, then these subpopulations have two distinctly different centers of distribution of power gain. The lower beta cut-off units have a power gain distribution centering about 12.5 db where-as the power gain of the higher beta cut off units centers about 16 db.

SMALL SIGNAL PARAMETERS - LOW FREQUENCY BEHAVIOR

Typical values for the small-signal hybrid parameters are listed in Table II below. These include values for both the common emitter and common base configuration and represent data obtained from more than 1000 transistors. The measurements were made at one kilocycle.

TABLE II

Parameter	Bias	Value
h_{ib}	V_{CB}=5v, I_E= -1 ma, f = 1 KC	55 ohms
h_{fb}	V_{CB}=5v, I_E= -1 ma, f = 1 KC	.965
h_{rb}	V_{CB}=5v, I_E= -1 ma, f = 1 KC	4 x 10^{-4}
h_{ob}	V_{CB}=5v, I_E= -1 ma, f = 1 KC	0.6 u mho
h_{rb}	V_{CB}=5v, I_E= -1 ma, f = 1 mc	6 X 10^{-2}
h_{ie}	V_{CB}=5v, I_E= -2 ma, f = 1 KC	640 ohms
h_{fe}	V_{CB}=5v, I_E= -2 ma, f = 1 KC	30
h_{re}	V_{CB}=5v, I_E= -2 ma, f = 1 KC	6 X 10^{-4}
h_{oe}	V_{CB}=5v, I_E= -2 ma, f = 1 KC	18 u mho

The variation of the common base hybrid parameters with emitter current is shown in Figure 9 in which the data was plotted relative to the value at an emitter current of 1 ma.

DC CHARACTERISTICS

An important set of characteristics for any transistor are the collector characteristics shown by figure 10. This is a plot of the collector current with collector voltage for different levels of base current.

One of the very useful pieces of information which can be obtained from these characteristics is the series saturation resistance. This resistance, designated by the symbol R_{sc}, is a measure of the collector to emitter voltage necessary to sustain a given collector current for some predetermined base current. R_{sc} is generally defined as the slope of a line from the origin to a given intercept on the saturation region of the V_c - I_c characteristics. On many devices, particularly germanium and alloy transistors, the saturation region is fairly linear and does intercept the origin, thus providing a measure of saturation resistance which is consistent and coincides identically with the previously mentioned definition. However, this is not true for the 4JD4A nor for many other silicon grown junction devices. The curves do not generally intercept the origin and are not quite as linear in the saturation region. Consequently, R_{sc} will vary with the point of operation and must be specified for a given collector and base current. Although the error may be small, a more consistent description would

be to restrict the definition of R_{sc} without ambiguity and would be useful to the circuit designer interested in ac operation. The necessary additional information could then be given in terms of the more truly descriptive term, the collector saturation voltage, V_{CE} (SAT) identified with a given collector and base current. Referring to Figure 10 the series saturation resistance on the basis of the above definition would be the slope of the envelope of the characteristic in saturation region. A typical value of saturation voltage, V_{CE} (SAT), for the 4JD4A is 200 millivolts, measured at I_B = 1 ma I_C =5 ma, which is equivalent to a saturation resistance of 40 ohms.

The crowding of the collector characteristics with base drive represents the beta hold-up with collector current for the transistor. Figure 11 shows a typical variation of dc beta with current. Here we see that beta rises rapidly with current maximizing in the range of 1 to 3 ma collector current and then falls off at higher current levels. This degradation of beta hold-up at the higher values of collector current is due to a combination of factors, a reduction in emitter efficiency, base crowding effect, and poor injection efficiency at the base lead contact. Although this type of characteristic is representative of the device as it is now being produced a number of 4JD4A transistors were found with beta hold-up characteristics that was essentially flat for collector currents ranging from one to forty milliamperes.

TEMPERATURE DEPENDENCE

Figure 12 shows the variation of the common base "h" parameters with temperature. These curves which represents typical behavior of the 4JD4A are normalized with reference to the values at room temperature, 25°C. It is seen that for the most part these parameters do not markedly deviate from their room temperature values below about 130°C. Above this temperature, however, a rather sharp rate of change is observed in all but h_{ib}.

The variation of breakdown voltage with temperature is interesting. Theoretically the junction breakdown voltage should increase with temperature in accordance with McKay's expression[6]

$$BV_{T_1} = BV_{T_0}\left[1 + B(T_1 - T_0)\right] \qquad (5)$$

where B is a constant of the order of 10-4 volts /°C, the exact value being a function of the junction grade. Measurements of the base to emitter breakdown, BV_{EBO}, and collector to base breakdown, BV_{CBO}, show an increase in breakdown voltage with temperature in accordance with this predicted variation. However, the collector to emitter breakdown voltage, BV_{CEO}, although exhibiting this increase below 100°C decreases fairly rapidly with temperature above 120°C. This can be explained when one considers the technique generally used to determine junction breakdown voltage which in essence involves measuring the voltage developed across the transistor junction under study, at a transfer current of 1 milliampere. When examining either the collector or emitter junction alone this method does provide a fairly reliable measure of the breakdown voltage because of the very sharp reverse characteristic associated with silicon junctions. This is not true, though, when the voltage stress is applied from emitter to collector. Under these conditions, since there is no base connection, the transfer current consists solely of the leakage current amplified by a $(1 - \alpha)$ term. To illustrate this, the emitter current may be written as

$$I_E = I_C + I_L = \alpha I_E + I_L \qquad (6)$$

where I_L = leakage current. Since there is no base connection in this test, it is reasonable to assume that the total transfer current I equals I_E and rewriting

$$I = \frac{I_L}{1 - \alpha} \qquad (7)$$

Leakage current increases rapidly with temperature and can become appreciable above 100°C. Furthermore, alpha also tends to increase with temperature so that the combination can give rise to fairly large transfer currents which also increase with temperature. Thus, as the temperature increases, the voltage necessary to support a given leakage current would decrease. The BV_{CEO} that was recorded is, therefore, most probably, not a true breakdown voltage but rather a measure of that voltage and temperature at which the amplified leakage current equals one milliampere. True breakdown, undoubtedly, occurs at a higher voltage. However, from an application standpoint this quasi-breakdown voltage is still significant, for it provides the circuit designer with a very real voltage limitation when operation in a common emitter configuration.

The variation of I_{CO} with temperature is shown in Figure 13 for a collector to base voltage of 5 volts.

The variation of common emitter power gain with temperature is shown in Figure 14 and is seen to decrease with an increase in the ambient temperature. For a grown junction device power gain is proportional to the square root of the product of the lattice mobilities. Inasmuch as the lattice mobility is also proportional to $(1/T)^x$, the power gain will decrease with temperature as shown.

CONCLUSIONS

The 4JD4A silicon transistor exhibits extremely good high frequency characteristics, which together with its low saturation resistance

of 40 ohms makes it particularly attractive for switching applications as well as for linear amplifier use.

CORRECTION

Frequency scale in Figure 6 is incorrect. However, the indicated alpha cutoff frequencies for the curves are correct.

REFERENCES

1. Lesk, I. A. - Grown-Diffused Germanium and Silicon Transistors for High Frequency Operation, presented at AIEE - IRE Semiconductor Device Research Conference, Purdue University, June 1956.

2. Hall, R. N. - Melt-Back Transistors, presented at AIEE - IRE Semiconductor Device Research Conference, University of Pennsylvania, June 1955.

3. Moll, J. L. and Ross, I. M. - Dependence of Transistor Parameters on the Distribution of Base Layer Resistivity, Proc. IRE, Vol.44, pp. 72 - 78, January 1956.

4. Pritchard, R. L. - Frequency Variations of Current-Amplification Factor for Junction Transistors, Proc. IRE, Vol. 40, pp. 1476 - 1481, November 1952.

5. Pritchard, R. L. - High Frequency Power Gain of Junction Transistors, Proc. IRE, Vol. 43, pp. 1075 - 1085 - 1955

6. McKay, K. G. - Avalanche Breakdown in Silicon, Physical Review, Vol. 94, pp. 877 - 884, May 1954

GENERAL ELECTRIC TYPE 4JD4A SILICON NPN TRANSISTOR*

HIGH-FREQUENCY CHARACTERISTICS:

PARAMETER	SYMBOL	TYPICAL VALUES
ALPHA-CUTOFF FREQUENCY	$f_{\alpha b}$	25 MEGACYCLES
COMMON EMITTER POWER GAIN	G_e	13 DB AT 5 MEGACYCLES
COLLECTOR CAPACITANCE	C_C	14 $\mu\mu$f
VOLTAGE FEEDBACK FACTOR	h'_{rb}	60 X 10-3

DC CHARACTERISTICS:

PARAMETER	SYMBOL	TYPICAL VALUES
COMMON EMITTER CURRENT GAIN	h_{FE}	30
COLLECTOR SATURATION RESISTANCE	R_{SC}	40 OHMS
COLLECTOR LEAKAGE CURRENT	I_{CO}	.01 MICROAMPS AT 5V
COLLECTOR-TO-BASE BREAKDOWN VOLTAGE	BV_{CBO}	60 VOLTS
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE	BV_{CEO}	30 VOLTS
EMITTER-TO-BASE BREAKDOWN VOLTAGE	BV_{EBO}	7 VOLTS

* MEASURED AT 25°C

Table 1

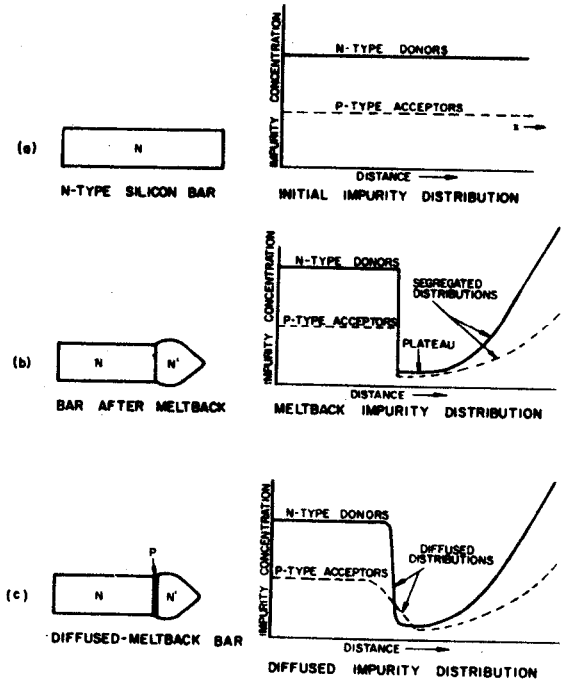

Fig. 1
Impurity distributions at each step of the silicon diffused - meltback process.

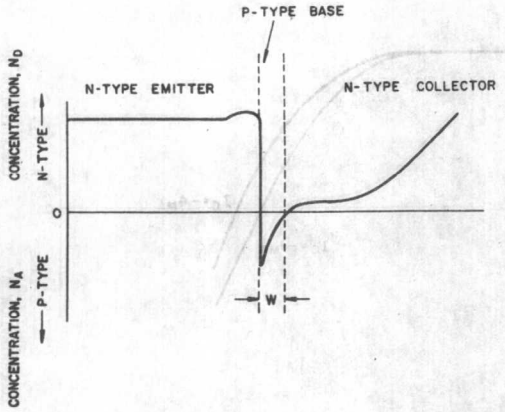

Fig. 2
Net impurity concentrations for silicon diffused - meltback bar.

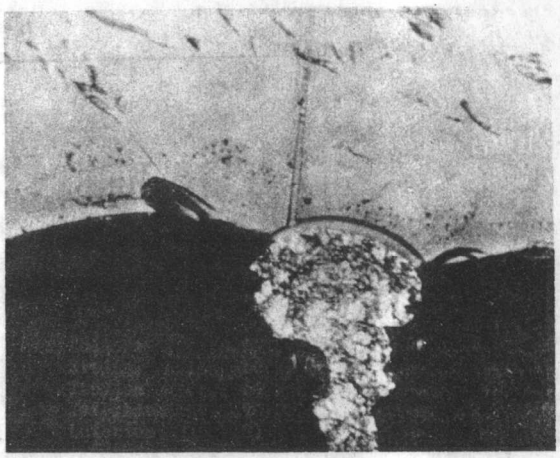

Fig. 4
Photomicrograph of cross-sectioned bar showing base region and aluminum base contact.

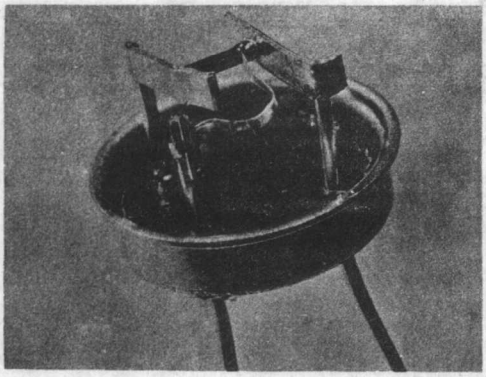

Fig. 3
Uncapped view of completed silicon diffused - meltback transistor.

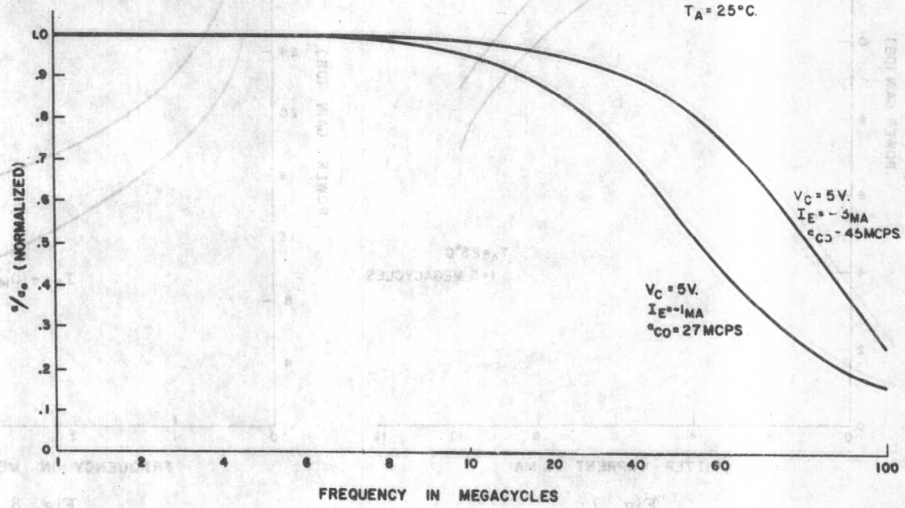

Fig. 5
Variation of alpha with frequency.

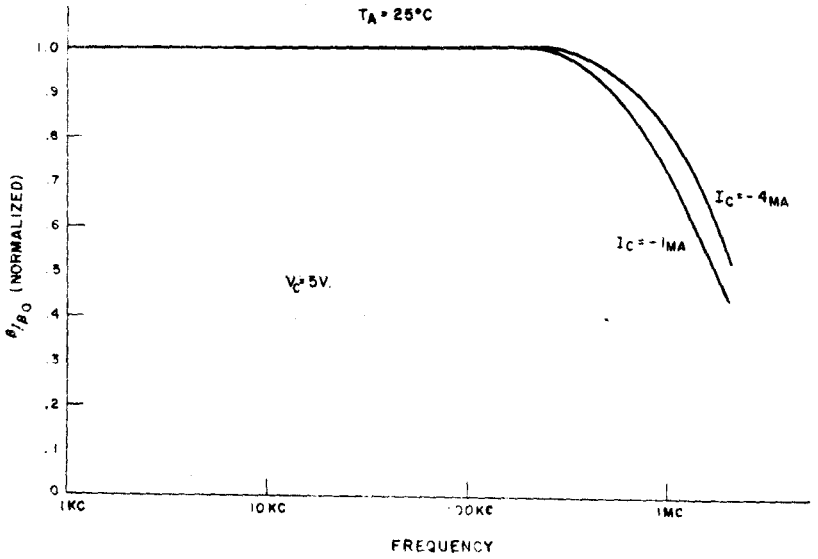

Fig. 6
Variation of beta with frequency.

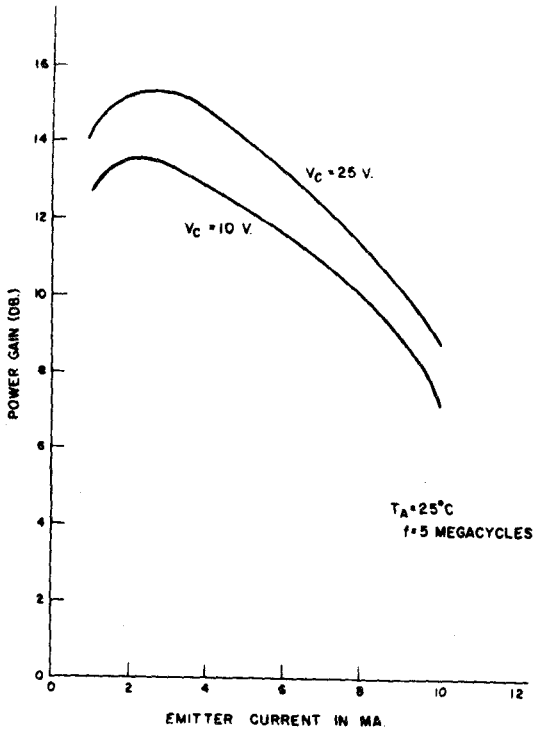

Fig. 7
Variation of grounded emitter power gain with bias.

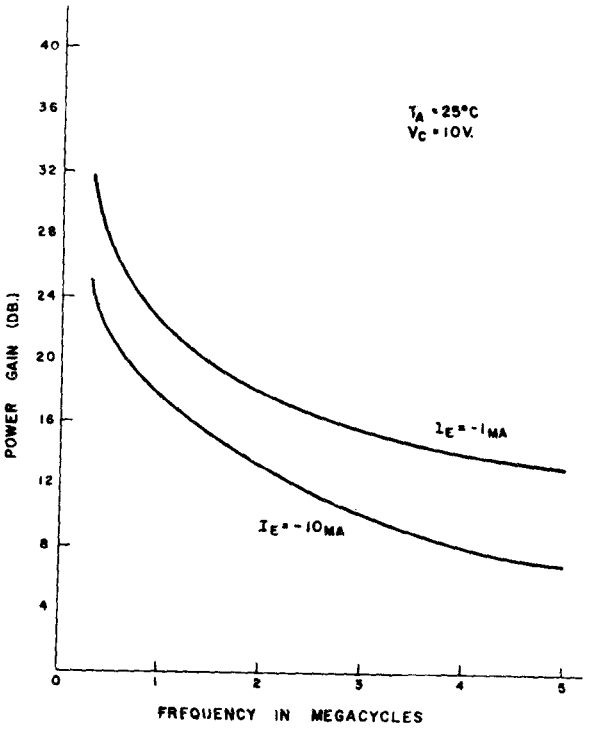

Fig. 8
Variation of grounded emitter power with frequency.

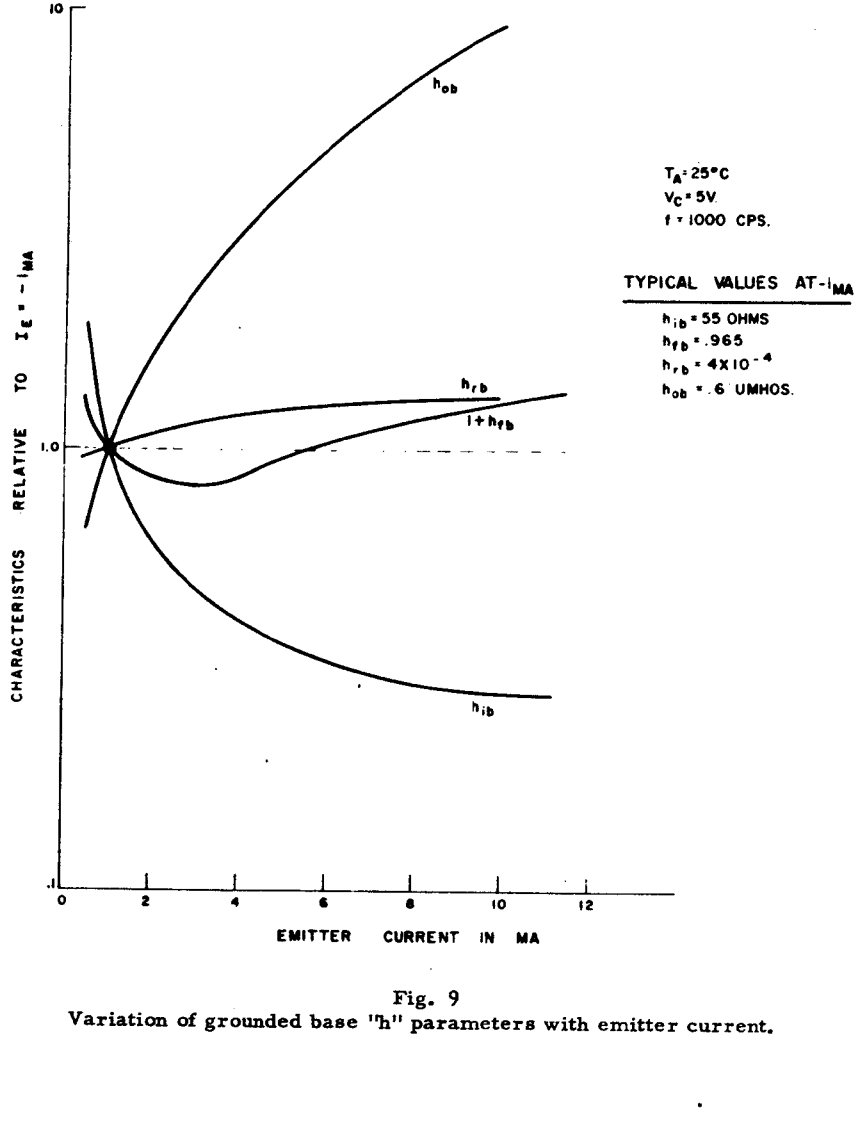

Fig. 9
Variation of grounded base "h" parameters with emitter current.

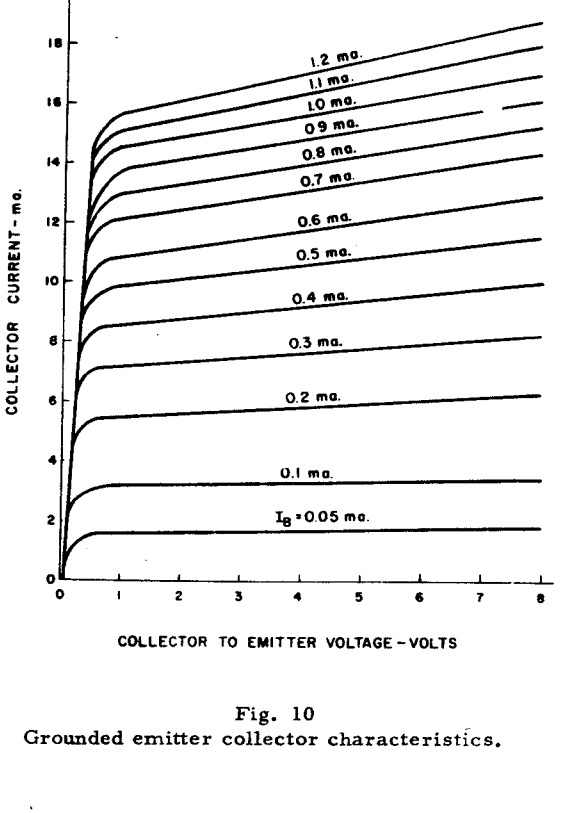

Fig. 10
Grounded emitter collector characteristics.

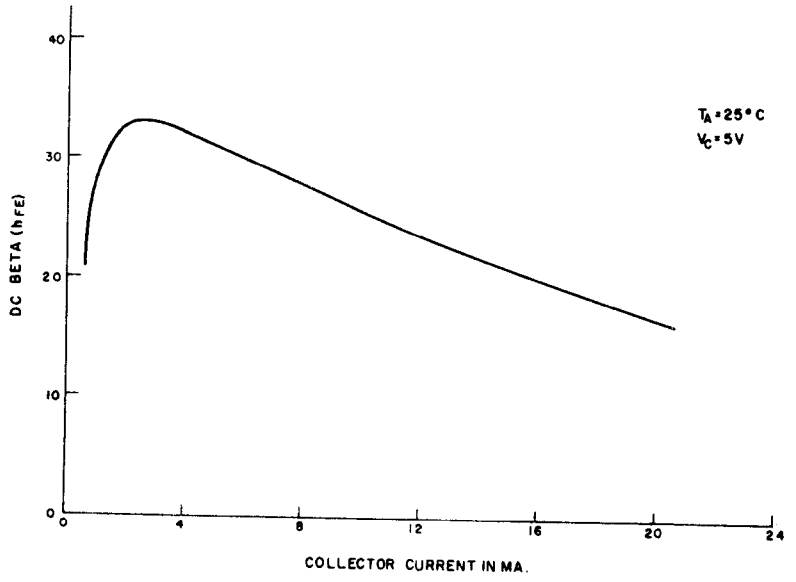

Fig. 11
Variation of DC beta with current.

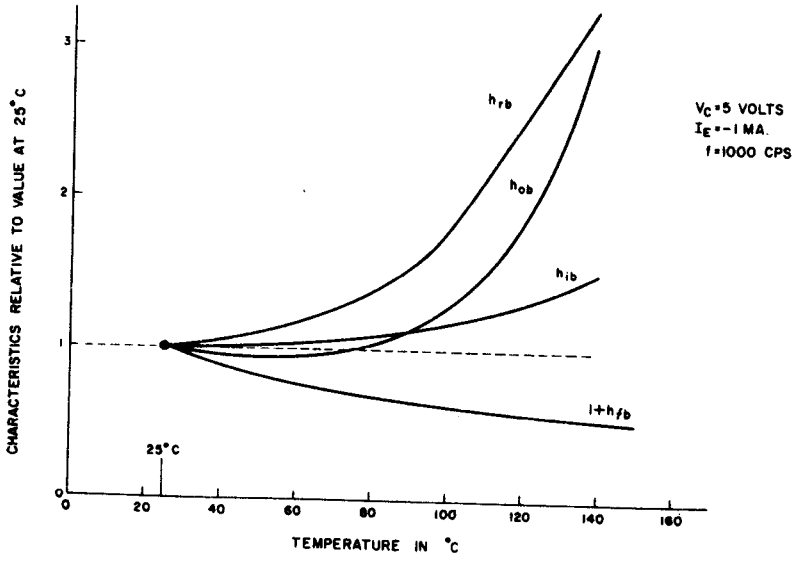

Fig. 12
Variation of grounded base "h" parameters with temperature.

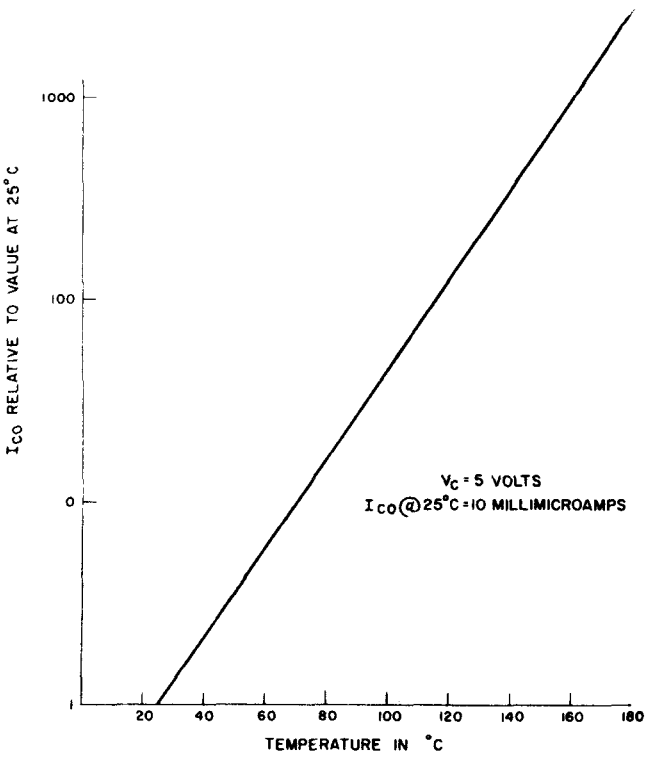

Fig. 13
Variation of I_{co} with temperature.

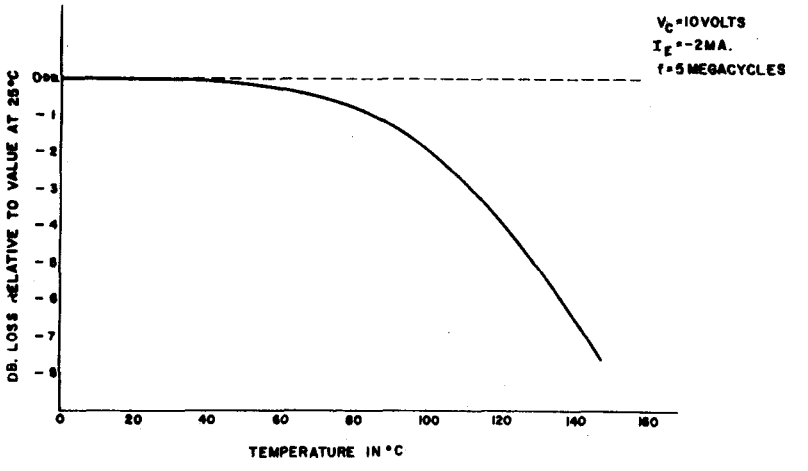

Fig. 14
Variation of grounded emitter power gain with temperature.

NOISE FIGURES IN SEMICONDUCTOR DIELECTRIC AMPLIFIERS+

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Introduction

Dielectric amplifiers[1,2] circuits utilize a non-linear capacitor in conjunction with other circuit elements to obtain amplification or control. In all dielectric amplifiers a low frequency control signal acts to modify the average impedance presented by the non-linear capacitor to a high frequency or carrier current. Variations in the carrier voltage resulting from impedance changes of the non-linear capacitor are rectified and constitute the amplifier output which is, consequently, directly related to the low-frequency control signal but at a higher power level.

Recent interest in dielectric amplifiers has been stimulated by the desire to obtain an amplifier with the reliability characteristics of solid-state devices, but with a very high input impedance at audio frequencies. The dielectric amplifier input impedance at audio frequencies without feedback can be made as high as about 100 megohms, whereas present solid state or transistor amplifiers have a maximum input impedance of the order of one megohm.

Two types of non-linear capacitors have been used in dielectric amplifiers - barium-strontium titanate capacitors[1] and, more recently, the junction capacitance of reversed-biased germanium and silicon diodes.[3] In barium-strontium titanate capacitors the capacitance non-linearity arises at high electric field strengths, close to rupture strengths. Consequently, when a barium-strontium titanate capacitor is used in a dielectric amplifier corona tends to develop at the edges and in internal voids as a result of the high electric fields necessary for proper operation of the amplifier. Noise associated with the corona and internal breakdown of the titanate capacitor is so erratic in both time and magnitude that no quantitative results can be given for the noise figure of the dielectric amplifier; indeed the noise level has been found often to be so high that noise figure is not worth investigating.

In contrast reverse-biased semiconductor junction diodes may be operated as non-linear capacitors in an entirely satisfactory manner at low voltages and are not subject to corona or other breakdown difficulties. Their noise figure is therefore of some interest.

This paper describes the results of a study of this noise figure.

Part I - Circuit Design in Dielectric Amplifiers

Dielectric amplifiers utilize impedance changes resulting from the changes in reactance of a non-linear capacitor to control the amplitude of a high-frequency carrier which is subsequently rectified. Series or parallel LC circuits resonant at the carrier frequency are employed to increase the sensitivity of the carrier output to small capacitance variations resulting from the input signal. There is no reason to expect major differences in performance of the two types of amplifier circuits other than convenience in design. This paper is concerned with a single circuit, that of Figure 1.

In the circuit of Figure 1, L_o and C_d comprise the series circuit resonant at the carrier frequency. C_d is the non-linear capacitor whose average impedance to the carrier is determined by the input signal. The capacitor, C_o, prevents the fixed bias, V_o, from disturbing the operation of the detector circuit and isolates the input terminals to prevent input impedance from dependence solely on the inductance, L_o, and the internal impedance of the carrier source. L_1 serves to isolate the input circuit from the carrier circuit at the frequency of the carrier.

The instantaneous value of the diode-junction capacitance is determined by the junction voltage in a manner which has been discussed in detail by Dill.[3] The input signal and the

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carrier appear across the diode junction and thereby determine the instantaneous junction capacitance. The average junction capacitance presented to the input signal is undisturbed by the carrier signal because the carrier signal is very high in frequency; however, the capacitance at the carrier frequency is changed by the input signal. Variation in the average junction capacitance as a function of the input signal causes the carrier amplitude to vary as a function the input signal. Consequently, the output, which is the detected carrier amplitude, varies with the input, and the circuit acts as an amplifier. The relationship is nearly linear and can be entirely so for small signals.

The selection of the carrier frequency and the value of L_o in this amplifier circuit are determined by the value conveniently obtainable for the junction capacitance, C_d. Typical commercially available junction diodes with high back resistances and, therefore, suitable for high-impedance amplifiers have a junction capacitance of 5-10 micromicrofarads. As much junction capacitance as desired may be obtained by utilizing multiple diodes in parallel at the expense of reduced input impedance. For convenience in the study of noise figure reported here it was considered desirable to use a moderately low carrier frequency and consequently multiple diodes were to obtain larger values of capacitance than would be employed in an amplifier in which input impedance was actually maximized. The diode unit employed comprised five IN158 germanium junction diodes in parallel. Substantially larger values of back resistance are, of course, to be found in silicon diodes which are now available. Such diodes were not available, however, at the initiation of this particular study.

A curve of the capacitance of the multiple diode unit (in the back biassed direction) is shown in Figure 2.

Noise Figure Measurements

Noise figure was measured by a substitution method. The experimental arrangement is shown in Figure 3. The output of the single stage dielectric amplifier was naturally too low for direct measurement. Consequently the output of the dielectric amplifier was fed into a low-noise amplifier to raise its level to a suitable value for a wave analyzer. The wave analyzer used had a four cycle per second bandwidth. The four cycle band of noise from the wave analyzer was fed into a cathode-follower which served to match the impedance of the wave analyzer to a thermocouple indicating device.

Noise output power of the dielectric amplifier was measured by recording the deflection on an output meter for various values of resistance at the amplifier input. Absolute calibrations were obtained with a continuous-wave standard signal generator substituted for the resistor at the amplifier input. The continuous-wave r.m.s. voltage that was equivalent to the r.m.s. noise voltage appearing at the amplifier output was used to calculate the square of the r.m.s. value of the output noise per cycle with the expression:

$$\overline{e_{no}^2} = \frac{\overline{V_{nc}^2}}{d_f}$$

in which Vnc = voltage of continuous wave standard signal generator r.m.s.
d_f = Bandwidth of the noise signal
e_{no}^2 = r.m.s. output noise voltage squared

Amplifier output noise power per cycle P, is then; $P = \overline{e_{no}^2}/R_L$, in which R_L is the output load resistance. Noise power in the output originating from the thermal noise of the source was determined by determining the voltage gain of the amplifier with a continuous-wave generator and then calculating the noise power per cycle, Ps, due to the thermal noise of the source with the expression:

$$P_s = \frac{4KTR_oG^2}{R_L}$$

in which R_L is the source resistance and G is the voltage gain of the amplifier. The noise figure, F, is then:

$$F = \frac{P}{P_s} = \frac{\overline{V_{nc}^2}}{4KTR_oG^2d_f}$$

This procedure for measuring noise figure was advantageous because an input signal to the amplifier was not required during the noise measurement itself. Use of a standard input signal to the amplifier during noise measurement tends to limit the measurements to cases in which the source impedance of the amplifier is somewhat less than 0.5 megohms because of the low impedances of standard signal sources and the difficulty of applying transformers to modify source impedances to megohm values.

Results of the measurements of the output noise power of the dielectric amplifier are shown in Figure 4. The signal source resistance was varied for the different sets of noise data to determine the dependence of the amplifier output noise power on the source resistance. As can be seen from the curves of Figure 4, the amplifier output noise decreases with decreasing source resistance and increasing frequency.

Noise power in the output of the dielectric amplifier resulting from the thermal noise of the source resistance was calculated after determining the amplifier gain.

Using the results of the measurements of the output noise power and the calculated output noise power due to the thermal noise of the source resistance the noise figure of the dielectric

amplifier was calculated. Figure 5 shows the noise figure of the dielectric amplifier as a function of frequency for various values of the source resistance, R_1. Such curves permit determination of the optimum value of source resistance since as source resistance is reduced the noise figure decreases until a critical value is reached. Further reduction results in an increase in noise figure. The data of Figure 5 are applicable to determination of optimum source resistance at signal frequencies of 1.5 kilocycles and above.

From the data presented the conclusions that can be drawn are; 1) noise figure decreases as frequency increases 2) the noise figure is a function of source resistance, and 3) there exists an optimum source resistance to minimize the noise figure, and this optimum resistance is different for every frequency. A more thorough explanation of the parameters governing the noise figure resulted from an investigation of the sources of noise and the representation of these sources in an equivalent circuit which are described in the next section.

Noise Sources and Equivalent Circuit

The general characteristics of noise in junction devices have been reported in the literature [4]. An investigation of the particular noise characteristics of the composite five unit diode was made prior to investigation of the influence of these characteristics in dielectric amplifier applications. The equivalent-circuit parameters of the diode shown in Figure 6a were evaluated before noise measurements were taken.

Noise measurements on the diode employed the same equipment used to measure the amplifier noise figure, Figure 3, with the input to the low-noise amplifier of the noise measuring equipment connected to the circuit shown in Figure 6b. R_o in Figure 6b was varied to determine the effect of this resistance on the diode noise output and V_1 was varied for different measurements to find the dependence of the diode noise on reverse bias.

In Figure 7 all the noise measurements taken on the set of junction diodes for three values of bias are consolidated. The shaded areas represent all the measurements taken at a particular value of bias by varying R_o. The open circuit noise voltage, $\overline{e_{no}^2}$, was obtained from measurements of $\overline{e_n^2}$ by the equation relating $\overline{e_n^2}$ to $\overline{e_{no}^2}$ which is

$$\overline{e_n^2} = \frac{R^2\,\overline{e_{no}^2}}{(R+R_d) + \omega^2 R^2 R_d^2 (C_a + C_d)}$$

in which

$$R = \frac{R_a R_o}{R_a + R_o}$$

Subscript a refers to low-noise amplifier components.

The agreement of the noise data taken at a particular value of bias corresponding to five values of R_o with no more descrepancy than that represented by a band 3db wide when used to determine $\overline{e_{no}^2}$ suggests the reliability of (1) the value obtained for R_d, (2) the general measuring technique in that results are repeatable, and (3) the placing of the diode noise generator in the resistance branch of the equivalent circuit.

The next question that arises is "does the noise originating in the diodes act as any other signal in changing the junction capcaitance of the diode?" This question has a bearing on the extent to which the diode noise influences the output of the dielectric amplifier. Referring to Figure 1 it can be seen that the output of the dielectric amplifier is taken across L_o and the internal impedance of the carrier source. Both of these have an impedance of less than ten ohms over the audio frequency band; whereas, C_o, which is in series with the combination of L_o and the carrier source impedance and acts as a voltage divider for any audio signal originating in the diode, has an impedance greater than 10^5 ohms over the audio frequency band. Thus for all practical purposes the point at which the output of the dielectric amplifier is taken is at ground potential for any audio signal originating in the diode, and as a result, any audio signal, such as noise originating in the diode can only affect the output of the dielectric amplifier by changing the junction capacitance.

It has been found necessary to assume that the diode noise generator acts in series with the diode dynamic resistance, R_d, in order to obtain calculated values consistent with noise measurements on both the diodes and dielectric amplifier. When the diode noise generator is in series with the dynamic resistance, R_d, a decrease in R_o decreases the noise appearing across the junction capacitance, C_d, and thus decreases the noise power output of the dielectric amplifier. This result is in agreement with noise measurements taken on the dielectric amplifier. If the noise generator were placed in series with the junction capacitance or in series with the parallel combination of junction capacitance and dynamic resistance, decreasing R_o would increase the noise appearing across the junction capacitance. Increasing the noise voltage appearing across the junction capacitance increases the noise power output of the dielectric amplifier which is contrary to the effect observed in dielectric amplifier noise measurements.

Noise measurements on the diode indicate that the noise originating in them behaves as 1/f over the audio frequency range; however, noise measurements on the dielectric amplifier indicate noise independent of frequency for frequencies above 1kc and low values of R_o.