PROCEEDINGS

1997 INTERNATIONAL SYMPOSIUM ON LOW POWER ELECTRONICS AND DESIGN

Doubletree Hotel *Monterey, CA*

August 18 – 20, 1997

Sponsored by:

ACM SIGDA

IEEE Circuits and Systems Society

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WELCOME

Welcome to the 1997 International Symposium on Low Power Electronics and Design. This is the second year of this symposium, which is the result of a merger between the Symposium on Low Power Electronics and the International Symposium on Low Power Design. Like its predecessors, the symposium contains a mix of invited talks and contributed papers. All invited talks will be in plenary sessions, and thus can be heard by all attendees. Most other sessions will consist of two parallel tracks: one focusing on systems and CAD, the other focusing on circuits and technology.

A total of 102 contributed papers were received. This strong response attests to the continuing level of interest in low power design across the international VLSI technical community. Many thanks to the authors who submitted papers, which report significant advances in the domain of low power electronics and design. Even with the parallel sessions, we were able to accept only 42 regular papers. In addition to regular papers presented orally, we have accepted 17 poster papers that will be displayed in two poster sessions scheduled during extended breaks, so that attendees can visit all poster papers of interest to them.

The plenary sessions will be highlighted by invited talks, six in all, including two talks at the keynote session on the first day. There will also be a special talk at the banquet that evening by James Meindl, on the subject of the history of low power electronics, from his perspective of innovative participation in that history over the past several decades.

An evening panel session on the second day will feature the fictional company, Speedy Microsystems, and its contractor team of experts who are trying to design their next-generation multimedia microprocessor, with highly-demanding specs on power and performance. It should be a stimulating event of interest to all attendees.

For the first time, we will offer two half-day tutorials, one on low-voltage design techniques and another on CAD methodologies. These tutorials will present techniques employed currently in industry as well as future trends.

Many thanks to the program committee for doing an excellent job of paper selection and session organization. Thanks also to the panel organizers and panelists for what should prove to be an enlightening and entertaining evening session. We thank Lew Terman for his continuing assistance in preparations for the conference. Finally, we want to thank the ACM SIGDA and the IEEE Circuits and Systems Society for their sponsorship, and the IEEE Solid-State Circuits Society for their technical co-sponsorship and technical support.

We hope you will find the symposium both stimulating and helpful. Please give us your comments and suggestions on any aspects of the conference.

Brock Barton, Massoud Pedram
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TABLE OF CONTENTS

Keynote Session

Chair: Brock Barton

Low-Power CMOS Design through V_{TH} Control and Low-Swing Circuits
Takayasu Sakurai, Hiroshi Kawaguchi, Tadahiro Kuroda 1

Session M1
Digital Circuit Techniques

Chair: Dan Dobberpuhl, Digital Equipment Corp

M1.1 **Survey of Low Power Techniques for ROMs**
Edwin de Angel, Earl E. Swartzlander, Jr. 7

M1.2 **High-Performance, Low-Power Design Techniques for Dynamic to Static Logic Interface**
June Jiang, Kan Lu, Uming Ko 12

M1.3 **LVDCSL: Low Voltage Differential Current Switch Logic, A Robust Low Power DCSL Family**
Dinesh Somasekhar, Kaushik Roy 18

Session M2
System Level Power Optimization

Chair: Jason Cong

M2.1 **System-Level Power Optimization of Special Purpose Applications: The Beach Solution**
Luca Benini, Giovanni De Micheli, Enrico Macii, Massimo Poncino, Stefano Quer 24

M2.2 **Formalized Methodology for Data Reuse Exploration in Hierarchical Memory Mappings**
J. Ph. Diguet, S. Wuytack, F. Catthoor, H. De Man 30

M2.3 **A Low-Power Design Method Using Multiple Supply Voltages**
Mutsunori Igarashi, Kimiyoshi Usami, Kazutaka Nogami, Fumihiro Minami, Yukio Kawasaki, Takahiro Aoki, Midori Takano, Chiharu Mizuno, Takashi Ishikawa, Masahiro Kanazawa, Shinji Sonoda, Makoto Ichida, Naoyuki Hatanaka 36

Invited Talk

Chair: Sayfe Kiaei

Minimizing Power Dissipation of Cellular Phones
Sven Mattisson 42

Session M3
Wireless Communication Circuits

Chair: R.J. van de Plassche

M3.1 **A 1V, 5mW, 1.8 GHz Balanced Voltage-Controlled Oscillator with an Integrated Resonator**
Donald A. Hitko, Theodore L. Tewksbury, Charles G. Sodini 46

M3.2 **Δ–Σ Frequency-to-Time Conversion by Triangularly Weighted ZC Counter**
M. Høvin, S. Kiaei, T. S. Lande 52

Session M4
Register Transfer High-Level Synthesis

Chair: R. Iris Bahar

M4.1 **A Symbolic Algorithm for Low-Power Sequential Synthesis**
Balakrishna Kumthekar, In-Ho Moon, Fabio Somenzi 56

M4.2 **Low Power High Level Synthesis By Increasing Data Correlation**
Dongwan Shin, Kiyoung Cho 62

Session P1
Poster Sessions

Chair: Sayfe Kiaei

P1.1 **A Programmable Power-Efficient Decimation Filter for Software Radios**
Emad N. Farag, Ran-Hong Yan, Mohamed I. Elmasry 68

P1.2 **Techniques for Low Energy Software**
Huzefa Mehta, Robert Michael Owens, Mary Jane Irwin, Rita Chen, Debashree Ghosh 72

P1.3 **Low Power Multiplication for FIR Filters**
Chris J. Nicol, Patrik Larsson 76

P1.4 **Low-Power H.263 Video CoDec Dedicated to Mobile Computing**
Morgan H. Miki, Gen Fujita, Takao Onoye, Isao Shirakawa 80

P1.5 **Scheduling for Power Reduction in a Real-Time System**
Jason J. Brown, Danny Z. Chen, Garrison W. Greenwood, Xiaobo (Sharon) Hu, Richard W. Taylor 84

P1.6 **Engineering Change for Power Optimization Using Global Sensitivity and Synthesis Flexibility**
Premal Buch, Christopher K. Lennard, A. Richard Newton 88

P1.7 **Synthesis of Low-Power Asynchronous Circuits in a Specified Environment**
Steven M. Nowick, Michael Theobald 92

P1.8 **Quasi-Static Energy Recovery Logic and Supply-Clock Generation Circuits**
Yibin Ye, Kaushik Roy, Georgios I. Stamoulis 96

P1.9 **A New 4-2 Adder and Booth Selector for Low Power MAC Unit**
Bum-Sik Kim, Dae-Hyun Chung, Lee-Sup Kim 100

P1.10 **Enhanced Prediction of Energy Losses During Adiabatic Charging**
A. Schlaffer, J.A. Nossek 104

Session M5
Analog Circuit Techniques

Chair: Louis Williams

M5.1 **Charge-Pump Assisted Low-Power/Low-Voltage CMOS Opamp Design**
J. Zhou, R.M. Ziazadeh, H. Gao, H.-H Ng, H.-T. Ng, D.J. Allstot 108

M5.2 **A Low Voltage CMOS Current Source**
Detlev Schmitt, Terri S. Fiez 110

M5.3 **New Stability Criteria for the Design of Low-Pass Sigma-Delta Modulators**
J. A. E .P. van Engelen, R. J. van de Plassche 114

M5.4 **A Capacitor-Based D/A Converter with Continuous Time Output for Low-Power Applications**
Lapoe Lynn, Paul Ferguson, Jr. 119

Session M6
Register Transfer & Architectural Level Power Estimation

Chair: Rob Roy

M6.1 **Cycle-Accurate Macro-Models for RT-Level Power Analysis**
Qinru Qiu, Qing Wu, Massoud Pedram, Chih-Shun Ding 125

M6.2 **A Method of Redundant Clocking Detection and Power Reduction at RT Level Design**
Mitsuhisa Ohnishi, Akihisa Yamada, Hiroaki Noda, Takashi Kambe 131

M6.3 **Power Analysis of a 32-bit RISC Microcontroller Integrated with a 16-bit DSP**
R. S. Bajwa, N. Schumann, H. Kojima 137
M6.4 **Analytical Energy Dissipation Models for Low-Power Caches**
Milind B. Kamble, Kanad Ghose 143

Banquet Talk

Chair: Anantha Chandrakasan
History of Low Power Electronics: How It Began and Where It's Headed
James D. Meindl 149

Invited Talks

Chair:Massoud Pedram
Issues and Directions in Low Power Design Tools: An Industrial Perspective
Jerry Frenkil 152
System-Level Power Estimation and Optimization—Challenges and Perspectives
Jan M. Rabaey 158

Session T1
Low Power Signal Processing

Chair: Chuck Traylor
T1.1 **Dynamic Algorithm Transformations (DAT) for Low-Power Adaptive Signal Processing**
Manish Goel, Naresh R. Shanbhag 161
T1.2 **Low Power Motion Estimation Design Using Adaptive Pixel Truncation**
Zhong-Li He, Kai-Keung Chan, Chi-Ying Tsui, Ming L. Liou 167
T1.3 **Low Power Signal Processing Architectures for Network Microsensors**
Michael J. Dong, K. Geoffrey Yung, Wiliam J. Kaiser 173

Session T2
Logic-Level Power Estimation

Chair: Farid Najm
T2.1 **K2: An Estimator for Peak Sustainable Power of VLSI Circuits**
Michael S. Hsiao, Elizabeth M. Rudnick, Janak H. Patel 178
T2.2 **Switching Activity Estimation Using Limited Depth Reconvergent Path Analysis**
José C. Costa, José C. Monteiro, Srinivas Devadas 184
T2.3 **Composite Sequence Compaction for Finite-State Machines Using Block Entropy and High-Order Markov Models**
Radu Marculescu, Diana Marculescu, Massoud Pedram 190

Session T3
Memory Techniques

Chair: Ingrid Verbauwhede
T3.1 **Reducing TLB Power Requirements**
Toni Juan, Tomas Lang, Juan J. Navarro 196
T3.2 **Exploiting the Locality of Memory References to Reduce the Address Bus Energy**
Enric Musoll, Tomás Lang, Jordi Cortadella 202
T3.3 **An Extended Addressing Mode for Low Power**
Atul Kalambur, Mary Jane Irwin 208

Session T4
Signal Processing Digital Circuits

Chair: Rick Carley

T4.1 **Minimizing Energy Dissipation in High-Speed Multipliers**
Rafael Fried 214

T4.2 **A One Division per Clock Pipelined Division Architecture Based on LAPR (Lookahead of Partial-Remainder) for Low-Power ECC Applications**
Hyung-Joon Kwon, Kwyro Lee 220

T4.3 **Power Reduction Techniques for a Spread Spectrum Based Correlator**
David Garrett, Mircea Stan 225

Session P2
Poster Session

Chair: Anantha Chandrakasan

P2.1 **A Sequential Procedure for Average Power Analysis of Sequential Circuits**
Li-Pen Yuan, Sung-Mo Kang 231

P2.2 **Energy Delay Measures of Barrel Switch Architectures for Pre-Alignment of Floating Point Operands for Addition**
R. V. K. Pillai, D. Al-Khalili, A. J. Al-Khalili 235

P2.3 **Analysis of Power Consumption in Memory Hierarchies**
Patrick Hicks, Matthew Walnock, Robert Michael Owens 239

P2.4 **The Impact of SOI MOSFETs on Low Power Digital Circuits**
Ying-Che Tseng, Steven C. Chin, Jason C. S. Woo 243

P2.5 **On the Power Dissipation in Dynamic Threshold Silicon-on-Insulator CMOS Inverter**
Wei Jin, Philip C. H. Chan, Mansun Chan 247

P2.6 **Analogue LSI RF Switch and Beamforming Matrixes for Communications Satellites**
Markku Aberg, Anssi Leppanen, Arto Rantala, Jouko Marjonen 251

P2.7 **Low Power Architecture for High Speed Infrared Wireless Communication System**
Hiroshi Uno, Keiji Kumatani, Hiroyuku Okuhata, Isao Shirakawa, Toru Chiba 255

Session T5
Embedded Caches

Chair: Mary Jane Irwin

T5.1 **Low Power Data Processing by Elimination of Redundant Computations**
Mir Azam, Paul Franzon, Wentai Liu 259

T5.2 **An Object Code Compression Approach to Embedded Processors**
Yukihiro Yoshida, Bao-Yu Song, Hiroyuki Okuhata, Takao Onoye, Isao Shirakawa 265

Session T6
Gate Level Power Optimization

Chair: Sasan Iman

T6.1 **Low Power Multiplexer Decomposition**
Unni Narayanan, Hon Wai Leong, Ki-Seok Chung, C. L. Liu 269

T6.2 **Node Normalization and Decomposition in Low Power Technology Mapping**
Winfried Nöth, Reiner Kolla 275

T6.3 **A Gate Resizing Technique for High Reduction in Power Consumption**
P. Girard, C. Landrault, S. Pravossoudovitch, D. Severac 281

T6.4 **Re-Mapping for Low Power Under Tight Timing Constraints**
P. Vuillod, L. Benini, G. De Micheli 287

Evening Panel: Low Power Design Without Compromise

Moderator/Organizer: Jim Burr
Co-organizer: Anantha Chandrakasan
Fari Assaderaghi, Francky Catthoor, Frank Fox, Dave Greenhill, Deo Singh, Jim Sproch 293

Invited Talk

Chair: Lisa Su
SOI CMOS as a Mainstream Low Power Technology: A Critical Assessment
Dimitri A. Antoniadis 295

Session W1
Technology Paths To Low Power

Chair: Lisa Su

W1.1 **Fully Depleted CMOS/SOI Device Design Guidelines for Low Power Applications**
Srinivasa R. Banna, Philip C. H. Chan, Mansun Chan, Samuel K. H. Fung, Ping K. Ko 301

W1.2 **Hybrid Dual-Threshold Design Techniques for High-Performance Processors with Low-Power Features**
Uming Ko, Andrew Pua, Anthony Hill, Pranjal Srivastava 307

Session W2
Technology Optimizations

Chair: Don Monroe

W2.1 **Device and Technology Optimizations for Low Power Design in Deep Sub-micron Regime**
Kai Chen, Chenming Hu 312

W2.2 **Supply and Threshold Voltage Optimization for Low Power Design**
David J. Frank, Paul Solomon, Scott Reynolds, John Shin 317

Session W3
Adiabatic Techniques

Chair: Brock Barton

W3.1 **Clocked CMOS Adiabatic Logic with Integrated Single-Phase Power-Clock Supply: Experimental Results**
Dragan Maksimovic, Vojin G. Oklobdzija, Borivoje Nikolic, K. Wayne Current 323

W3.2 **AC-1: A Clock-Powered Microprocessor**
W. Athas, N. Tzartzanis, L. Svensson, L. Peterson, H. Li, X. Jiang, P. Wang, W-C. Liu 328

Low-Power CMOS Design through V_{TH} Control and Low-Swing Circuits

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Abstract

This paper describes some of the circuit level techniques for low-power CMOS designs. V_{TH} control circuits are necessary for achieving low-threshold voltage in high-speed low-voltage applications. As for the low-swing circuit techniques, applications to a clock system, logic part, and I/O's are discussed.

1. Introduction

CMOS power dissipation and delay are given by[1,2]

$$\text{Power} = p_t \cdot C_L \cdot V_S \cdot V_{DD} \cdot f_{CLK} + I_0 \cdot 10^{\frac{V_{TH}}{S}} \cdot V_{DD} \quad (1)$$

The first term, in (1) represents dynamic power dissipation due to charging and discharging of the load capacitance, where p_t is the switching probability, C_L is the load capacitance, V_S is the voltage swing of a signal, and f_{CLK} is the clock frequency. The second term is the subthreshold leak term and S is typically about 100mV/decade.

Figure 1 shows the plot for power and delay assuming 0.5μm design rule. As seen from the figure, lowering V_{DD} is effective in decreasing power but delay increases. Fig.1(b) shows equi-delay curves and the delay can be maintained if the V_{TH} is lowered as V_{DD} is reduced. Lowering V_{TH}, however, increases subthreshold leakage. In order to cope with this problem, V_{TH} control schemes have been proposed which are covered in Section 2.

In most cases, V_S in (1) is the same as V_{DD}, but in low-swing circuits V_S is smaller than V_{DD}. As seen from Eq.(1), reducing V_S can be one promising way to decrease power consumption. As for the low-swing circuit techniques, applications to a clock system, logic part, and I/O's are discussed in Section 3, 4, and 5, respectively

2. V_{TH} control techniques

To maintain throughput while lowering supply voltage to decrease power consumption, it is effective to lower the threshold voltage of MOSFET's. There are, however, issues associated with low V_{TH} in low V_{DD} environments.

First, delay fluctuates intolerably with V_{TH} fluctuation in low V_{DD} regime. For example, delay increase by 3 times for ΔV_{TH} = +0.15V at V_{DD} of 1V. The second issue is the subthreshold leakage increase. The leakage increases by 10 times for every ΔV_{TH} of - 0.1V. The third problem is the inability for I_{DDQ} test. I_{DDQ} test is necessary to screen out LSI's with defects and micro-shorts which develop to a failure in a long run.

In order to cope with these issues, V_{TH} control techniques have been proposed which are summarized in TABLE 1. Multi-Threshold V_{TH} CMOS[3,4], MTCMOS in short, tries to decrease the subthreshold leak in standby mode by inserting high V_{TH} MOSFET in series to normal circuitry. The high-V_{TH} device is turned off in standby mode and completely cut-off the leakage path. The drawback is the large inserted MOSFET which increases area and delay.

While the MTCMOS can solve only the standby leakage problem, the Variable Threshold CMOS[5-9] (VT CMOS) can solve all the three problems. It dynamically varies V_{TH} through substrate-bias, V_{BB}. Typically, V_{BB} is controlled so as to compensate V_{TH} fluctuations in the active mode, while in the standby mode and in the I_{DDQ} testing, deep V_{BB} is applied to increase V_{TH} and cut off the subthreshold leakage current. The idea to control the V_{BB} so as to minimize the subthreshold leakage under the condition that a representative circuit shows sufficient speed was also proposed (Frequency adaptive Threshold CMOS, FTCMOS[10]).

The Elastic V_{TH} CMOS[11], EVTCMOS in short, controls both V_{DD} and V_{BB} such that when V_{DD} is lowered VBB becomes that much deeper to raise V_{TH} and further reduce power dissipation. Note that internal V_{DD} and VSS are provided by source-follower n- and p- transistors, respectively, whose gate voltages are controlled. In order to control the internal power supply voltage independent from the power current, the source-follower transistors should operate near the threshold. This requires very large transistors.

In VTCMOS, it has been experimentally evaluated that the number of substrate (well) contacts can be greatly reduced in low voltage environments [7-9]. Using a phase-locked loop and an SRAM in a VTCMOS gate-array [8], the substrate noise influence has been shown to be negligible even with 1/400 of the contact frequency compared with the conventional gate-array. A DCT (Discrete Cosine Transform) macro made with the VTCMOS [7] has also been manufactured with substrate- and well- contacts only at the periphery of the macro and it worked without problems realizing more than one order of magnitude smaller power dissipation than a DCT macro in the conventional CMOS design.

3. Low-swing circuit for clock system

The four pie charts in Fig.2 shows power distribution in VLSI's. As seen from the charts, the power distribution of VLSI's differs from product to product. However, it is interesting to note that a clock system and a logic part itself consume almost the same power in various chips, and the clock system consumes 20% to 45% of the total chip power. One of the reasons for this large power consumption of the clock system is that the transition ratio of the clock net is

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one while that of the ordinary logic is about one third on average.

In order to reduce the clock system power, it is effective to reduce a clock voltage swing. Such idea is embodied in the Reduced Clock Swing Flip-Flop (RCSFF)[12]. Figure 3 shows circuit diagrams of the RCSFF. The RCSFF is composed of a current-latch sense amplifier and cross-coupled NAND gates which act as a slave latch. This type of flip-flop was first introduced in 1994[14] and extensively used in a microprocessor design[13]. The sense-amplifying F/F is often used with low-swing circuits because there is no DC leakage path even if the input is not full swing being different from the conventional gates or F/F's.

The salient feature of the RCSFF is to accept a reduced voltage swing clock. The voltage swing, Vclk, can be as low as 1V. When a clock driver Type A in Fig. 4 is used, power improvement is proportional to $Vclk^1$, while it is $Vclk^2$ if Type B driver is used. Type A is easy to implement but less efficient. Type B needs either an external Vclk supply or a DC-DC converter.

The issue of the RCSFF is that when a clock is high to Vclk, P1 and P2 do not switch off completely, leaving leak current flowing through either P1 or P2. The power consumption by this leak current turns out to be permissible for some cases (see next section), but further power improvement is possible by reducing the leak current. One way is to apply backgate bias to P1 and P2 and increase the threshold voltage. The other way is to increase the V_{TH} of P1 and P2 by ion-implant, which needs process modification and is usually prohibitive. When the clock is to be stopped, it should be stopped at V_{SS}. Then there is no leak current.

A. Area & Speed

The area of the RCSFF is about 20% smaller than the conventional F/F as seen from Fig. 5 even when the well for the precharge PMOS is separated.

As for delay, SPICE analysis is carried out assuming typical parameters of a generic 0.5μm double metal CMOS process. The delay depends on Wclk (Wclk is defined in Fig.3). Since delay improvement is saturated at Wclk = 10μm, this value of Wclk is used in the area and power estimation. Clock-to-Q delay is improved by a factor of 20% over the conventional F/F even when Vclk = 2.2V, which can be easily realized by a clock driver of the Type A1. Data setup time and hold time in reference to clock are 0.04ns and 0ns , respectively being independent from Vclk, compared to 0.1ns and 0ns for the conventional F/F.

B. Power

The power in the Fig.6 includes clock system power per F/F and the power of a F/F itself. The power consumption is reduced to about 1/2~1/3 compared to the conventional F/F depending on the type of the clock driver and V_{WELL}. In the best case studied here, 63% power reduction is observed. TABLE 2 summarizes typical performance improvement.

C. Application to reduced swing bus

For the RCSFF, the D and $\bar{D}$ input can also be small voltage swing signals. Using this characteristics, the RCSFF can be used to speed up RC delay of long buses. By placing the RCSFF at the end of a long bus and by sense-amplifying the slowly changing D input, RC delay can be reduced to 1/3 compared to the conventional F/F case (see Fig.7).

Let us consider what amount of power gain is observed when a distributed RC line is driven in full swing[15] at one end and switched off when the other terminal becomes V_2.

$$\frac{V(x,t)}{V_{DD}} = 1 + \frac{2}{\pi}\sum_{k=1}^{\infty}\frac{(-1)^k}{k-\frac{1}{2}}\cos\left\{\left(k-\frac{1}{2}\right)\pi\left(1-\frac{x}{L}\right)\right\}e^{-\left(k-\frac{1}{2}\right)^2\pi^2\frac{t}{RC}}$$

$$Q = \int_0^L cv(x,t)dx = CV_{DD}\left\{1-\frac{2}{\pi}\sum_{k=1}^{\infty}\frac{1}{\left(k-\frac{1}{2}\right)^2\pi^2}e^{-\left(k-\frac{1}{2}\right)^2\pi^2\frac{t}{RC}}\right\}$$

If the energy per cycle, E (=QV_{DD}), is expressed in terms of the terminal voltage, V_2 (=V(L,t)), E≈0.36+0.64V_2. This means that about 50% power saving is possible if an RC interconnect is driven when the voltage swing of V_2 is 0.2V_{DD}.

4. Low-swing circuit for logic

A pass transistor logic is known to provide a low-power design style. An attempt has been made to further reduce the power-delay product by reducing the signal voltage swing. A Sense-Amplifying Pass-transistor Logic (SAPL) [14] is such a circuit. In the SAPL, a reduced output signal of NMOS pass-transistor logic is amplified by a current latch sense-amplifier to gain speed and save power dissipation as shown in Fig. 9 and Fig.10. The SAPL has been applied to a 1.5ns 20bit carry skip adder in a Discrete Cosine Transform (DCT) macro whose circuit diagram is shown in Fig. 11. 50% speed, 30% area, and 50% power advantage were observed compared with the conventional static CMOS design.

The SAPL is also applied to a 0.9ns 64bit to 32bit double barrel shifter. In this case, 100% speed, 50% area, and 50% power advantage were observed. The MPEG2 decoder LSI which utilizes the DCT and VLD macro with SAPL operates under 0.9V supply voltage.

5. Low-swing circuit for I/O

Application of low-swing circuit to I/O's is also possible. The circuit diagram is shown in Fig.14. The transmitted signal is differential and again is received by a current-latch type sense-amplifier F/F. The two chips are put side by side and bonded directly with minimum capacitance and inductance. The photos of the system are shown in Figs.15 and 16.

At the frequency of 500MHz, the power consumption is 13mW per bonding which includes output and input power (see Fig. 17).

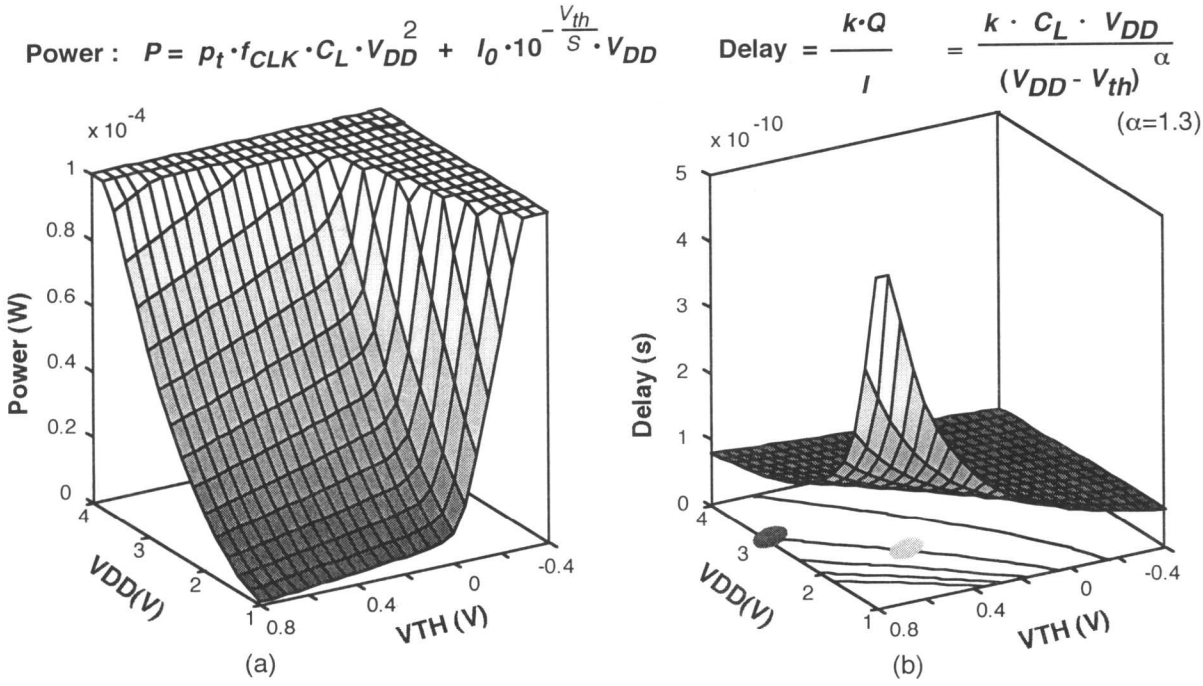


Fig.1 Dependence of (a) power and (b) delay on the supply voltage, V_{DD} and the threshold voltage, V_{TH}.

TABLE 1 Comparison of various V_{TH} control techniques

	MTCMOS	VTCMOS	EVTCMOS
Scheme	St'by, *High-Vth, V_{DD}, V_{DD}', Low-Vth, V_{SS} Ref.[3,4]	n-well, St'by, control (SSB), V_{DD}, V_{SS}, p-well Ref.[5-9]	St'by, control (DLL), *, V_{DD}, V_{DD}', V_{SS}', V_{SS} Ref.[11]
	V_{DD} on-off	V_{BB} control	V_{DD}&V_{BB} control
Effect	+ $I_{st'by}$ reduction	+ ΔV_{th} compensation + $I_{st'by}$ reduction + I_{DDQ} test	+ ΔV_{th} compensation + $I_{st'by}$ reduction + I_{DDQ} test
Penalty	- large serial MOSFET(*) slower,larger,lower yield - special latch	- triple well (desirable)	- large serial MOSFET operating near threshold(*)

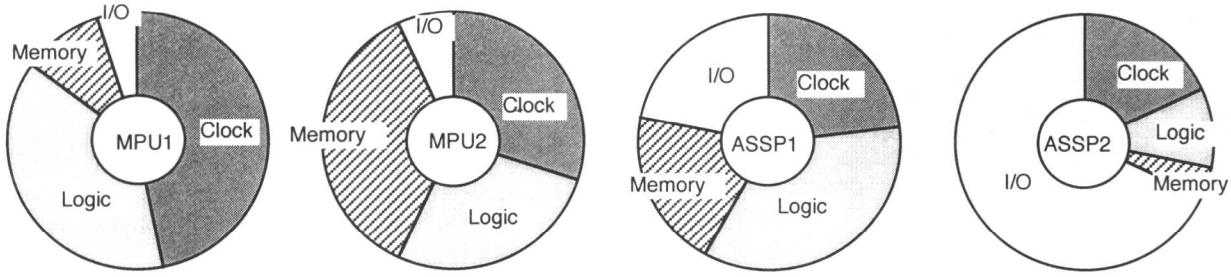
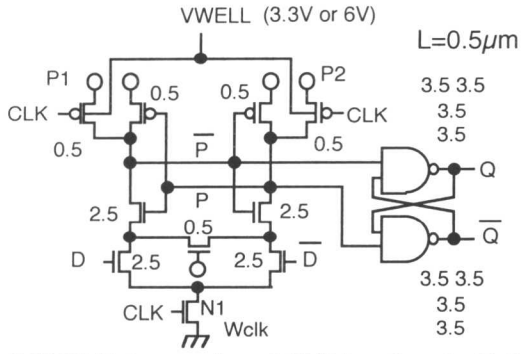
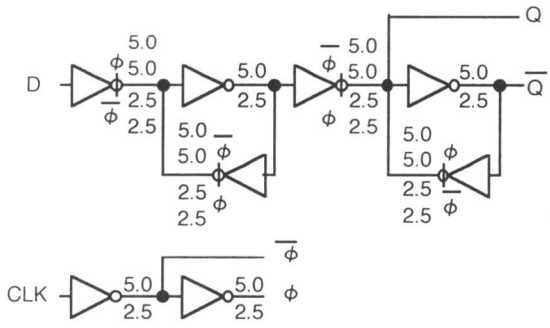


Fig. 2 Power distribution in VLSI's. MPU1 is a low-end microprocessor for embedded use, MPU2 is a high-end CPU with large amount of cache, ASSP1 is a MPEG2 decoder and ASSP2 is an ATM switch.

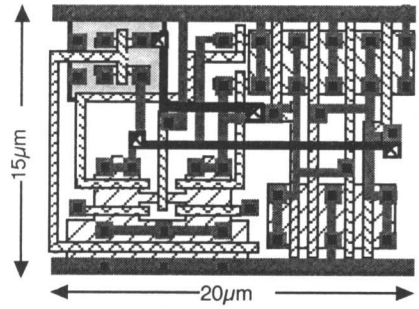


(a) RCSFF. Voltage swing of CLK is reduced toVclk

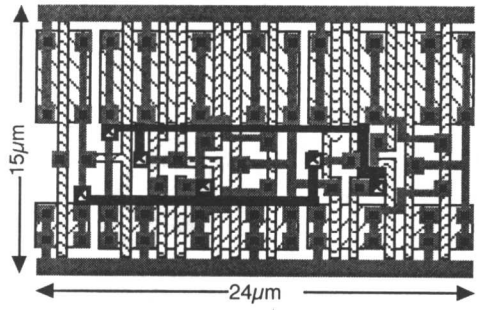


(b) Conventional F/F

Fig. 3 Circuit diagram of (a) the Reduced Clock Swing Flip-Flop (RCSFF) and (b) the conventional F/F. Numbers in the figure signify MOSFET gate width. Wclk is the gate width of N1



(a) RCSFF (N-well for P1 & P2 separated)



(b) Conventional F/F

Fig. 5 Layout of (a) the Reduced Clock Swing Flip-Flop (RCSFF) with Wclk being 10μm and (b) the conventional F/F.

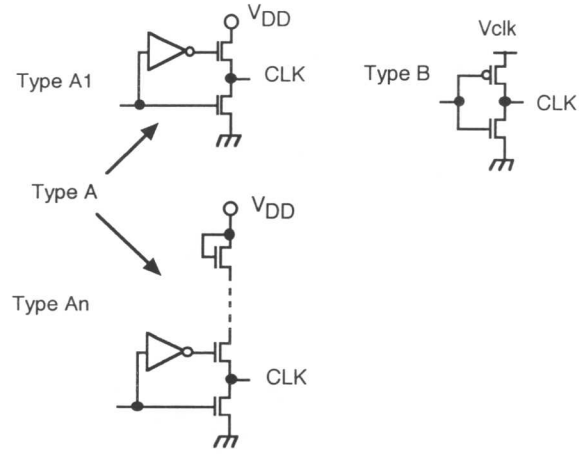


Fig. 4 Types of clock drivers. Type A1 and Type An are grouped as Type A. In Type B, Vclk is supplied by externally.

TABLE 2 Performance comparison of RCSFF and Conventional F/F

	Driver	Vclk[V]	Power	Delay	Area
Conventional		3.3	100%	100%	100%
RCSFF	Type A1	2.2	59%	82%	83%
V_{well} =6.6V	Type A2	1.3	48%	123%	83%
W_{clk} =10μm	Type B	2.2	48%	82%	83%
f clk =100MHz	Type B	1.3	37%	123%	83%

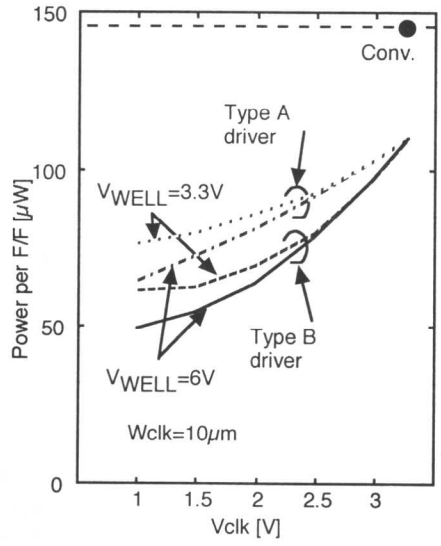


Fig 6. Power consumption for one F/F. Clock interconnection length per one F/F is assumed to be 200μm and data activation ratio is assumed to be 30%. $f$clk is 100MHz. By applying 6V well bias, the initial Vth of P1 and P2 (0.6V) increases to 1.4V.

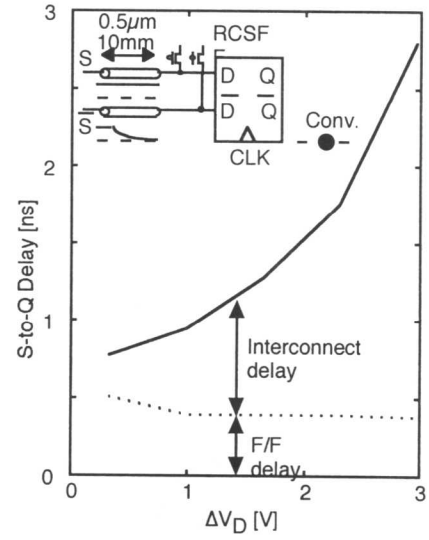


Fig. 7 Delay improvement of a long RC bus by RCSFF. Wclk=10μm and Type A1 clock driver is used. Bus is differential and precharged to VDD first and then CLK is asserted when the voltage difference of D and D becomes ΔVD.

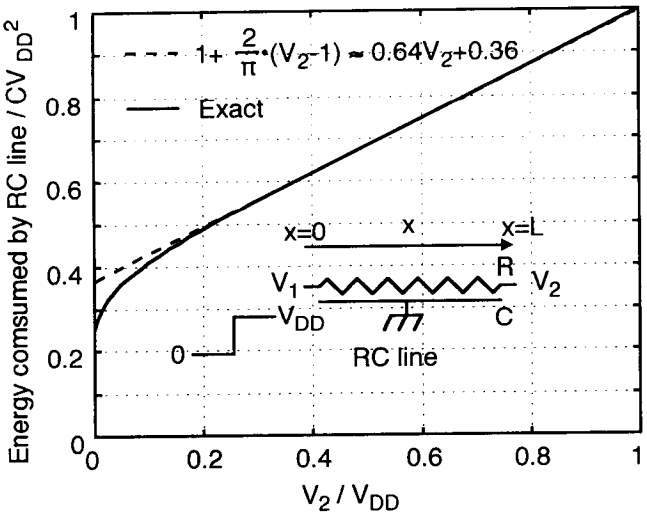


Fig.8 Energy consumed by RC interconnect if the voltage swing of V2 is reduced.

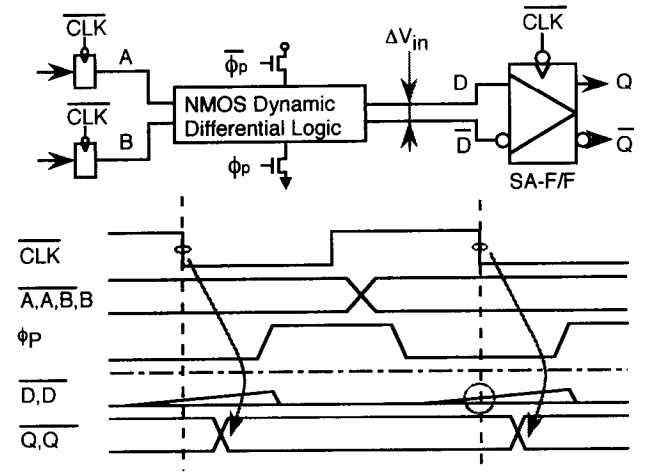


Fig.10 Timing chart of SAPL

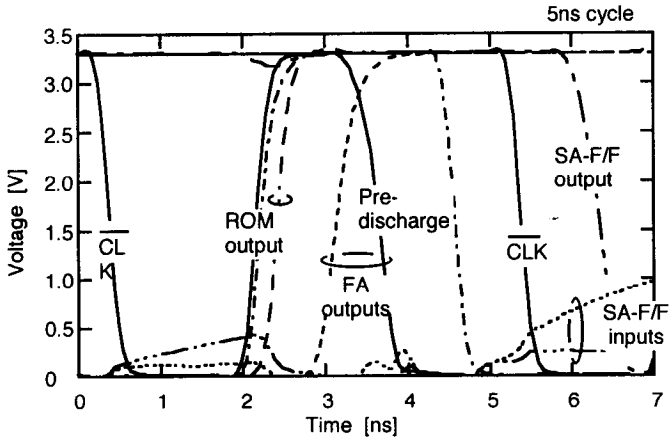


Fig.12 Waveforms for SAPL adder of Fig. 11

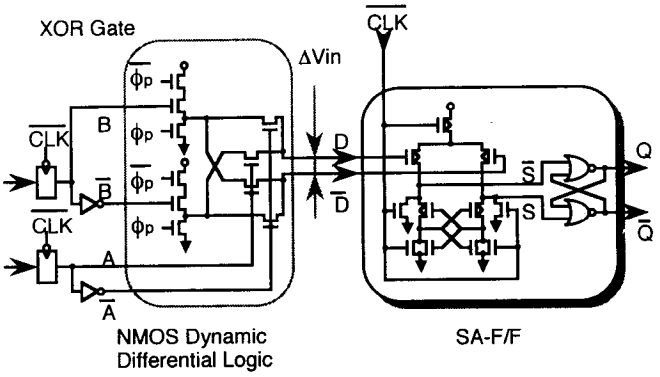


Fig.9 Sense-Amplifying Pass-Transistor (SAPL) logic concept.. The reduced swing signal is amplified by sense-amplifying flip-flop.

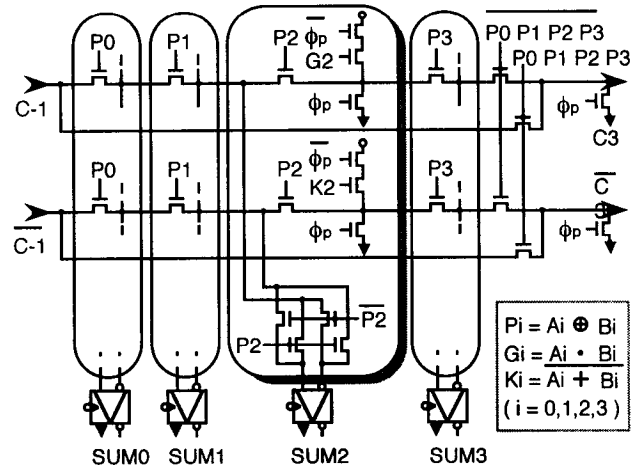


Fig.11 Sense-Amplifying Pass-Transistor (SAPL) applied to 20bit skip-carry adder. The adder was used in a Descrete Cosine Transform macro in a MPEG2 decoder chip which worked under 0.9V.

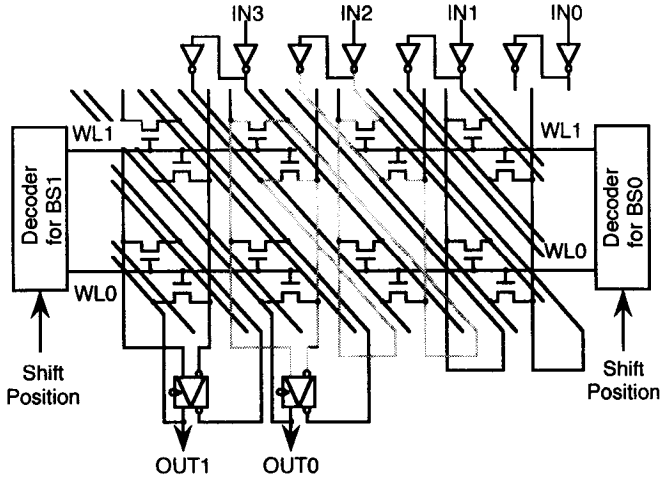


Fig.13 Sense-Amplifying Pass-Transistor (SAPL) applied to a 32bit barrel shifter. The shifter was used in a Variable Length Decoder macro in a MPEG2 decoder chip which worked under 0.9V.

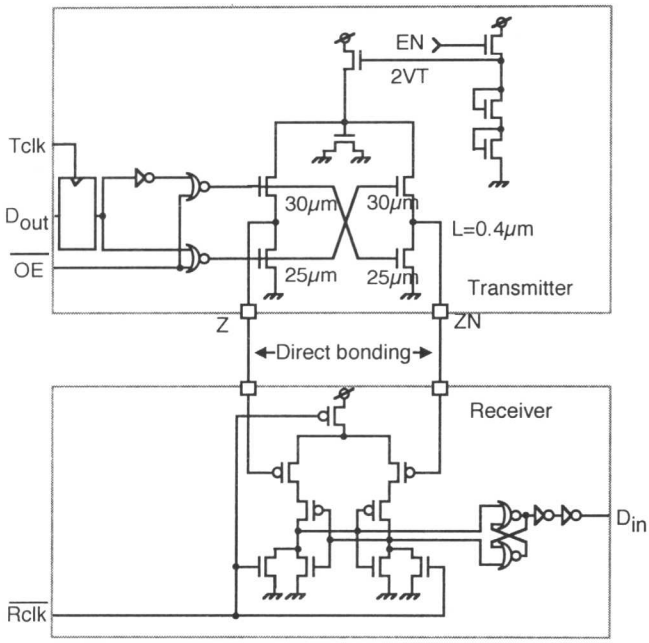


Fig.14 Circuit diagram of low-swing I/O. The upper half is a transmitter side and the lower half is a receiver side.

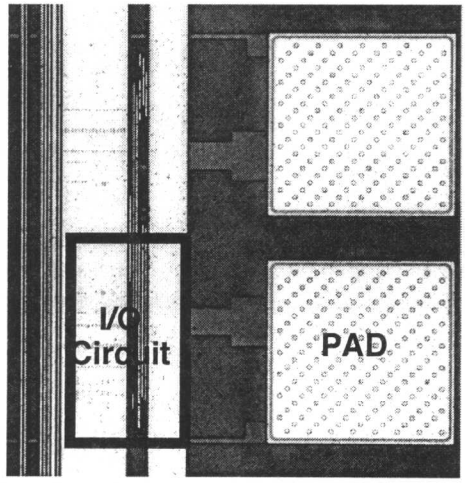


Fig.15 Microphotograph showing bonding pads and I/O circuits (mostly under Al lines). The I/O circuit includes input and output circuit and is smaller than a pad.

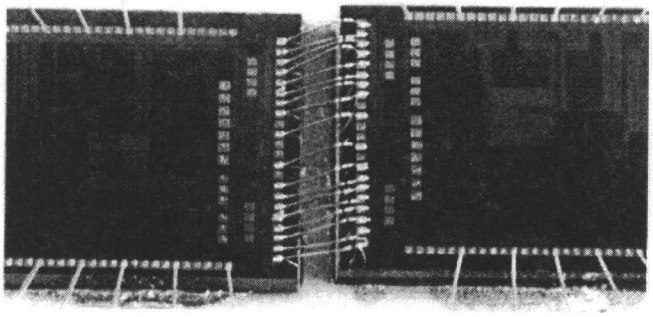


Fig.16 Photograph to show two chips are connected by bonding wires directly.

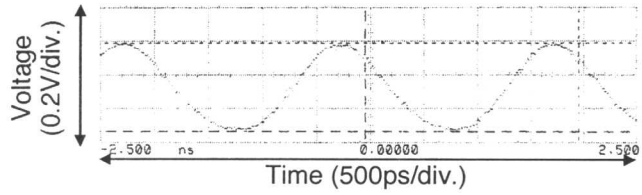


Fig.17 Measured waveform on the bonding pads. The frequency is 500MHz.

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Survey of Low Power Techniques for ROMs

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Abstract

This paper presents a survey of low power techniques for Read Only Memories (ROMs). Significant savings in power dissipation are achieved through the use of techniques at the circuit and architecture level. The ROM circuits have been designed in 0.35 μm CMOS technology and simulated using PowerMill.

Introduction

With the development of submicron technologies and the increase of complexity on VLSI chips, the market for portable applications, digital signal processors and ASIC implementations has focused significant effort on the design of low power systems [1]. ROMs (Read Only Memories) are an important part of many digital systems (e.g., digital filters, digital signal processors, microprocessors etc). The high area density of ROMs makes these types of circuits very attractive to store fixed information (e.g., coefficients of a digital filter). As new submicron technologies are developed, the fast speeds of these processes allow the implementation of architectures which could not be implemented in the past. Also the increase in the number of metal layers becomes a main instrument to reduce switched capacitance without penalty in the density of the ROM. Significant savings in power are achieved through the implementation of several techniques. The focus of this paper is on techniques at the architecture and transistor levels and their global impact on power dissipation.

The first section of the paper explains traditional ROM designs and the sources of power dissipation. The second part of this paper discusses low power techniques at the architecture level. The next section presents techniques that are applicable at the circuit level. The last section shows results and conclusions.

1 Sources of Power Dissipation

Figure 1 shows the traditional architecture of a ROM. The decoder selects among the row lines that run through the ROM core, turning on only one row line at a given time. The column multiplexer and driver select which column is being read and drive the data bus. The control logic generates the internal signals of the ROM (i.e., precharge, read etc.). The ROM core is used to store information through the placement of transistors. There are two main types of ROMS: NAND array, where pull down transistors are in series and NOR array where the pull down transistors are in parallel. This paper focuses on ROMs using a NOR array since these structures are faster than NAND arrays and are the most frequently used [2].

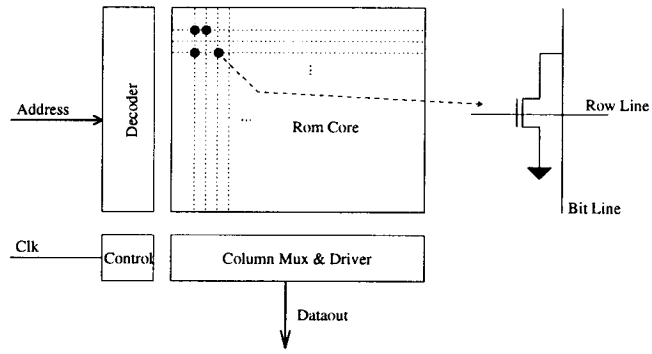

Figure 1: ROM Block Diagram

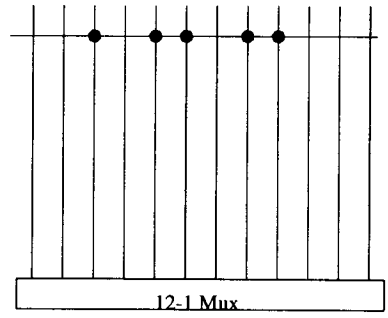

Figure 2: ROM Bitlines

In order to save power, most ROMs precharge during one phase of the clock and evaluate in the other. Table 1 shows the power dissipation in a 2K x 18 ROM designed in 0.6 μm technology at 3.3V and clocked at 10 MHz. As the table shows, the precharge of the bit lines in the ROM core dissipates most of the power. There are two main reasons for this. First, bit lines have large capacitance (drain capacitance of the transistors tied to this line, parallel plate and fringe component to substrate plus the overlap of the row lines and other metal layers). Second, more than 18 bit lines are switched per access; this is due to the word line selecting more bit lines than

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