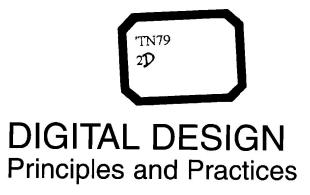
THIRD EDITION UPDATED

# Package includes the Soundarion of All NA. Series Software Edition

PRINCIPLES & PRACTICES

JOHN F. WAKERLY



Third Edition Updated

# John F. Wakerly

Cisco Systems, Inc. Stanford University



Prentice Hall, Upper Saddle River, New Jersey 07458

Library of Congress Cataloging-in-Publication Data

Wakerly, John F.

Digital design: principles and practices.. John F. Wakerly.--3rd ed., updated

Includes bibliographical references and index.

ISBN 0-13-089896-1

1. Digital integrated circuits--Design and construction.

I.Title.

TK7874.65.W34 2000 621 .39'5--dc21

00-041684 CIP

Publisher: TOM ROBBINS

Vice president and editorial director of ECS: MARCIA HORTON

Acquistions editor: ERIC FRANK Production editor: IRWIN ZUCKER

Executive managing editor: VINCE O'BRIEN Managing editor: DAVID A. GEORGE Manufacturing buyer: PAT BROWN

Vice president and director of production and manufacturing, ESM: DAVID W. RICCARDI

Director of creative services: PAUL BELFANTI

Art director: JONATHAN BOYLAN Cover art: ROBERT MCFADDEN Cover designer: JOHN CHRISTIANA Interior designer: DONNA WICKES Editorial assistant: JENNIFER DIBLASI



© 2001, 2000,1994, 1990 by Prentice Hall Prentice-Hall, Inc. Upper Saddle River, New Jersey 07458

All rights reserved. No part of this book may be reproduced, in any format or by any means, without permission in writing from the publisher

The author and publisher of this book have used their best efforts in preparing this book. These efforts include the development, research, and testing of the theories and programs to determine their effectiveness. The author and publisher make no warranty of any kind, expressed or implied, with regard to these programs or the documentation contained in this book. The author and publisher shall not be liable in any event for incidental or consequential damages in connection with, or arising out of, the furnishing, performance, or use of these programs.

Trademark Information: Verilog is a trademark of Cadence Design Systems. Inc. Silos III is a trademark of Simucad Inc. Synopsys and Foundation Express are trademarks of Synopsys, Inc. Xilinx is a trademark of Xilinx Corp. Aldec is a trademark of Aldec.

Printed in the United States of America

10987654321

#### ISBN 0-13-089896-1

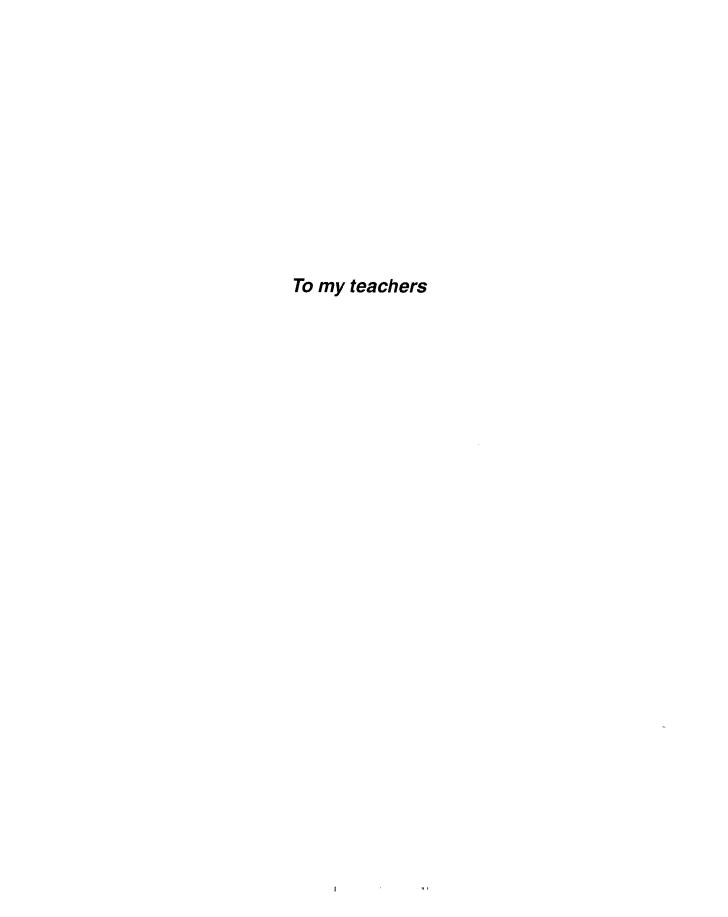
Prentice-Hall International (UK) Limited, London Prentice-Hall of Australia Pty. Limited, Sydney

Prentice-Hall Canada Inc., Toronto

Prentice-Hall Hispanoamericana, S.A.. Mexico Prentice-Hall of India Private Limited. New Delhi

Prentice-Hall of Japan, Inc., Tokyo Pearson Education Asia Pte. Ltd.

Editora Prentice-Hall do Brasil, Ltda., Rio de Janeiro



# **FOREWORD**

Moore's Law, which observes that semiconductor technology advances exponentially, has been valid for over three decades. Experts predict it will continue to hold for at least one more. When integrated circuits were introduced, logic packages had a dozen or so transistors. Today, with exponential increases in circuit density, microprocessor chips have passed the 10-million-transistor mark. In less than another decade they will reach 100 million transistors per chip.

To keep up with Moore's Law, design techniques have changed drastically. Hand-crafted logic circuits were once the norm. Now designers generate circuits from high-level descriptions. Connections on printed-circuit boards have been absorbed within chips. With programmable logic, on-chip logic functions and connections can be updated within the user environment.

How does education keep up with Moore's Law? What can we do to enable students to practice their skills today and adapt them tomorrow to new generations of devices? This is the challenge John Wakerly faced when he began this work.

His approach is multifaceted. It is grounded in basic principles of digital design that do not change with technology, such as combinational logic, sequential logic, and state machines. Wakerly weds these principles with tools and practical techniques that teach how to design for today's technology. These include how to use the ABEL and VHDL design languages, how to structure designs with large building blocks, and how to implement designs with programmable logic devices. These techniques are essential for successful design.

The most difficult goal is to help the student adapt to the inevitable changes to come. Wakerly does this by revealing what is happening underneath the logic. For example, he gives transistor models of gates and uses them to expose issues

related to timing and noise. Gates may become faster and denser and may use different control voltages, but how to assure correct and reliable operation will be a continuing concern. We learn the characteristics, constraints, and failure modes and how to design to them. We learn through examples of alternate designs how to judge design quality and evaluate tradeoffs. As new technology emerges, we will be able to design to it.

Wakerly enhances the approach with presentation skills that are rare in college texts. The reader will quickly appreciate the effective graphics, entertaining writing style, and instructive exercises.

Moore's Law condemns textbooks in this field to short lives. Nevertheless. Wakerly's text is a classic.

Harold S. Stone Princeton, New Jersey

# **PREFACE**

This book is for everyone who wants to design and build real digital circuits. It is based on the idea that, in order to do this, you have to grasp the fundamentals, but at the same time you need to understand how things work in the real world. Hence, the "principles and practices" theme.

The material in this book is appropriate for introductory courses on digital logic design in electrical or computer engineering or computer science curricula. Computer science students who are unfamiliar with basic electronics concepts or who just aren't interested in the electrical behavior of digital devices may wish to skip Chapter 3; the rest of the book is written to be independent of this material as much as possible. On the other hand, *anyone* with a basic electronics background who wants to get up to speed on digital electronics can do so by reading Chapter 3. In addition, students with *no* electronics background can get the basics by reading Bruce M. Fleischer's "Electrical Circuits Review," a freely reproducible 20-page electronics tutorial available on this book's Web site, www.ddpp.com.

Although this book's level is introductory, it contains much more material than can be taught in a typical introductory course. Once I started writing, I found that I had many important things to say that wouldn't fit into a one-quarter course at Stanford or a 400-page book. Therefore, I have followed my usual practice of including *everything* that I think is at least moderately important, and leaving it up to the instructor or reader to decide what is most important in a particular environment. To help these decisions along, though, I've marked the headings of *optional sections* with an asterisk. In general, these sections can be skipped without any loss of continuity in the non-optional sections that follow.

Undoubtedly, some people will use this book in advanced courses and in laboratory courses. Advanced students will want to skip the basics and get right into the fun stuff. Once you know the basics, the most important and fun stuff in

introductory courses

electronics concepts

optional sections

advanced courses laboratory courses fun stuff

working digital designers

marginal notes marginal pun this book is in the sections on hardware description languages ABEL and VHDL, where you'll discover that your programming courses actually helped prepare you to design hardware.

Another use of this book is as a self-study reference for a working digital designer, who may be either of two kinds:

*Novice* If you're just getting started as a working digital designer, and you took a very "theoretical" logic design course in school, you should concentrate on Chapters 3, 5, 6, and 8–11 to get prepared for the real world.

Old pro If you're experienced, you may not need all of the "practices" material in this book, but the principles in Chapters 2, 4, and 7 can help you organize your thinking, and the discussions there of what's important and what's not might relieve the guilt you feel for not having used a Karnaugh map in 10 years. The examples in Chapters 6, 8, and 9 should give you additional insights into and appreciation for a variety of design methods. Finally, the ABEL and VHDL language descriptions and examples sprinkled throughout Chapters 4 through 9 may serve as your first organized introduction to HDL-based design.

All readers should make good use of the comprehensive index and of the *marginal notes* throughout the text that call attention to definitions and important topics. Maybe the highlighted topics in *this* section were more marginal than important, but I just wanted to show off my text formatting system.

#### **Chapter Descriptions**

What follows is a list of short descriptions of this book's eleven chapters. This may remind you of the section in software guides, "For People Who Hate Reading Manuals." If you read this list, then maybe you don't have to read the rest of the book.

- Chapter 1 gives a few basic definitions and lays down the ground rules for what we think is and is not important in this book.
- Chapter 2 is an introduction to binary number systems and codes. Readers who are already familiar with binary number systems from a software course should still read Sections 2.10–2.13 to get an idea of how binary codes are used by hardware. Advanced students can get a nice introduction to error-detecting codes by reading Sections 2.14 and 2.15. The material in Section 2.16.1 should be read by everyone; it is used in some design examples in Chapter 8.
- Chapter 3 describes "everything you ever wanted to know about" digital
  circuit operation, placing primary emphasis on the external electrical characteristics of logic devices. The starting point is a basic electronics
  background including voltage, current, and Ohm's law; readers unfamiliar

- with these concepts may wish to consult the "Electrical Circuits Review" mentioned earlier. This chapter may be omitted by readers who aren't interested in how to make real circuits work, or who have the luxury of having someone else to do the dirty work.
- Chapter 4 teaches combinational logic design principles, including switching algebra and combinational-circuit analysis, synthesis, and minimization. Introductions to ABEL and VHDL appear at the end of this chapter.
- Chapter 5 begins with a discussion of digital-system documentation standards, probably the most important practice for aspiring designers to start practicing. Next, this chapter introduces programmable logic devices (PLDs), focusing on their capability to realize combinational logic functions. The rest of the chapter describes commonly used combinational logic functions and applications. For each function, it describes standard MSI building blocks, ABEL programs for PLD realizations, and VHDL models.
- Chapter 6 is a collection of larger combinational-circuit design examples.
   For each example, it shows how the design can be carried out with MSI building blocks (if appropriate), ABEL and PLDs, or VHDL that can be targeted to a CPLD or FPGA.
- Chapter 7 teaches sequential logic design principles, starting with latches and flip-flops. The main emphasis in this chapter is on the analysis and design of clocked synchronous state machines. However, for the brave and daring, the chapter includes an introduction to fundamental-mode circuits and the analysis and design of feedback sequential circuits. The chapter ends with sections on ABEL and VHDL features that support sequential-circuit design.
- Chapter 8 is all about the practical design of sequential circuits. Like
  Chapter 5 before it, this chapter focuses on commonly used functions and
  gives examples using MSI building blocks, ABEL and PLDs, and VHDL.
  Sections 8.8 and 8.9 discuss the inevitable impediments to the ideal of fully
  synchronous design and address the important problem of how to live
  synchronously in an asynchronous world.
- Chapter 9 is a collection of state-machine and larger sequential-circuit design examples. Each example is carried out both using ABEL for a PLD and using VHDL that can be targeted to a CPLD or FPGA.
- Chapter 10 is an introduction to memory devices, CPLDs, and FPGAs.
   Memory coverage includes read-only memory and static and dynamic read-write memories from the points of view of both internal circuitry and functional behavior. The last two sections introduce CPLD and FPGA architecture.

• Chapter 11 discusses several miscellaneous real-world topics that are of interest to digital designers. When I started writing what I thought would be a 300-page book, I included this chapter in the outline to pad out the "core" material to a more impressive length. Well, the book is obviously long enough without it, but this material is useful just the same.

Most of the chapters contain references, drill problems, and exercises. Drill problems are typically short-answer or turn-the-crank questions that can be answered directly based on the text material, while exercises may require a little more thinking. The drill problems in Chapter 3 are particularly extensive and are designed to allow non-EE types to ease into this material.

#### Xilinx Foundation Tools

Xilinx, Inc. (San Jose, CA 95124) has kindly allowed us to package their Foundation Express digital-design tools on two CD-ROMs with this book (in most domestic and international printings). These tools are quite comprehensive, including an ABEL compiler, VHDL and Verilog language processors, a schematic drawing package, and a simulator. Much of the software in the package is based on the popular Active-CAD<sup>TM</sup> and Active-HDL<sup>TM</sup> tools from Aldec, Inc. The package also includes FPGA Express<sup>TM</sup> software from Synopsys, which allows ABEL, VHDL, and Verilog designs to be targeted to CPLDs and FPGAs; popular Xilinx parts are supported by the included version.

The Foundation tools were very useful to me as an author. Using them, I was able to write and test all of the example programs in the text. I trust that the tools will be even more useful to the students who use the text. They will allow you to write and test your own hardware designs and download them into Xilinx CPLDs and FPGAs in a lab environment. The student package support designs with up to 20,000 gates that fit into a single device. For a nominal fee, you can access a comprehensive set of Xilinx tutorials and two excellent Xilinx lab books online at www.prenhall.com/xilinx. These and other resources at this website will help you get the most out of the Foundation tools.

Even if you're not ready to do your own original designs, you can use the Foundation tools to try out and modify any of the examples in the text, since the source code for all of them is available at the book's Web site, discussed next.

#### www.ddpp.com

Support materials for this book are available at the book's own dedicated Web site, www.ddpp.com. A key resource for students is the set of source listings for all of the example C, ABEL, and VHDL programs in the book. Also available are ZIP'ed Foundation project directories, including not only ABEL and VHDL source files but also schematics that are set up to use and simulate some of the example designs.

During the preparation of this edition, I was surprised and delighted to see how much digital design reference material is available on the Web, especially from device manufacturers. The DDPP Web site contains a "living" references section with links to many useful sites that you can use as a jumping-off point for your own independent study.

A couple of appendices from previous editions are available on the Web site—"Electrical Circuits Review" by Bruce M. Fleischer and "IEEE Standard Symbols." Students taking lab courses may also appreciate the four pages of handy IC pinout guides, which appeared on the inside-cover pages of previous editions.

One thing that students may or may not like is a collection of new exercises that I expect to build up as I continue to teach digital design at Stanford and as I receive contributions from others.

#### For Instructors

The DDPP Web site has additional materials for instructors only. This part of the site is password protected; if you plan to use it, please allow up to a week to obtain a login name and password via the procedure published there.

The instructors' area contains files with all of the figures and tables in the book. You can use these files to make presentation slides directly, or you can insert selected materials into your own customized presentations.

The site also contains answers to selected exercises—more than half of the exercises in the book, equivalent to over 200 printed pages. There are also several sample exams and solutions.

Another important resource for instructors is Xilinx' University Program (www.xilinx.com/programs/univ). The site offers a variety of product materials, course materials, and discounts on chips and boards that you can use in digital-design lab courses.

# **How This Book Was Prepared**

The text of the third edition of this book was converted from the original second-edition TEX version into Adobe FrameMaker<sup>®</sup>. Figures from previous editions were converted from Cricket Draw into Adobe Illustrator<sup>®</sup> EPS files.

All of the writing, editing, drawing, and circuit designing was done on a PC running Windows 95 or 98 with 384 Mbytes of memory, which, regrettably, would still crash if too many programs or files were open at once. The good news is that this edition's use of standard programs and tools has allowed me to provide readers and instructors with a large collection of useful materials on the book's Web site, as described earlier.

#### **Errors**

Warning: This book may contain errors. The author assumes no liability for any damage—incidental, brain, or otherwise—caused by errors.

There, that should make the lawyers happy. Now, to make you happy, let me assure you that a great deal of care has gone into the preparation of this manuscript to make it as error free as possible. I am anxious to learn of the remaining errors so that they may be fixed in future printings, editions, and spin-offs. Therefore I will pay \$5 to the first finder of each undiscovered error, be it technical, typographical, or otherwise. Please email your comments by using the link on the Web site, or by writing to me at john@wakerly.com.

Any reader can obtain an up-to-date list of discovered errors using the link at the book's Web site. It will be a very short file transfer, I hope.

#### Acknowledgements

Many people helped make this book possible. Most of them helped with the first and second editions and are acknowledged there. Preparation of the third edition has been a lonelier task, but it was made easier by my colleagues Mario Mazzola and Prem Jain at Cisco Systems. They and the company made it possible for me to cut back my commitment at Cisco to less than half time for the eight months that it took to prepare this edition.

For the ideas on the "principles" side of this book, I still owe great thanks to my teacher, research advisor, and friend Ed McCluskey. On the "practices" side, my personal "Digital Designers Hall of Fame" includes (in chronological order): Ed Davidson, Jim McClure, Courtenay Heater, Sam Wood, Curt Widdoes, Prem Jain, Ted Tracy, Dave Raaum, Akhil Duggal, Des Young, and Tom Edsall.

The seed that got me started writing this book and many others was planted in the early 70s by Harold Stone at Stanford. He put me to work reviewing and indexing his books, and his computer organization books inspired me to write my first software book. Now, I'd like to offer Harold my belated thanks for getting me started, and I give him special thanks for helping to pad out this edition by another two pages!

In the summer of 1997, during the early stages of this edition's planning, friend and colleague Jean-Pierre Steger took a sabbatical from the Burgdorf School of Engineering near Bern, Switzerland to help me get jump-started with VHDL, the Xilinx Foundation tools, and other topics. A number of other people contributed review comments or other materials to this edition, including John Birkner, Rebecca Farley, Don Gaubatz, John Gill, Linley Gwennap. Jesse Jenkins, and Jeff Purnell.

Xilinx, Inc. naturally deserves credit for providing the Foundation tools that are an important adjunct to this edition. On the people side, their original

University Program leader Jason Feinsmith was very helpful, and their recently appointed leader Patrick Kane has supported our efforts enthusiastically.

Since the second edition was published, I have received many helpful comments from readers. In addition to suggesting or otherwise motivating many improvements, readers have spotted dozens of typographical and technical errors whose fixes are incorporated in this third edition.

My sponsoring editor at Prentice Hall, Tom Robbins, deserves great thanks for his patience. He's the second editor to have been lured to Prentice Hall in part by the (falsely attractive) prospect of working on a project with me, only to find out upon his arrival that the project was very late. In Tom's case, though, I had known him since the early 80s when he first tried to sign me up for a project with another publisher, and we'd been trying to find a way to work together ever since. We're finally there, starting the third decade of our friendship. Tom contributed more than patience—among other things, you have him to thank for getting you the free Xilinx software that comes with this book (most printings).

Production editor Irwin Zucker also deserves credit for providing a very smooth interface with the production side of the house and for putting in long hours to help me during the final "crunch" stage of the project. If not for him, I would not have been able to leave on a long-planned three-week family vacation after the book's completion. (I'm told that if I hadn't finished in time, our 90-pound dog would have gone to Europe in my seat instead!)

Special thanks go to artist Robert McFadden, whose trippy cover painting is hanging in my home along with several other of his far-out works. His painting, which I commissioned and he completed well over a year ago, provided me with the motivation to actually get the *inside* of the book done.

It seems like some disaster always strikes just as I am completing one of these projects. For the first edition, it was the World-Series earthquake of 1989. For the second edition, it was acute appendicitis four days before the book's scheduled completion. This time, I didn't get the bad news until after the first printing of the new edition came out. When I tried to call Robert McFadden for the address to send complimentary copies with his wonderful cover art, his wife informed me that he had passed away nine months before. He's gone at much too young an age, but his paintings will live on and continue to inspire many of us in future flights of fancy.

As always, I must thank my wife Kate for putting up with the late hours, frustration, crabbiness, preoccupation, and phone calls from weird people that occur when I'm engaged in a writing project like this. We hope you enjoy starting this book as much as we enjoy finishing it!

John F. Wakerly Mountain View, California

# Digital Design Principles and Practices

# **CONTENTS**

ΧV

About Digital Design

Digital Devices

Analog versus Digital 3

xvii

INTRODUCTION

FOREWORD

1.1

1.2

1.3

PREFACE

1

1.4	Electronic Aspects of Digital Design 7
1.5	Software Aspects of Digital Design 9
1.6	Integrated Circuits 12
1.7	Programmable Logic Devices 15
1.8	Application-Specific ICs 16
1.9	Printed-Circuit Boards 18
1.10	Digital-Design Levels 18
1.11	The Name of the Game 22
1.12	Going Forward 23
Drill F	Problems 24
NUM	MBER SYSTEMS AND CODES 25
2.1	Positional Number Systems 26
2.2	Octal and Hexadecimal Numbers 27
2.3	General Positional-Number-System Conversions 29
2.4	Addition and Subtraction of Nondecimal Numbers 32
2.5	Representation of Negative Numbers 34
	2.5.1 Signed-Magnitude Representation
	2.5.2 Complement Number Systems
	2.5.3 Radix-Complement Representation
	2.5.4 Two's-Complement Representation
	2.5.5 Diminished Radix-Complement Representation
	2.5.6 Ones'-Complement Representation 2.5.7 Excess Representations
2.6	Two's-Complement Addition and Subtraction 39
	2.6.1 Addition Rules 2.6.2 A Graphical View 2.6.3 Overflow
	2.6.4 Subtraction Rules 2.6.5 Two's-Complement and Unsigned Binary Numbers

2.7	Ones'-Complement Addition and Subtraction 44
2.8	Binary Multiplication 45
2.9	Binary Division 47
2.10	Binary Codes for Decimal Numbers 48
2.11	Gray Code 51
2.12	Character Codes 53
2.13	Codes for Actions, Conditions, and States 53
2.14	n-Cubes and Distance 57
2.15	Codes for Detecting and Correcting Errors 58
	2.15.1 Error-Detecting Codes
	2.15.2 Error-Correcting and Multiple-Error-Detecting Codes
	2.15.3 Hamming Codes 2.15.4 CRC Codes
	2.15.5 Two-Dimensional Codes 2.15.6 Checksum Codes
	2.15.7 m-out-of-n Codes
2.16	Codes for Serial Data Transmission and Storage 69
	2.16.1 Parallel and Serial Data 2.16.2 Serial Line Codes
	erences 73
	Problems 74
Exer	rcises 76
DIGITAL CIRCUITS 79	
3.1	Logic Signals and Gates 80
3.2	Logic Families 84
3.3	CMOS Logic 86 3.3.1 CMOS Logic Levels 3.3.2 MOS Transistors
	3.3.1 CMOS Logic Levels 3.3.2 MOS Transisions 3.3.3 Basic CMOS Inverter Circuit
	3.3.4 CMOS NAND and NOR Gates 3.3.5 Fan-In
	3.3.6 Noninverting Gates
	3.3.7 CMOS AND-OR-INVERT and OR-AND-INVERT Gates
3.4	Electrical Behavior of CMOS Circuits 96
0.4	3.4.1 Overview 3.4.2 Data Sheets and Specifications
3.5	CMOS Steady-State Electrical Behavior 99
0.0	3.5.1 Logic Levels and Noise Margins
	3.5.2 Circuit Behavior with Resistive Loads
	3.5.3 Circuit Behavior with Nonideal Inputs 3.5.4 Fanout
	3.5.5 Effects of Loading 3.5.6 Unused Inputs
	3.5.7 Current Spikes and Decoupling Capacitors
	3.5.8 How to Destroy a CMOS Device
3.6	CMOS Dynamic Electrical Behavior 113
	3.6.1 Transition Time 3.6.2 Propagation Delay
	3.6.3 Power Consumption
3.7	
	3.7.1 Transmission Gates 3.7.2 Schmitt-Trigger Inputs
	3.7.3 Three-State Outputs 3.7.4 Open-Drain Outputs 3.7.5 Driving LEDs 3.7.6 Multisource Buses 3.7.7 Wired Logic
	5.7.5 Ditting EEDS
	3.7.8 Pull-Up Resistors

```
3.8 CMOS Logic Families
                             135
                            3.8.2 VHC and VHCT
     3.8.1 HC and HCT
     3.8.3 HC, HCT, VHC, and VHCT Electrical Characteristics
     3.8.4 FCT and FCT-T
     3.8.5 FCT-T Electrical Characteristics
3.9 Bipolar Logic
                     145
     3.9.1 Diodes
                      3.9.2 Diode Logic
                                          3.9.4 Transistor Logic Inverter
     3.9.3 Bipolar Junction Transistors
     3.9.5 Schottky Transistors
3.10 Transistor-Transistor Logic
                                  156
     3.10.1 Basic TTL NAND Gate
     3.10.2 Logic Levels and Noise Margins
                                              3.10.3 Fanout
     3.10.4 Unused Inputs
                              3.10.5 Additional TTL Gate Types
3.11 TTL Families
                                   3.11.2 Schottky TTL Families
     3.11.1 Early TTL Families
                                              3.11.4 A TTL Data Sheet
     3.11.3 Characteristics of TTL Families
3.12 CMOS/TTL Interfacing
3.13 Low-Voltage CMOS Logic and Interfacing
                                                171
                                                3.13.2 5-V Tolerant Inputs
      3.13.1 3.3-V LVTTL and LVCMOS Logic
                                    3.13.4 TTL/LVTTL Interfacing Summary
     3.13.3 5-V Tolerant Outputs
      3.13.5 2.5-V and 1.8-V Logic
3.14 Emitter-Coupled Logic
                                  3.14.2 ECL 10K/10H Families
      3.14.1 Basic CML Circuit
                                  3.14.4 Positive ECL (PECL)
      3.14.3 ECL 100K Family
              183
References
Drill Problems
                 184
Exercises
             188
COMBINATIONAL LOGIC DESIGN PRINCIPLES
                                                        193
                          194
4.1
      Switching Algebra
                       4.1.2 Single-Variable Theorems
      4.1.1 Axioms
      4.1.3 Two- and Three-Variable Theorems
      4.1.4 n-Variable Theorems
                                   4.1.5 Duality
      4.1.6 Standard Representations of Logic Functions
4.2 Combinational-Circuit Analysis
                                      209
     Combinational-Circuit Synthesis
                                        215
4.3
                                               4.3.2 Circuit Manipulations
      4.3.1 Circuit Descriptions and Designs
                                                  4.3.4 Karnaugh Maps
      4.3.3 Combinational-Circuit Minimization
                                           4.3.6 Simplifying Products of Sums
      4.3.5 Minimizing Sums of Products
      4.3.7 "Don't-Care" Input Combinations
      4.3.8 Multiple-Output Minimization
      Programmed Minimization Methods
                                           236
      4.4.1 Representation of Product Terms
      4.4.2 Finding Prime Implicants by Combining Product Terms
      4.4.3 Finding a Minimal Cover Using a Prime-Implicant Table
      4.4.4 Other Minimization Methods
```