BCTM PROCEEDINGS

# PROCEEDINGS OF THE 1994 BIPOLAR/BiCMOS CIRCUITS AND TECHNOLOGY MEETING

# 1994


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# PROCEEDINGS OF THE 1994 BIPOLAR/BiCMOS CIRCUITS AND TECHNOLOGY MEETING

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EDITED BY C. R. SELVAKUMAR

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# Welcome to the 1994 Bipolar/BiCMOS Circuits & Technology Meeting

The remarkable progress made in Bipolar/BiCMOS technologies in the early part of the nineties, an age emerging with a major accent on low power, nomadic, information super processing, is both fascinating and challenging. In the midst of vigorous challenge from CMOS, the bipolar/BiCMOS technologies are marching ahead with commercial launching of Multi-Gigabits/s Bipolar Gate Arrays and complex BiCMOS microprocessors at blazing speed, not to mention the impressive analog products and 200mm wafer SiGe technologies. Entering the ninth year, the 1994 BCTM continues to serve as a primary forum for discussing the advances made in the area of bipolar/BiCMOS technologies.

This year's program begins with a keynote address by David Fullagar of Maxim, entitled "The Future of Bipolar in Analog ICs." He will talk about a second renaissance of analog bipolar ICs in the offing and the interesting challenges and opportunities ahead. At Monday's luncheon talk, John Shier of VTC will present the intricate interdisciplinary nature of complexities and challenges of disk drives, a $25billion/year market.

The double-length invited tutorial/review paper sessions continue to be a popular feature of this conference. We have five interesting invited tutorial/review papers to be presented by leading experts. John Prince of the University of Arizona will present a talk on modeling of interconnects. The issues in the design by simulation as applicable to BiCMOS will be discussed by Jeffrey Frey of the University of Maryland. Greg Taylor on Intel will present circuit techniques for high fan-in, dynamic BiNMOS gates and its application in the 90 MHz and higher speed microprocessors. Analog BiCMOS circuit design techniques are discussed by Sone and Yatsuyanagi of NEC. Where Silicon-Germanium HBT technology is heading, and its role in the RF to millimeterwave spectrum of frequencies, including the recent work by Bernard Meyerson's group at IBM, will be discussed by Christian Kermarrec of Analog Devices.

There are two exciting evening panel discussions planned for this year. The first one is on Low Power Design, organized by Tom Fletcher of Intel, and the second one, organized by David Harame of IBM and Alan Solheim of BNR, is on, "Is SiGe a Laboratory Curiosity or Something Real?"

Of the total number of abstracts submitted, 55% were accepted for presentation. This year, we received 55% of the abstracts from industry and 45% from universities. The regional distribution of abstracts received is as follows: 52% from the USA and Canada, 26% from Japan and Asia, 20% from Europe and 2% from elsewhere, which includes a paper from New Zealand.

We thank the committee members for their enthusiastic contributions and strongly encourage your active participation in this years BCTM.

C. (Selva) R. Selvakumar (Program Chairman) & John Shier (General Chairman)

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# 1994 BCTM SCHEDULE AT A GLANCE

**SUNDAY - OCTOBER 9**
Registration & Social Hour - Ballroom 1 - 7:00 PM

**MONDAY - OCTOBER 10**
Registration opens at 7:30 AM in the Ballroom Foyer

| | | | |
|---|---|---|---|
| Opening Remarks & Annoucements | Ballrooms 1 & 2 | | 8:30 AM |
| KEYNOTE SPEECH: "The Future of Bipolar Analog ICs" | Ballrooms 1 & 2 | | 8:45 AM |
| 20 Minute Break: Coffee & Rolls in the Foyer | | | 9:30 - 9:50 AM |
| I. Analog 1 Ballroom 3 | II. High Performance BiCMOS Ballroom 4 | III. I.C. Modeling Fifth Season | 9:50 AM - Noon |
| LUNCHEON TALK "A Fast Spin on Disk Drives" | | | 12:00 PM |
| IV. IC Bipolar Transistor Technology Ballroom 3 | VI. High-Speed Digital Ballroom 4 | VIII. Power and Thermal Effects Fifth Season | 1:45 - 3:25 PM |
| V. Analog BiCMOS Ballroom 3 | VII: High Performance ECL Ballroom 4 | IX. Characterization Ballroom 1 | 3:35 PM - 4:50/5:15 PM |
| Author Interviews Immediately After Sessions | | | |
| DINNER BREAK | | | |
| Panel A Low Power Design Ballroom 3 | Panel B - SiGe: Laboratory Curiosity or Something Real? Ballroom 4 | | 8:00 PM |

**TUESDAY - OCTOBER 11**

| | | | |
|---|---|---|---|
| X. Analog II Ballroom 2 | XII. Device Simulation Ballroom 3 | XIV. Bipolar Process Integration Ballroom 4 | 8:30 - 10:10 AM |
| XI. Analog III Ballroom 2 | XIII. Stress & Reliability Ballroom 3 | XV. Process Integration Issues Ballroom 4 | 10:20 AM - Noon |
| Author Interviews Immediately After Sessions | | | |

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**Monday, October 10, Ballroom 3**
Co-chairs: Masahiko Nakamae (NEC), John Shott (Stanford)



**Session V: ANALOG BiCMOS**
**Monday, October 10, Ballroom 3**
Co-chairs: Derek Bowers (Analog Devices), Bob Pease (National)

**Session VI: HIGH-SPEED DIGITAL**
**Monday, October 10, Ballroom 4**
Co-chairs: Tony Brown (Northern Telecom), Dan Hopta (DEC)



**Session VII: HIGH-PERFORMANCE ECL**
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**Session VIII: POWER AND THERMAL EFFECTS**
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Co-chairs: Ron Schrimpf (U. of Arizona), Colin McAndew (AT&T)

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**Tuesday, October 11, BALLROOM 4**
Co-chairs: Tom Long (AT&T), Tad Yamaguchi (Maxim)



**Session XV: PROCESS INTEGRATION ISSUES**
**Tuesday, October 11, BALLROOM 4**
Co-chairs: Hiroshi Iwai (Toshiba), Scott Robins (Cypress)

# A 14-b 2.5 MSPS Pipelined ADC With On Chip EPROM

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## ABSTRACT

A 14-b 2.5-MSPS, multi-stage pipeline, subranging analog-to-digital converter is presented. In addition to conventional laser-wafer-trim, on chip, "write once" EPROM is used to calibrate inter-stage gain errors at package sort. Integral nonlinearity errors as small as +/- 2LSB, and differential nonlinearity errors of -0.6, +0.8 LSB have been achieved. The 5.4 mm by 4.4 mm device includes a 2.5-V reference is built on a 2-um 10-V BiCMOS process and consumes 550 mW of power.

## Introduction

Applications such as high end still imaging (CCD and PMT) systems and high data rate digital communications over twisted pair (ADSL) require converters with dynamic range higher than 12 bits. Also the conversion rates required are beyond what presently available monolithic converters with more than 12 bits offer. High resolution, high sample rate converters have been reported. A 15-b ADC [1] samples only up to 1 MSPS, lacks much of the digital calibration circuitry and consumes 1.8 watts. A 2.5 MSPS ADC [2] has only 13 bit resolution. Other 14-b converters with conversion rates greater than 1 MSPS are available as multi-chip hybrids. These converters are in relatively large packages and can consume more than 2 watts of power.

A monolithic 14-b 2.5 MSPS ADC, with a fast acquisition time of less than 200 nSeconds combined with 110 uV rms total noise, has been developed on a 2 micron 10 V BiCMOS process. The converter dissipates only 550 mW from +/- 5 volt power supplies and is packaged in a 44 pin PLCC package. The process includes laser trimmable thin film resistors, double poly capacitors in addition to 2 GHz ft NPN devices and 2 micron CMOS. The double poly feature has been used to fabricate a simple floating gate NMOS "write once" EPROM structure. The EPROM calibration is used to insure linearity at the 14-b level after packaging.

## Functional Description

The design (block diagram shown in figure 1) extends and integrates proven circuit techniques to provide a complete monolithic converter function. A low noise, self-correcting, frontend sample-hold amplifier from [3] has been extended to improve settling time from 12 bits in 250 nSeconds to 14 bits in less than 200 nSeconds and to lower its noise below 80 uV rms for use in this 14-b ADC. The converter is a multi-stage pipeline design with 5 stages of Flash/DAC/SHA and a final 6th Flash. The flash resolution for the stages is 4-3-3-3-3-3. One bit of overlap between stages is used for error correction. The choice of the number of bits to use in first stage is based on matching requirements for 14 bit linearity. The advantages of a less complex design are possible if all the stages in the pipeline are the same number of bits. With 4 bits in the first stage, only way to end up with 14 bits after digital error correction is to have all the rest of the stages be 3 bits per stage.

To economize on power, only the frontend SHA, first flash and DAC, where the highest dynamic range is needed, use the full +/- 5 volt power supplies. The second SHA (which is in stage1) and stages 2-6 operate from only the +5 analog power supply. The DACs and SHAs in these single supply stages are based on a high speed low power design presented in [4]. The total power has a design center of just over 500 mW at room temperature. About 1/2 of the total power is used in the frontend SHA and first stage Flash/DAC/SHA.

### Lowering The Input Noise

The input SHA is based on an architecture from [3]. The block diagram of the SHA is shown in figure 2. In a SHA there are two modes of operation, sampling the input and holding a sample on the output. The wide band noise seen in the output is the combination of the noise present across the hold capacitor at the moment of sampling and the noise present while in hold mode. The former of these two is often the largest contributor. The designer must identify the important noise sources to tackle problem.

To understand the performance of this circuit the following is a quick look at its operation as it impacts the noise. When sampling the input, switches S1, S2 and S3 are closed with S4 open. Because S1 is closed around amplifier GMamp, the bottom of capacitor Chold is held at a virtual ground. The top of Chold is driven to the input by buffer Buff1 through switch S3. The major contributors to the noise across Chold in this mode are Buff1 as it drives the top and GMamp which is driving the bottom. The noise contribution from the on resistance of the switches can be made low enough by sizing as not to be significant, and Buff2 is not in the signal path.

These two amplifier stages must be designed to optimize the trade-off between noise and signal bandwidth. It is desirable to have Buff1 be as wide band as possible for two reasons, fast acquisition of the input and stability while in hold mode. However, wide bandwidth also contributes more noise. The same is true of the amplifier GMamp. A significant portion of the power is used in this SHA to provide both low noise and wide bandwidth and fast settling time. The noise was reduced from 170uV in [3] to 80uV.

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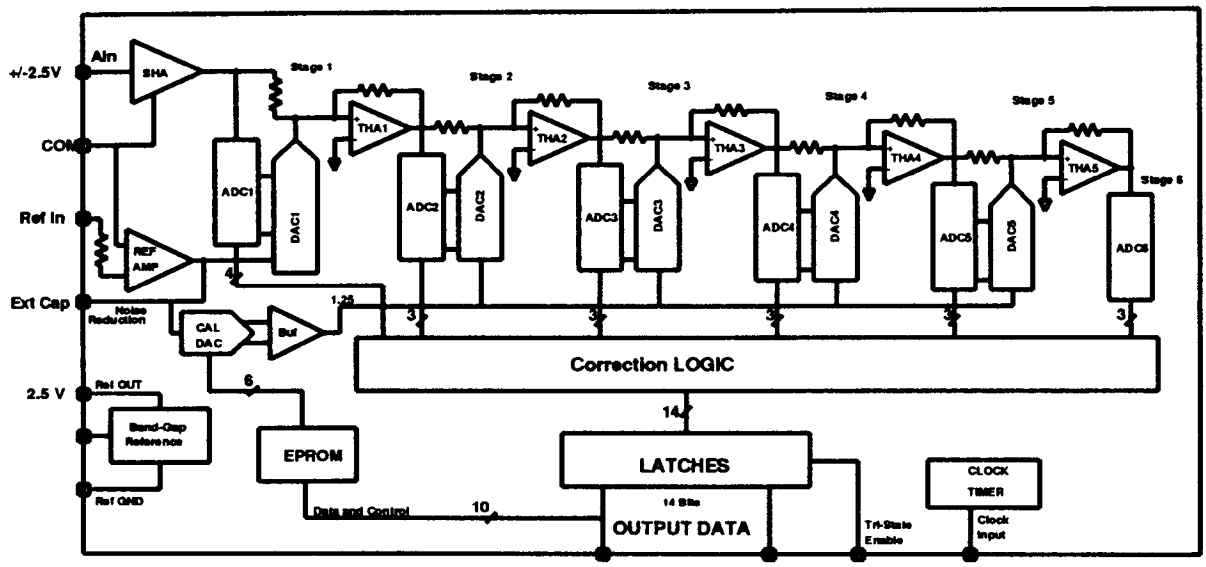


Figure 1 Block Diagram

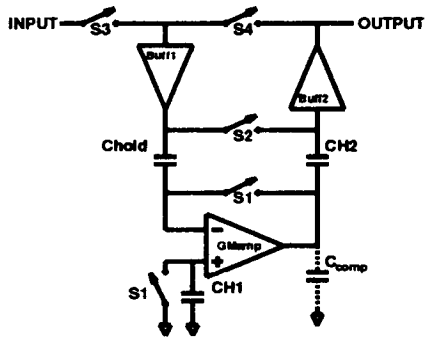


Figure 2 Sample and Hold Amplifier

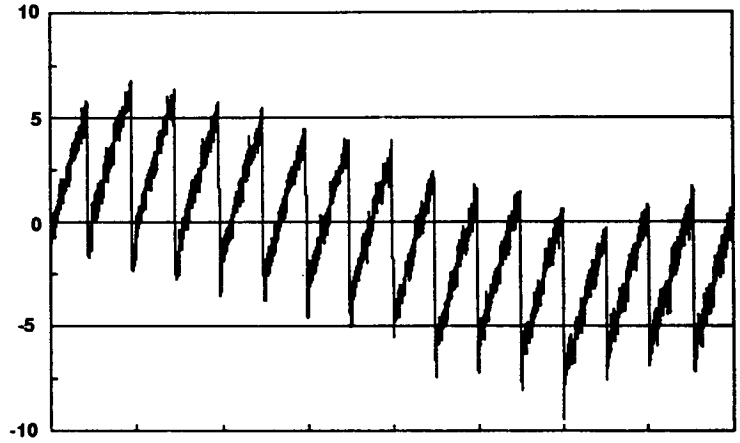


Figure 3a
INL with Inter-stage gain error

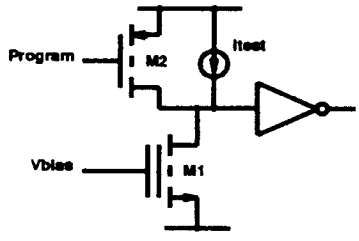


Figure 4 EPROM Cell

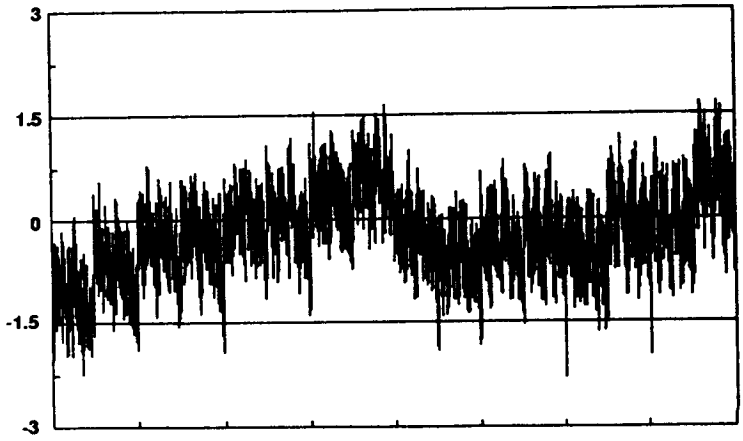


Figure 3b
INL After Inter-stage gain calibration