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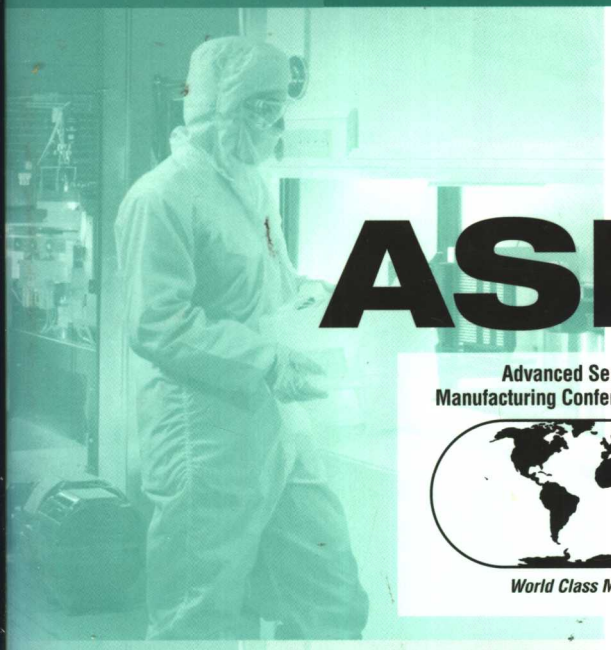

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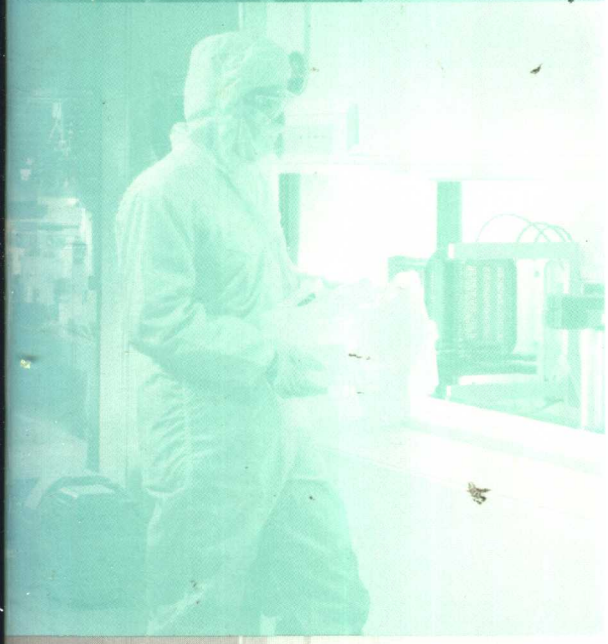

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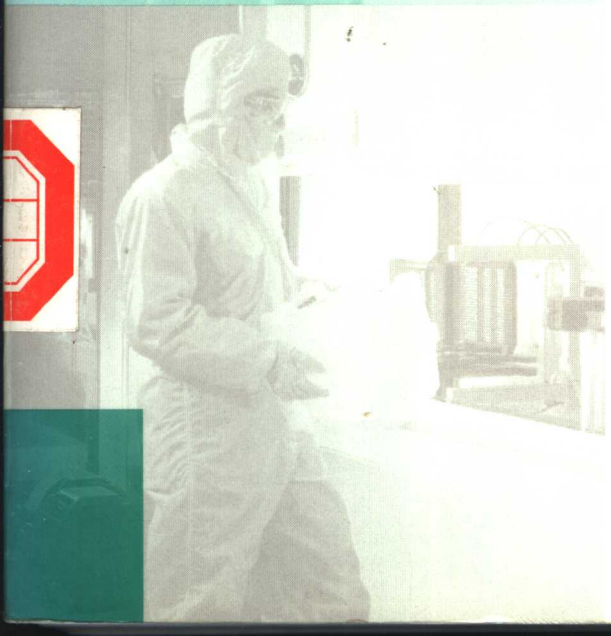

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In-line electrical characterization of ultrathin gate dielectric films

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Abstract

In this paper, in-line measurements of ultrathin gate dielectrics are reported. Various plasma nitrided oxides down to 1.5 nm EOT have been studied using in-line optical and non-contact electrical measurement techniques. The good correlation obtained with physical analysis and "classic" capacitance-voltage measurements shows the suitability of in-line measurement techniques for a first qualitative evaluation of ultrathin dielectric films.

Keywords

Nitrided oxide, plasma nitridation, gate dielectric, in-line characterization, Quantox, capacitance, EOT.

Introduction

Progress in CMOS technology has been dominated by the scaling down of device feature sizes. One of the many challenges in CMOS scaling is the continued increase of the gate dielectric capacitance per unit area. This can be accomplished by either reducing the gate dielectric thickness or increasing the gate dielectric constant (ε_r). For rapid assessment and optimization of new gate dielectric materials such as nitrided silicon oxide, a reliable in-line characterization of these ultrathin films is required [1]. This work presents results from in-line optical and electrical characterization of heavily nitrided oxides formed in a rapid thermal processing (RTP) chamber with plasma nitridation (PN) capability. In addition, the obtained results are compared to conventional physical and electrical characterization.

Experiment

In this study, ultrathin nitrided oxides were grown on high quality p-type Si (100) wafers. The bottom silicon oxide was grown using a rapid thermal oxidation (RTO) or an in-situ steam generation (ISSG) oxidation and was followed by a plasma nitridation. Two different nitridation techniques have been studied (PN1 and PN2). The oxynitrides received a post anneal at 1000°C under N_2 for 60 seconds and 1000°C under O_2 for 15 seconds for PN1 and PN2 nitridation, respectively. Table 1 summarizes the different conditions and variants used for this experiment.

Base oxide RTO/ISSG	Plasma nitridation	
	PN1	PN2
950°C	550°C, 240 sec, 3 Torr	27°C, 15 sec, 25mTorr
12 Å	20 % He	
13 Å	20, 40, 60, 80 % He	
15 Å	20, 40, 60, 80 % He	95 % He
16 Å	20 % He	
20 Å	20 % He	

Table 1: Process conditions used for the oxidation and the plasma nitridation.

In-line optical measurements were performed using the KLA-Tencor ASET-F5 and physical analysis were performed using X-ray Photoelectron Spectroscopy (XPS). In-line electrical measurements were performed using the KLA-Tencor Quantox. The Corona-Oxide-Silicon (COS) Quantox system [1] is based on combining three non-contacting technologies: charged corona, vibrating Kelvin probe and a pulsed light source, as shown in Figure 1. Charged corona ions provide biasing and emulate the function of the gate electrode of the Metal Oxide Semiconductor (MOS) structure. The Equivalent physical Oxide Thickness (EOT) parameter is determined from dielectric capacitance. The capacitance is determined from dQ/dV in accumulation in the COS system. The capacitance is

converted to thickness using ε_r = 3.9. Some second order corrections can be applied to acquire data to account for semiconductor band bending.

After completion of MOS capacitor fabrication, conventional, Capacitance-Voltage (C-V) measurements were performed on capacitors of 100 μmx100 μm. The C-V EOT was extracted using the CVC modeling program from NCSU [2], accounting for polysilicon depletion of gate electrode and quantum mechanical effects in substrate.

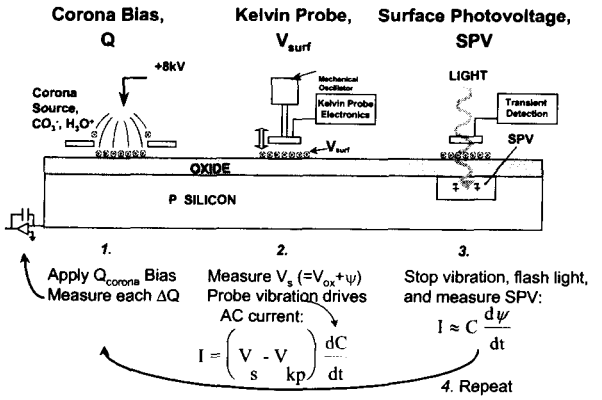

Figure 1: Quantox COS measurement theory.

Results and Discussion

In-line electrical measurement of the EOT of ultrathin dielectric films has been performed using the Quantox. The stability of the in-line EOT measurement has been assessed, and determined to be 3σ < 0.4 Å static repeatability. The repeatability data is presented in Figure 2.

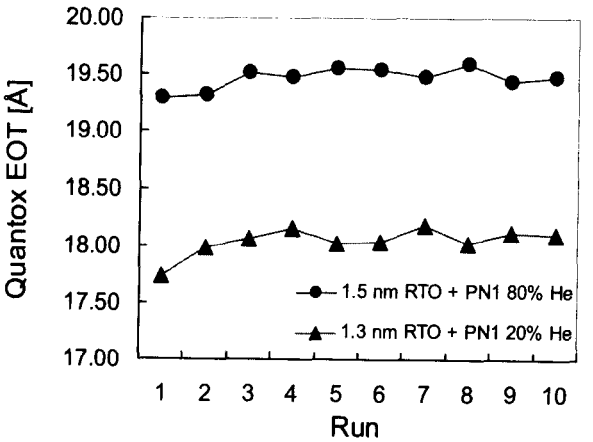

Figure 2: Stability of the Quantox EOT. The measurement of the EOT of two different dielectrics has been repeated ten times. The 3-sigma variation is less than 0.4 Å for both EOTs.

Based on the optical thickness and the EOT measured respectively with the ASET-F5 and the Quantox, the physical thickness and dielectric constant of the ultrathin nitrided oxides have been estimated. For this purpose, some basic assumptions have been made: a linear transition on optical constant (n) from pure oxide (SiO_2) to pure nitride (Si_3N_4) (Equation 1) as well as a linear correlation of optical constant to dielectric constant (Equation 2) have been assumed using Palik optical tables (Table 2) [3].

$$T_{optical} = \frac{n}{n_{SiO_2}} T_{physical} \quad (1)$$

$$\varepsilon_r = 6.383 \times n - 5.4 \quad (2)$$

	n @ 633 nm	ε_r
Oxide	1.457	3.9
Nitride	2.021	7.5

Table 2: Palik optical tables for pure oxide and pure nitride.

Figure 3 shows a strong correlation of the estimated physical thicknesses with the thicknesses calculated from XPS analysis. This relation is diverging from a 1:1 correlation when the films get thinner. This might be attributed to the assumptions made to calculate the physical thicknesses (e.g. AMC noise on optical thickness measurements [4]) and/or to the XPS error

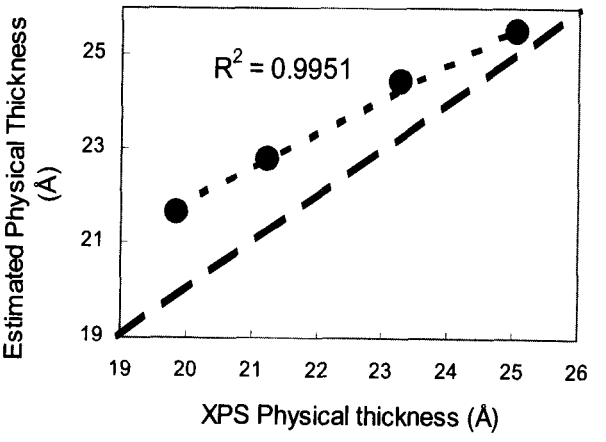

Figure 3: Correlation between the estimated physical thickness with the thickness calculated from XPS analysis of thin nitrided oxide films formed with a base oxide of 1.5nm followed by a plasma nitridation with different dilution ratio: 20, 40, 60, 80 % He.

Figure 4 shows that when the He dilution percentage (the dilution ratio in the PN chamber) is increased, both the physical thickness and the dielectric constant increase. A higher He dilution percentage in PN1 process results in more physical growth of the dielectric. The increase in dielectric constant with increasing N content is in accordance with previously published result [5] and with XPS measurements presented in Figure 5. Figure 5 confirms that a higher He dilution ratio causes an increase of the nitrogen content incorporated in the film, which leads to an increase of the dielectric constant.

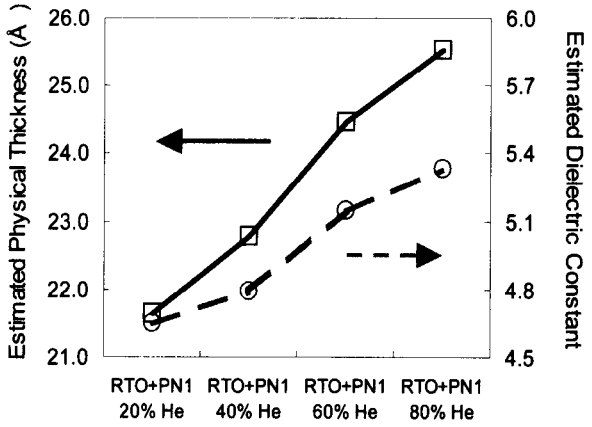

Figure 4: Estimated physical thickness and dielectric constant of nitrided thin films formed with a base oxide of 1.5 nm followed by a plasma nitridation (PN1) with different He dilution ratio.

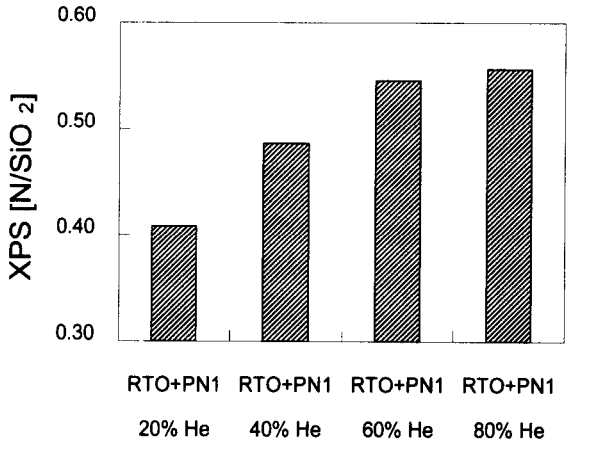

Figure 5: XPS measurements of the nitrogen content in nitrided oxide films formed with a base oxide of 1.5 nm followed by a plasma nitridation (PN1) with different He dilution ratio.

Dielectrics with various base oxide thicknesses followed by a common nitridation have been studied. The thinner the base oxide the more nitrogen is incorporated in the film, as shown in the literature [6]. The interface trap density in such films has been measured with the Quantox. A higher interface trap density has been measured for the thinner films which contain a higher amount of nitrogen. This is in accordance with previous work [7] showing that a large amount of charges (fixed charges, interface states) are incorporated in the dielectric during the plasma nitridation process. The higher Dit implies that the incremental N is located primarily at the Si-SiO_2 interface.

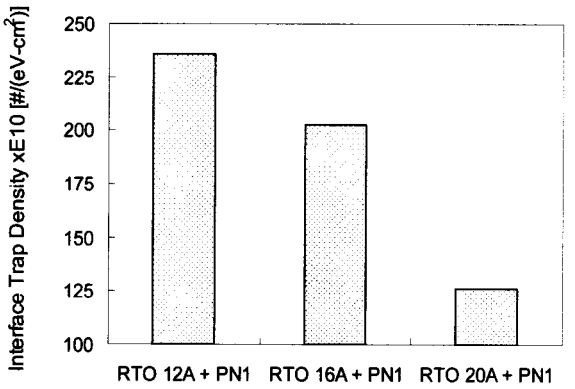

Figure 6: Interface trap density of nitrided oxide films formed with various base oxide thicknesses and followed by a common plasma nitridation (PN1).

Figure 6, in conjunction with Figures 4 and 5, illustrates the correlation between increases in He dilution, nitrogen incorporation, and interface states. The end-of-line electrical (transistor) interface trap density is less than in-line electrical (Quantox) [7], which is attributed to the additional high temperature processing beyond gate dielectric formation. The additional high temperature processing, and particularly the final forming gas anneal, seen by the end of line dielectric serves to reduce the interface trap density. Yet, the amount of nitrogen in ultrathin oxynitride films has been qualitatively measured by performing in-line electrical measurements.

Quantox mapping capabilities have been used to look at the non-uniformity of plasma nitridation PN1. Figures 7 and 8 show a radial pattern for respectively the surface voltage (Vs) and the surface photo voltage (SPV).

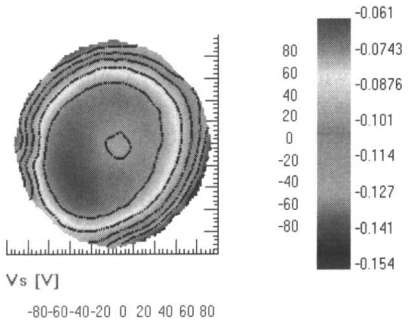

Figure 7: Surface Voltage (Vs) map of 1.5 nm RTO followed by PN1 with 80% He dilution ratio.

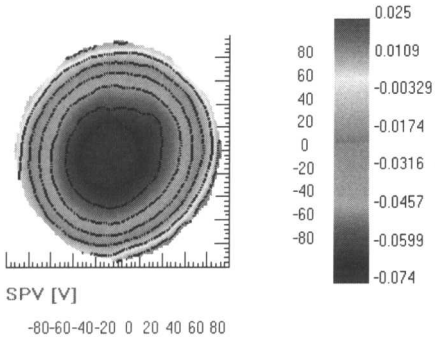

Figure 8: Surface PhotoVoltage (SPV) map of 1.5 nm RTO followed by PN1 with 80% He dilution ratio.

This non-uniformity has been quantified with 4-point measurements from the center to the edge of the wafer. The EOT values, measured with the Quantox or extracted from C-V curves using the CVC model, confirm the radial non-uniformity observed in the Vs and SPV maps (Figure 9). A variation of about 2 Å is observed from the center to the edge of the wafer. Further optimisation of the PN1 process conditions will be needed to address the non-uniformity issue. Figure 9 shows the correlation between the EOT measured on the Quantox and the EOT extracted from C-V curves. The minor differences seen between the two EOTs can be attributed to the extra processing steps needed to manufacture capacitors. Yet, these results show that it is possible to obtain in-line electrical test measurements that correlate strongly with conventional off-line C-V analysis.

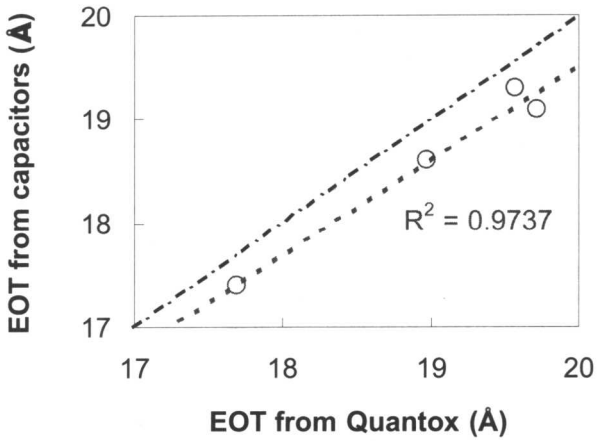

Figure 9: Correlation between the EOT measured with the Quantox and the one extracted from C-V curves using the CVC fitting model. This correlation is made for a 1.5 nm base oxide followed by PN1 with 80% He on four locations on the wafer.

Finally, in-line measurement of the EOT has been made for dielectrics with a fixed base oxide thickness followed by different nitridation processes: PN1 and PN2 (Table 1). The physical thickness, estimated using equations 1 and 2, was the same for the studied dielectrics while the dielectric constant was higher for the oxynitrides formed with PN2. Correlation of the EOTs and the amount of nitrogen in the films has been established, as presented in Figure 10. As expected [5, 8, 9], the higher the amount of nitrogen in the film, the smaller is the EOT. In this study, the lower EOT films were achieved with PN2.

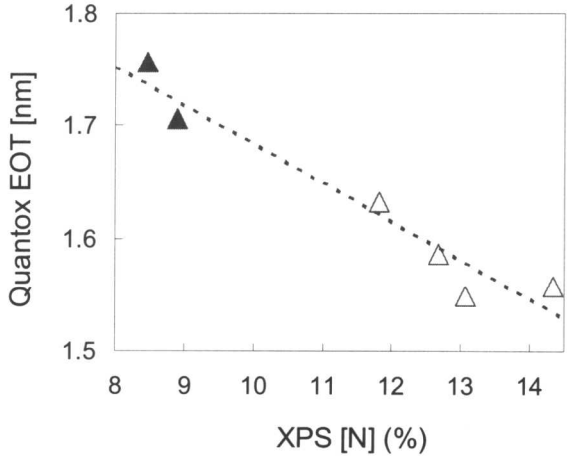

Figure 10: Amount of nitrogen in the oxynitride films as a function of the EOT measured with the Quantox. The dielectrics studied have the same base oxide thickness but various plasma nitridation processes: PN1 and PN2 (Table 1).

A comparison between the EOT measured with the Quantox and the EOT extracted from C-V curves is illustrated in Figure 11. Again, the differences seen between the two EOTs can be attributed to the extra processing steps needed to manufacture capacitors.

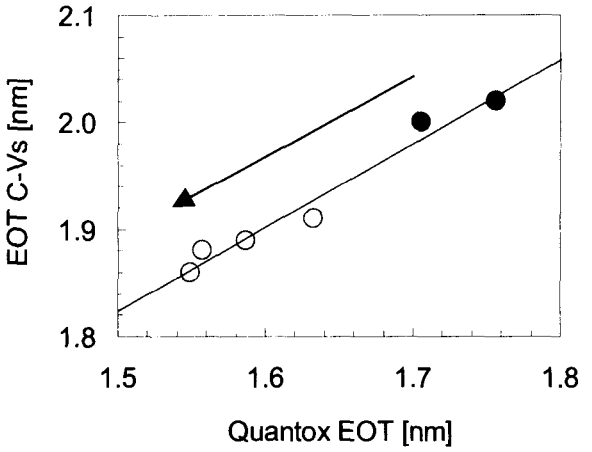

Figure 11 Correlation of the EOT measured with the Quantox and the one extracted from C-V curves using the CVC fitting model for dielectrics with different nitridation PN1 and PN2 (Table 1).

These results show that it is possible to obtain a correlation between in-line and off-line electrical measurements. This allows for a fast screening and first qualitative optimization of novel gate dielectrics.

Conclusions

In this paper, ultrathin plasma nitrided silicon oxide films have been characterized using in-line optical and non-contact electrical measurements. Two different plasma nitridation processes have been studied. The correlation obtained between the optical thickness, physical analysis, capacitor and Quantox measurements demonstrates that in-line electrical characterization is well suited for a first qualitative evaluation of ultrathin dielectric films.

The EOT of various dielectrics has been measured using the Quantox. A static repeatability 3σ better than 0. 4 Å was achieved. The physical thickness and the dielectric constant were estimated using in-line optical and electrical measurements and correlated to XPS analysis. The amount of nitrogen in ultrathin oxynitride films has been qualitatively measured by performing in-line electrical measurements. We found a correlation between increases in the He dilution ratio of the plasma nitridation process, nitrogen incorporation, and interface trap density. Finally, two different plasma nitridation processes were compared demonstrating the usefulness of in-line electrical measurements as a first optimisation of thin gate dielectrics.

Acknowledgement

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Alternative Smart-cut-like Process for Ultra-thin SOI Fabrication

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Abstract

We describe for the first time a layer transfer caused by delamination along the hydrogen platelet layer formed by RF plasma hydrogenation at a place of end-of-range defects. The process involves first creating a buried trap layer using variously silicon, or argon implantation. Wafers thus processed with an initial implant to levels below 10^{16} cm^{-2} are then hydrogenated with RF plasma. Next steps include pre-bonding, cleavage, and post-bonding as in the Smart-cut process. The cleavage occurs at a depth corresponding to the maximum of vacancy-enriched defects (between $R_p/2$ and R_p). Plasma hydrogenation may be used as a step in the process of fabricating thin SOI wafers.

Keywords

Silicon-on-insulator
Layer transfer
Plasma hydrogenation
Thin top layer SOI

1. Introduction

The International Technology Roadmap for Semiconductors 2001 [1] projects that the top silicon layer for SOI starting wafers will be 20 to 100 nm in thickness by 2004 to support processing of fully-depleted CMOS circuits. At the present time processes such as Smart-Cut™ provide an inherent silicon film thickness of about 500 nm and a minimum thickness of about 200 nm [2]. The thickness of the delaminated layer in the Smart-Cut process depends on the energy of implantation of hydrogen. When the energy of the hydrogen implant is reduced to levels below 50 keV to achieve thin delaminating thickness problems arise [3 - 5]. Attempts have been reported to thin the surface silicon layer of Smart-cut processed wafers to obtain SOI wafers with surface films of less than 200 nm thickness. Terreault et al. [3 – 5] used low energy hydrogen implantation (5 to 8 keV) in a regular Smart-cut to get a thinner top SOI layer. They report blistering the thin layer, but do not describe the layer transfer. Maleville at al. [6] reports 70 nm top Si SOI using touch polishing of an initial 500 nm layer. Srikrishnan [7] forms an etch stop layer inside of the transferred with Smart-Cut silicon film by implantation into the top silicon layer with a subsequent etching. Popov [8] reports a layer-by-layer oxidation (of the film transferred with Smart-cut) with subsequent stripping in diluted HF for thinning of the layer. All listed approaches increase SOI wafer production cost and degrade thickness uniformity. Our work here reports the utilization of RF plasma hydrogenation as a post process following a low level implant to create the desired surface layer of thickness less than 100 nm.

2. Experimental

Silicon wafers were ion implanted with silicon, argon, or hydrogen to form a buried trap layer for hydrogen. Then the as-implanted wafers were hydrogenated in an RF plasma setup Tegal-100 at hydrogen pressures of 0.5 to 10 Torr and an RF power of 300 Watts. Importantly, the RF plasma processing is performed in two temperature regimes: a first step 200°C or less and a second step at 300°C or more. Pre-bonding, cleavage, and post-bonding steps were performed according to the as in the Smart-cut process. The thickness of transferred layers was measured with a Dektak profilometer near wafer edges where the layer transfer fails. Infrared absorbtion measurements were performed using both transmission and multiple internal reflection geometries [9] to gain access to both bonding and stretching vibrations of trapped hydrogen.

3. Results

The layer transfer occurs in cases of proper selection of implantation conditions and plasma hydrogenation conditions. A typical edge profile of the transferred layer is shown on Fig.1. The thickness of the

transferred layer is 75 nm. The donor wafer properties, implantation, and plasma hydrogenation conditions are listed in the Table below.

Table

Wafer	
Diameter	100 mm
Growth	Czochralski
Dopant	Boron
Resistivity	1 Ohm cm
Implantation	
Specie	Silicon
Energy	180 keV
Dose	$2x10^{15}$ cm^{-2}
Hydrogenation	
Source	RF plasma
Plasma power	300 Watts
Temperature, 1st step	200°C
Duration, 1st step	1 hour
Temperature, 2nd step	350°C
Duration, 2nd step	1 hour

The profile is shown in Fig.1 for the silicon-into-silicon implantation for trap layer formation. In this case the surface silicon layer is 75 nm in thickness. Similar results are obtained for some other heavier ions that penetrate less deeply.

Infrared absorbtion measurements taken on samples annealed up to 300°C during the second plasma immersion step indicate that hydrogen is primarily located on internal surfaces, with some H still in monovacancy-type defects such as VH and VH_3. This finding is consistent with previous studies [9]. Further studies are under way to characterize the nature and location of hydrogen incorporated in the silicon as function of processing conditions.

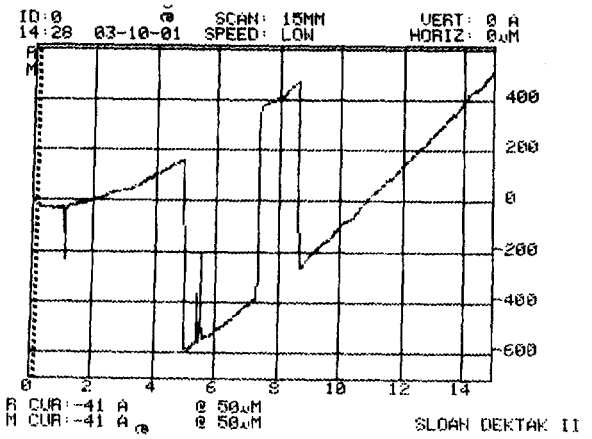

Fig.1 Profile near the edge of transferred layer.

4. Discussion

Our previous work [10] we reported silicon flaking along a hydrogenated trap layer. We used electrolytic hydrogenation. In the present paper we present results using plasma instead of electrolytic hydrogenation.

Hydrogen in atomic form is known for its high diffusivity in silicon and its ability to combine with many types of defects in crystalline silicon. It has been known since 1987 that plasma hydrogenation of single crystalline silicon can result in the formation of hydrogen platelets [11,12]. Because of the lack of defects in silicon bulk and low hydrogen solubility in silicon, the platelets in [11,12] are found in near-surface defect-rich regions only. To control the process of hydrogen platelet distribution in silicon, an additional step in the formation of the defect-rich layer is needed. To accumulate hydrogen in the desired part of the wafer we need to pre-form defects that readily interact with hydrogen. Silicon-into-silicon implantation forms a dense defect layer at desired depth under the surface.

An inherent delaminating thickness for either Smart-cut or the trap-filling processes is controlled by implantation depths [3, 6, 8]. For Smart-cut the depth is the R_p of hydrogen while for the trap-filling process is between $R_p/2$ and R_p for heavier ions. Correspondingly, the layer transfer depths are 200-2000 nm, and 20-200 nm. Therefore, the trap-filling process is advantageous for making thin SOI.

At the beginning of plasma hydrogenation, atomic hydrogen diffuses through silicon and attaches to broken bonds in a layer damaged by implantation [11]. The next step in hydrogen evolution is to form nuclei of hydrogen platelets. It happens at temperatures lower than 250°C as previously found by Johnson et al. [12]. Further hydrogenation increases the platelet size and can be done at higher temperatures. Higher temperature during the second stage of hydrogenation is also needed to allow Oswald ripening during which time bigger platelets grow at the expense of smaller ones [12].

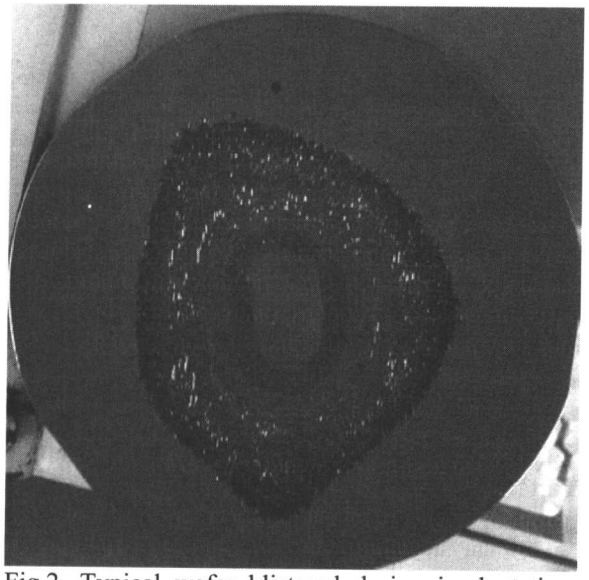

Fig.2. Typical wafer blistered during implantation. Implantation conditions: H_2^+ at 100 keV, 0.3 mA.

Experiments with blistering were widely used elsewhere to understand phenomena involved in the Smart-cut [3, 9, 14] process. At the level of hydrogen implantation required in Smart-cut (i.e. about $4x10^{16}$ cm^{-2}), the silicon surface easily blisters during implantation (Fig.2), even without an additional annealing. The silicon wafer surface can be also blistered after RF plasma hydrogenation. An interesting feature is that the minimum hydrogenation time in RF plasma required for blistering is several times longer, than the time required for successful layer transfer. Typical blistering picture after RF plasma hydrogenation and subsequent anneal is shown on Fig.3 and Fig.4. It was found that the hydrogen implantation dose needed for blistering is about the same as the dose required for layer transfer (for the same annealing temperatures). We suppose, that in our case there is much higher hydrogen loss due to outdiffusion than for the case of blistering caused by high dose hydrogen implantation. These hydrogen losses may be due to the proximity of surface, or due to a difference in the type of the traps binding the hydrogen. When the hydrogen-rich layer (either obtained by trapping of by implantation) evolves into a quasi-continuous cleavage plane, the hydrogen atoms or ions detraps from one defect, diffuse to another defect with higher bonding energy, and get trapped again. In a case of high dose hydrogen implantation the higher mechanical stress is expected, so we expect more weakened silicon bonds, and higher bonding energy for hydrogen attaching to those sites.

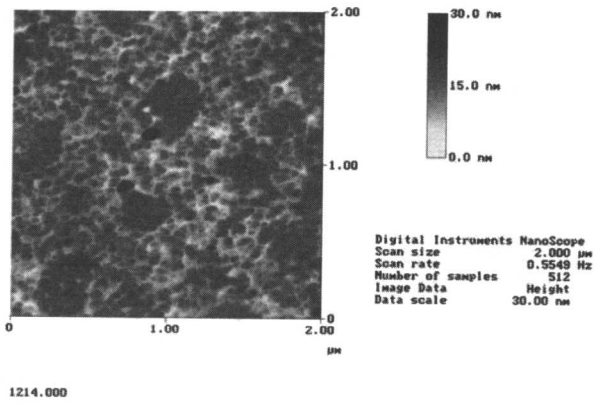

Fig.3. Surface relief developed on self-implanted silicon wafer after plasma hydrogenation, (area of view 2x2 μm^2).

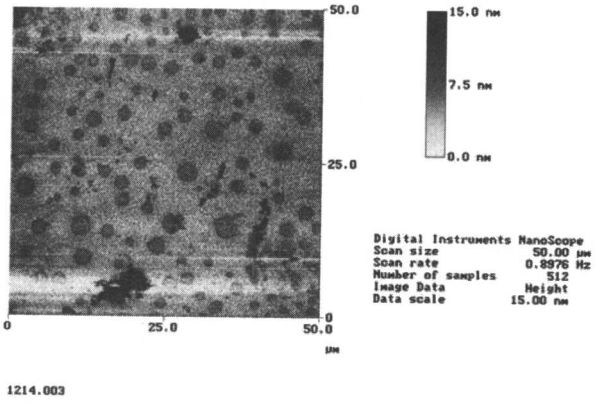

Fig.4. Surface relief developed on self-implanted silicon wafer after plasma hydrogenation, (area of view 50x50 μm^2).

Figures 3 and 4 show the surface of a wafer processed with self-implantation+hydrogenation. The surface is covered with features with lateral dimensions about 0.2 micron and vertical dimension about 5 nanometers. Infrared measurements show high hydrogen peak.

To keep the large amount of hydrogen inside the silicon wafer, the local temperature under the beam should not substantially exceed room temperature. This restriction severely limits the maximum hydrogen ion beam current during the implantation step in the Smart-cut process. For similar process work reported elsewhere [13-18] and by ourselves [19-26], the hydrogen beam current is limited to 0.1 mA using conventional implant equipment in order to maintain the lower implant temperatures. At this beam current density we require 24 hours to fully implant a wafer with hydrogen using the published

Smart-cut process making the process ineffective. Higher implant rates are possible using implanters with a special cooling system, but there are no published data yet that confirm efficiency of the cooling for this case. In our process, neither high dose implantation not hydrogen implantation are needed, thus making our process potentially advantageous. Also, the typical implantation doses needed to form the trap layer is lower than 10^{15} cm^{-2}, that might result in better crystalline quality of the top layer in the final SOI wafer as compared to the Smart-cut.

The RF plasma causes a platelet nucleation and growth along a layer at a depth of about ½Rp of the defect-inducing implant. The room temperature step of the plasma process is for nucleation, and the 300oC step is for fast growth, similar as in [4,5]. The surface features of Fig's 1 and 2 show smaller features by a factor of 10x and 100x for lateral and vertical dimensions, respectively, compared with laboratory results [2,3] obtained with heavy hydrogen implants.

4. Conclusion

RF plasma hydrogenation of a buried trap layer formed with low dose ion implantation has been demonstrated for forming silicon SOI with a thin top layer. Experiments described here indicate that the trap-filling process can provide a 10X reduction in SOI top layer thickness.

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A Manufacturable Shallow Trench Isolation Process for sub-0.2um DRAM Technologies

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Abstract

A highly manufacturable and defect-free shallow trench isolation (STI) process is demonstrated by using 64M DRAM as a sensitive monitor. In the STI flow, a special sequence of extra anneal (1100C) after corner oxidation (i.e., liner oxide) and an RTA (1000C) anneal after HDP CVD oxide deposition can result in a significantly higher yield in 64M DRAM by effectively reducing silicon stress related substrate defects.

Keywords

DRAM, STI, liner oxide, HDP CVD oxide, SiN pull-back

I. Introduction

Shallow trench isolation (STI) is the most favorable scheme for advanced CMOS technology (since 0.25um generation) due to its high scalability and excellent isolation capability [1-3]. One of the most critical issues of STI process [4-5] is the reduction of stress related defects as resulted from nitride and silicon trench etch, liner oxidation, HDP CVD oxide gap-fill, and more importantly those subsequent thermal cycles and high energy implants. The stress can result in defects later in the process, especially triggered by high energy Arsenic implantation for source-drain. Such defects lead to many undesirable effects (e.g. increasing diode leakage, punch-through in transistor, GIDL in pass transistor, degradation of refresh time in DRAM) leading to low yields. Recent studies discussed methods for reducing such STI related stress and defects in silicon by applying high-temperature annealing after device and gate formation [4-5]. However, these methods are not suitable for advanced CMOS, as they will increase dopant diffusion and serious short-channel effects.

This paper reports a highly manufacturable STI flow by using high-temperature annealing before device and gate formation. We have compared the process variables impacting the generation of STI defects, including flow sequence of corner oxidation and HDP CVD oxide densification. In addition, the effects of STI SiN pull-back and sacrificial oxide (SAC-ox) formation on the cell transistor performance and 64M DRAM CP1 yield are also studied.

II. Experiments

A brief description of the STI process flow used in this study is similar to conventional flow as sketched in Figure 1. After forming film stacks of pad oxide and nitride on substrate, a mask for defining active area (AA mask) is used by etching nitride, pad oxide and silicon substrate (Figure 1a). Then, a liner oxide is grown on the exposed substrate surface (Figure 1b). After the trench is filled by HDP CVD oxide (Figure 1c), a reverse AA (R-AA) masking step is performed (Figure 1d), and followed by plasma etching of HDP CVD oxide on the larger AA area. After photo-resist removal, oxide CMP is conducted (with nitride as a stop layer) for planarization (Figure 1e). Then the nitride layer is stripped by wet process to complete the STI fabrication (Figure 1f).

The key features of the DRAM vehicle used in this study are summarized in Table 1. The process technologies implemented include 3000A STI depth, retrograded triple-well, SAC (self-aligned contact) for storage node contact and bit-line contact, crown structure of cell capacitors, and tungsten bit-line.

Table 1. Key technology features of 64M DRAM in this study.

Minimum Feature	0.19 um
Minimum Pitch	0.44 um
Cell Structure	CUB
Isolation	STI
STI Trench Depth	3000A
Cell Size	0.387 um^2

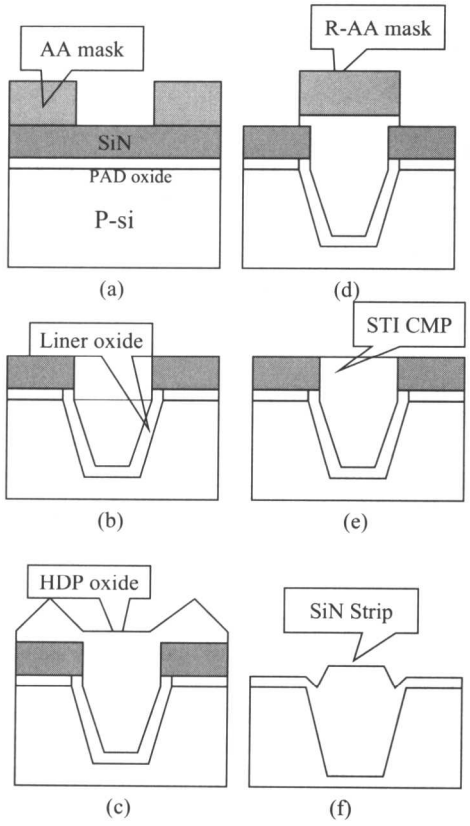


Figure 1: Illustration of key process steps for STI flow.

Additional process steps of STI nitride pull-back, annealing after liner oxide, RTA for HDP CVD oxide, and sacrificial oxide formation performed in this study are described below.

III. Results and Discussions

Effects of STI Process Sequences

Process variables impacting the generation of STI defects, including the flow sequence of corner oxidation and HDP CVD oxide densification are studied. Table 2 shows the split conditions of the present study for the STI liner oxide and HDP CVD oxide flow sequences. Wafer of Group-A was implemented with a high-temperature furnace anneal (1100C) after depositing STI HDP CVD oxide. In the Group-B wafer, the high-temperature furnace anneal (1100C) was used after STI corner liner oxidation, and a RTA annealing step was used to densify STI HDP CVD oxide.

The dependence of 64M DRAM CP1 yield on the STI flow sequence is shown in Figure 2. The major yield loss found in the Group-A process is related to the DC fail, as resulted from abnormal standby leakage current on the CP1 test.

Table 2. Split table for liner oxide anneal and HDP CVD oxide anneal in STI.

Flow	Split	Wafer #	
Liner Oxide Anneal	1100C furnace		B
	w/o	A	
HDP CVD Oxide Densify	1100C furnace	A	
	1000C RTA		B

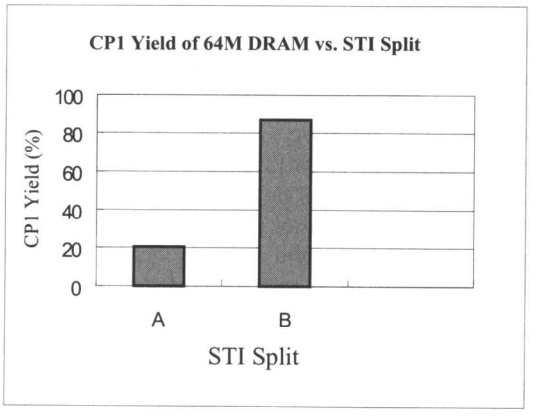
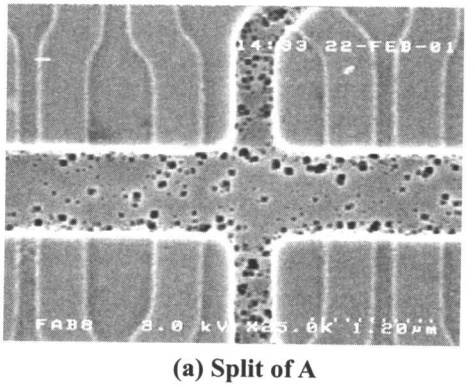


Figure 2: 64M DRAM's CP1 yield with STI flow splits (referred to Table 2).

To find out the root cause of the abnormal leakage current occurred in Group-A process, we checked the SEM plan view by using de-layering and Wright etching methods. Figure 3 shows the SEM results and the STI substrate defects can be easily found in the sense-amplifier (SA) area with N+ (As) implant in Group-A wafers (Figure 3(a)). However, Group-B wafers have no such substrate defects found in the SA area with N+ implant (Figure 3(b)). By using the STI process sequence of Group-B, the STI substrate defects can be effectively eliminated and a significantly higher 64M DRAM yield is achieved as shown in Figure 2.



(a) Split of A