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Preface

This proceedings contains the papers presented at the Third International Conference on CAD and Computer Graphics which will be held on August 23–26, 1993 in Beijing, China.

The response to the call for papers of this Conference was overwhelming. There are 227 papers from more than 20 countries and regions submitted to this Conference.

Paper selection was completed by the Program Committee of this Conference. The Committee was co–chaired by Professors Zesheng Tang and Jose L. Encarnacao. Every paper was reviewed by at least two committee members and was reviewed by a third referee if the two original reviews differed. Special effort was made to have committee members reviewing papers in their area of expertise. After the reviews were completed, the Program Committee had a meeting in January 13–14, 1993 in Beijing to discuss and decide the acceptance and rejection of reviewed papers. As the result, 166 papers were accepted for presentation at this Conference and publication in this proceedings.

All the papers in this proceedings are categorized in to the following 8 subject areas:

- Computer Graphics
- User Interface
- Computational Geometry
- Geometric Modeling
- Electrical CAD and CAT
- Intelligent CAD
- CAD Application
- Image Processing and Multimedia

The papers are compiled in accordance with the above group classifications and the sequence of their presentation at the Conference.

The basic goal of this Conference is to promote international scientific information exchange among scholars, experts, researchers and developers in the fields of CAD and Computer Graphics. I would like to express appreciation to the invited speakers for their interesting presentations on advanced research work and application in CAD and Computer Graphics. I world like to take this opportunity to repeat my warmest thanks to the authors of all the papers for their contributions to this Conference.

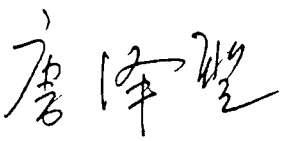
The large number of submissions exacerbated the normally tedious task of paper selections. The committee members and reviewers must be recommended for their extensive efforts.

I world like to express thanks to Professor Jose L. Encarnacao for his help in papers submissions and paper reviews and his guidance throughout the process for putting these papers together.

Before the publication of this proceedings, I world like to express sincere appreciation to Ms. Wei Yang for her extensive work in collection papers, sending the information into computer and verification of printing quality. In addition, my students, Mr. Zhigang Xiong, Weidong Min,

Yong Zhou and others have done a lot of work for the publication of this proceedings. Otherwise, it is impossible to publish this technical documentation.

Finally, I wish to express many thanks to the International Academic Publishers for the quality and appearance of this proceedings.



Zesheng Tang
Co–chairman of Program Committee
CAD / Graphics'93

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PERFORMANCE-DRIVEN CLOCK NET ROUTING

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ABSTRACT

Many existing zero-skew clock net construction algorithms have focused on minimizing the wire length in Manhattan space. However, for performance-driven designs, as microelectronic manufacturing technology advances, routing can be performed in non-Manhattan spaces as well. Consequently, we propose a *general* algorithm for zero-skew clock net synthesis, which works in any routing space. We first devise a simulated annealing approach to construct a zero-skew clock tree under the Elmore delay model. A simple yet powerful tree grafting scheme is designed as the perturbation function to generate new neighborhood configurations in the annealing process. Additionally, we propose a Steiner point placement optimization procedure to refine the results generated by the previous stage. Experimental results show that our algorithm can achieve average wire length savings of 23.95% compared to those of the previous best work based on the same benchmarks.

INTRODUCTION

The increase in complexity of synchronous VLSI systems and Multi-Chip Modules (MCMs) has made the clock signal distribution an important limiting factor of performance enhancement. This is revealed by inequality (1) determined the clock cycle, C_P, of a synchronous system:

$$C_P \geq t_d + t_{skew} + t_{su} + t_{pd}; \qquad (1)$$

t_d is the longest path delay through the combinational logic; t_{skew}, the clock skew, is defined as the maximum difference in arrival times from the clock source to sinks; t_{su} is the set-up time of the synchronizing elements; t_{pd} is the propagation delay within the synchronizing elements[9]. Bakoglu[1] has indicated that t_{skew} may account for more than 10% of the system cycle time in high-performance systems. Advances in VLSI fabrication technology are making feature sizes smaller. Hence, t_{su}, t_{pd}, and t_d will be reduceed significantly making clock skew a more dominating factor in performance consideration.

The H-tree approach[1,19] is able to minimize the clock skew successfully when the sinks are identical and are placed in a symmetric array. Jackson et al.[9] generalized the H-tree approach for asymmetric clock sink distributions in the MMM (Method of Means and Medians). Kahng et al.[11] then proposed a recursive geometric-matching algorithm which reduces the wire length of MMM solutions by 5% to 7%. Since length reduction methods such as H-flipping and edge uncrossing are used in their algorithm, it has exponential time complexity. Li and Jabri[13] reduceed the time complexity of the previous algorithm to $O(n^2 \log n)$ using the Voronoi diagram. The algorithm also achieved an average 8% wire length savings over those of Kahng et al. by adding optimization techniques such as L-shaped pairing. However, all these algorithms[9,11,13] balance the wire length rather than balance the real clock delay.

Tsay[17] initiated a new era for zero-skew clock net routing algorithms by devising a zero-skew merging scheme using the Elmore delay model for delay approximation in addition to length-balancing. The algorithm recursively combines a pair of zero-skew subtrees at a *tapping point* to produce a larger zero-skew tree. However, the total wire length is not optimized. Although a skew-free clock circuitry significantly enhances a system's performance by eliminating t_{skew} from the clock cycle inequality (1), total wire length is still a critical parameter. Excess interconnect not only increases layout area and reduces the overall routability, but also results in greater net capacitance, hence requiring more power for clock signal distribution.

Consequently, Chao et al.[4] proposed a two-phase algorithm which achieves an average 10% wire length reduction from that of Tsay based on the same benchmarks in Manhattan space. Since, in Manhattan space, the set of tapping points satisfying the zero-skew property with respect to the two given children is a line segment, a "tree of merging segments" can be built bottom-up by using the same zero-skew merging scheme proposed by Tsay[17]. Then a *delayed merging method* is applied to the tree of segments, with the freedom of choosing different merging positions on each merging segment, to minimize the wire length while maintaining the skew-free environment. Boese and Kahng[3] independently developed a *DME* (Deferred-Merge Embedding) algorithm which is in principle identical to that of Chao et al. By combining the DME with a length-balancing clock tree topology generated from a previous work[11], the composite algorithm resulted in an average 12% wire length reduction from that of Tsay[17].

Notice that the latter two algorithms exploit the specific

properties of Manhattan space. Because multiple routing layers is not uncommon in current VLSI technology, and the state-of-the-art MCM fabrication is capable of coping with over fifty routing layers[8], we should consider routing of wires in octolinear and Euclidean spaces as well[7]. With these considerations in mind, we propose a *general* clock tree construction algorithm for the current diversified CAD environment. We also adopt the Elmore delay model as the basis of our clock skew calculations. Our algorithm is general in that it is readily applicable to various routing spaces, from Manhattan to Euclidean. We have achieved average wire length savings of 14.31% and 23.95% in Manhattan and Euclidean spaces compared to the previous best results[3].

PROBLEM FORMULATION

In CAD physical designs, the placement phase determines locations of synchronizing elements of a given circuit. We call these positions the *sinks* of a clock net, and denote the sink set by $C_{net} = \{s_1, s_2, ..., s_n\}$, where $C_{net} \subset \mathcal{R}^2$. A *clock tree* is a rooted binary tree $T(C_{net})$ over the clock net C_{net} with the clock source s_0 being the root and C_{net} being the leaves of $T(C_{net})$. Let the edges in the clock tree be directed away from the source; then an edge e_{uv} connects parent u and child v. The distance between u and v, $\delta(u,v)$, is a function determined by the current routing space. For example, in Manhattan space $\delta(u,v) = |x_u - x_v| + |y_u - y_v|$, and in Euclidean space $\delta(u,v) = ((x_u - x_v)^2 + (y_u - y_v)^2)^{1/2}$. The wire length of e_{uv}, denoted by $\ell(u,v)$, is greater than or equal to $\delta(u,v)$. The length can be greater than the geometric distance because sometimes we have to elongate the wire to maintain the zero-skew property. We define the *cost* of a $T(C_{net})$ as the total length of all edges in $T(C_{net})$.

Let $t_d(s_0, s_i)$ denote the signal propagation time of the unique path from source s_0 to sink s_i. The *skew* of a clock tree $T(C_{net})$ is determined by equation (2).

$$Max\ (\ |t_d(s_0,s_i) - t_d(s_0,s_j)|\ ),\quad \forall\ i,\ j \in C_{net}. \qquad (2)$$

We define a clock tree $T(C_{net})$ as a *zero-skew clock tree* or *ZS tree* if its skew is zero. In this paper, we follow assumptions made implicitly or explicitly in previous ZS tree algorithms[3,4,17]. First, we assume a constant-width wire; hence only wire length counts. Additionally, we assume the interconnect delay parameters are identical for all metal routing layers, and ignore via capacitances and resistances. Finally, we assume single-staged clock trees. The ZS tree construction problem can now be stated as:

Given a clock net C_{net} and a routing space, construct a zero-skew clock tree $T(C_{net})$ with minimum cost.

1. Delay Models

In the linear model, the delay along a path is proportional to the path length. Although less accurate, it has been adopted by many clock tree construction algorithms[9,11,13]. On the other hand, the Elmore delay model uses a distributed RC tree for improved accuracy. Let α and β denote the resistance and capacitance per unit length of wire, c_{g_i} be the gate capacitance of sink s_i, and c_v be the node capacitance of v. Then the lumped capacitance C_v of the subtree rooted at v can be calculated by the following recursive formula[15,17]:

$$C_v = \begin{cases} c_{g_i} & v \text{ is a sink } s_i \\ c_v + \sum_{w \in children(v)} (\beta \cdot \ell(v,w) + C_w) & \text{otherwise} \end{cases} \qquad (3)$$

The propagation delay of a ZS tree $t_d(s_0, s_i)$ can thus be computed as follows:

$$t_d(s_0,s_i) = \sum_{e_{uv} \in path(s_0,s_i)} \alpha \cdot \ell(u,v)\left(\frac{\beta \cdot \ell(u,v)}{2} + C_v\right) \qquad (4)$$

We will adopt the Elmore delay model for a better delay approximation in this paper.

GENERAL ZS TREE CONSTRUCTION ALGORITHM

Our algorithm contains two phases. In the simulated annealing ZS tree construction phase, we use Tsay's zero-skew merging scheme[17] to construct a ZS tree. A *tapping point* is used to merge two ZS subtrees into a larger ZS tree with an equal propagation delay. In this phase, we search the tapping point only within its corresponding *merging regions*[3,4] in which every point has the minimum total distance to the two roots of the merged subtrees. The search space within the merging regions simplifies the tapping point calculation; hence, it fits better into the simulated annealing engine when searching a good ZS tree topology. In the second phase of our algorithm, we propose a Steiner point placement optimization technique to further refine the results generated by the first phase.

1. ZS Merging Scheme under the Elmore Delay Model

To connect two zero-skew subtrees rooted at nodes a and b while ensuring a ZS tree rooted at v involves determining the right placement for the new root v. Let the subtrees rooted at a and b have capacitances C_1 and C_2, and delays $t_1 = t_d(v,a)$ and $t_2 = t_d(v,b)$ respectively. Let $\ell(v,a) = \gamma_1$ and $\ell(v,a) = \gamma_2$. From equation (4), to maintain a ZS tree, the placement of v must satisfy the following equality:

$$\alpha\gamma_1\left(\frac{\beta\gamma_1}{2} + C_1\right) + t_1 = \alpha\gamma_2\left(\frac{\beta\gamma_2}{2} + C_2\right) + t_2 \qquad (5)$$

Let $\delta(a,b) = m$, $\gamma_1 = x$, and $\gamma_2 = m - x$. Substituting x and $m - x$ into equation (5) and solving for x, we have

$$x = \frac{t_2 - t_1 + \alpha m(C_2 + \frac{\beta m}{2})}{\alpha(C_1 + C_2 + \beta m)} \qquad (6)$$

If $0 \le x \le m$, the placement of v can be found on the interconnect wire of length $\ell(a,b) = \delta(a,b)$, where $\delta(v,a) = \gamma_1 = x$ and $\delta(v,b) = \gamma_2 = m - x$ define the position of v. Otherwise, extra wire must be added to balance the delays of the two subtrees to form a new ZS tree. Let $\ell(a,b) = m' > \delta(a,b)$ be the total wire length of the elongated wire. If $x > m$, which means $t_2 > t_1$, we should superimpose v with b, and set $\gamma_2 = 0$ and $\gamma_1 = m'$. Now equation (5) becomes

$$\alpha \cdot m'\left(\frac{\beta \cdot m'}{2} + C_1\right) + t_1 = t_2, \qquad (7)$$