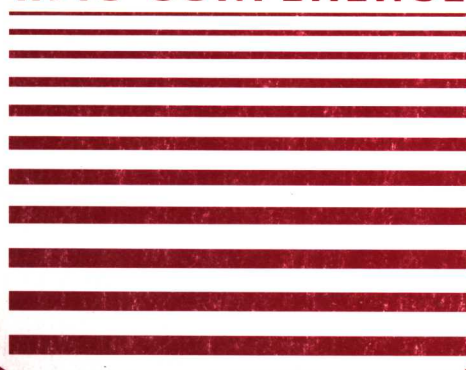


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## ELEVENTH ANNUAL IEEE INTERNATIONAL ASIC CONFERENCE



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# **Welcome to ASIC '98**

## **1998 IEEE International ASIC Conference**

Welcome to the 11th Annual IEEE International ASIC Conference and Exhibit. The program committee is proud to offer an outstanding agenda with 11 technical paper sessions, five workshops, three distinguished speakers, and one Panel Discussion.

The paper sessions offer the latest ASIC designs and the most recent advances in both ASIC technology and design methodology from the best engineers and researchers in the international ASIC community.

The Keynote Speaker is Raul Camposano, Chief Technical Officer, Senior Vice President and General Manager of the Design Tools Group of Synopsys Corporation. The title of his speech is "Design Technology for System on a Chip."

The Tuesday luncheon presentation is "Silicon Intellectual Property: The Passport to System-on-a-Chip." This talk is presented by Vic Kulkarni, Head of Operations for Galax!, a subsidiary of Avant! Corporation. Galax! is in the business of silicon intellectual property and IC design solutions. We continue this conversation on Tuesday evening with our panel discussion, "Intellectual Property Companies – A Key Industry Megatrend for 2002."

The ASIC'98 banquet takes place on Monday night. The banquet speech is titled "NASA Mars Rovers & Orbiters: Imaging the Geologic History of the Red Planes," by James Bell. Dr. Bell is on the faculty of the Cornell University Astronomy Department and Center for Radiophysics and Space Research. He is also a member of several current NASA Teams, including the pathfinder Science Team, Mars Surveyor '98 Orbiter Team, and the Athena Mars 2001 Rover Mission Team.

These talks present the latest work from the cutting edge in three important areas: ASIC technology development (ULSI), the design of the ASIC business (intellectual property companies) and ASIC applications (space exploration).

On Sunday, September 13, five carefully selected workshops provide in-depth coverage in new areas of interest to ASIC designers. They were selected specifically to contribute to the ASIC designer's ability to stay both effective and innovative in the face of changing engineering demands.

We thank our distinguished speakers, the authors of our technical papers, our workshop presenters, and the panelists for contributing their time, their knowledge, and their talent. We thank the ASIC'98 Technical Committee, ASIC'98 Organizing Committee, and the ASIC'98 Steering Committee for the tireless dedication to continually improving the quality of this event. We thank IEEE Travel & Conference Management Services for their partnership and attention to detail. And finally, we thank our attendees, for helping us all make ASIC'98 a valuable contribution to the greater ASIC Community.

Sincerely,

P.R. Mukund, Steering Committee Chair  
Mark Schrader, General Chair  
Ramalingham Sridhar, Technical Program Co-Chair  
Tom Buechner, Technical Program Co-Chair

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# ASIC '98 Technical Committee Group Photo



**Back Row: (Right to Left)**

Duen-Jeng Wang, Kerry Van Iseghem, Dave Braverman, Jim Barby, Robert Frye, Sudhakar Muddu, John Chickanosky, Richard J. Auletta

**Middle Row: (Right to Left)**

David England, Mike Gaboury, Chris Ryan, Gershon Kedem, Howard Chen, Hyun Lee

**Front Row: (Right to Left)**

Thad Gabara, Cherrice Traver, Ramalingam Sridhar, Mark Schrader, Thomas Buechner, Nanjunda Shastry, P.R. Mukund

# Keynote Address



## *“Design Technology for System on a Chip”*

---

Dr. Raul Camposano  
Chief Technical Officer  
Senior Vice President & General Manager  
Design Tools Group  
Synopsys Inc.  
700 East Middlefield Road  
Mountain View, CA 94043

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### **Biography**

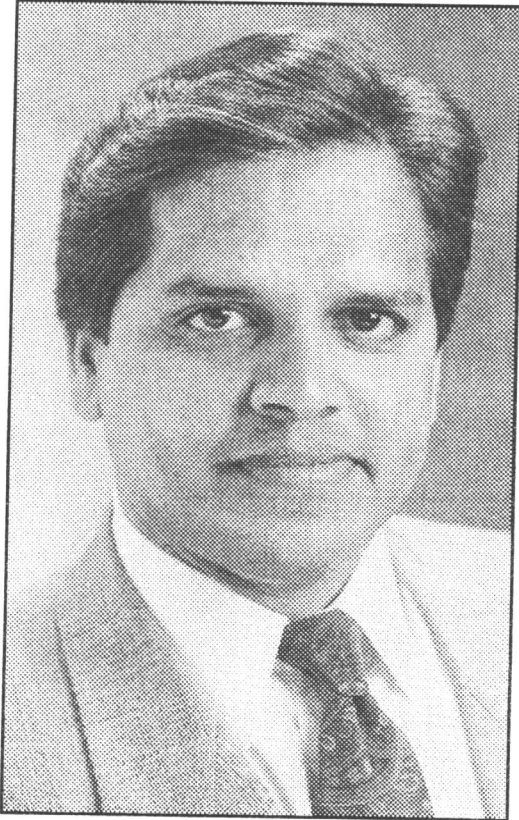
A specialist in behavioral synthesis and embedded system design, Dr. Raul Camposano is Vice President of Engineering for the Design Tools Group of Synopsys. Previously he was General Manager of Design Planning and Director of Design Environment, R&D, at Synopsys since 1993. Prior to joining Synopsys, he concurrently served as the institute director for the German National Research Center for Computer Science (GMD), and professor in the department of computer science at the University of Paderborn, Germany. Between 1986 and 1991, Dr. Camposano led the project on high-level synthesis at the IBM T.J. Watson Research Center. He was also a member of the research staff at the Computer Science Research Laboratory at the University of Karlsruhe.

Dr. Camposano received his B.S.E.E. degree in 1977 and the diploma in electrical engineering in 1978 from the University of Chile, and his Ph.D. in computer science from the University of Karlsruhe in 1981. Active in the EDA professional community, Dr. Camposano serves on various technical program committees and editorial boards worldwide, and has been awarded many accolades and honors for his contributions to the design automation of digital systems.

An active author, Dr. Camposano has written and co-authored three books and a myriad of technical papers on design automation for both academia and industry.



# Luncheon Address



## *“Silicon Intellectual Property: The Passport to System-on-a-Chip”*

---

Vic Kulkarni  
Galax!, Inc.  
46871 Bayside Parkway  
Fremont, CA 94538

---

This luncheon speech will address the challenges of reducing the design gap which exists between manufacturing and design tools capabilities today. The design paradigm has changed from gate delay-driven, top-down methodology to interconnect-driven design methodology. Multiple independent teams are now developing design blocks in different parts of the world and sometimes in separate corporate boundaries to make successful systems in silicon. In this luncheon address, technical, business and legal issues in creating a system-on-a-chip will be examined and Galax!'s experience in setting course for a successful “chipless IC company” will be shared by the speaker.

### **Biography**

Vic Kulkarni has over 21 years of experience in the semiconductor and EDA industry. He has held various engineering and marketing management positions with National, Fairchild, VLSI Technology and Avant! corporation. His background includes CMOS logic and A/D converter design, gate arrays and cell-based IC design, strategic and product marketing of EDA tools ranging from device modeling, circuit simulation, synthesis to physical design tools for deep-submicron technologies. He is currently Head of Operations for Galax!, a subsidiary of Avant! Corporation dedicated to silicon intellectual property and IC design solutions.

# Banquet Address



## *“NASA Mars Rovers and Orbiters: Imaging the Geologic History of the Red Planet”*

---

Dr. James F. Bell, III  
Cornell University Department of Astronomy  
Center for Radiophysics and Space Research  
Ithaca, NY 14853

---

Jim Bell, an astronomer and planetary scientist from Cornell University and a member of the Imaging Team for the NASA Mars Pathfinder mission, will speak on the latest results obtained from the Mars spacecraft rover and orbiter missions, plus future plans to explore Mars using a Cornell-led rover in 2002. Dr. Bell's particular focus is on multispectral imaging and spectroscopy, and he will discuss some of the specific imaging and sensor requirements of these missions, from the science perspective. He and other colleagues on the NASA Mars mission teams are attempting to use spacecraft data to determine the chemical and mineralogical composition of the planet's rocks and soils. These results, plus results from previous studies, are being used to determine whether the climate of Mars in the distant past (when the rocks and soils were first formed) was, as hypothesized by some scientists, much "warmer and wetter" than it is today. Was early Mars a more Earthlike planet? If so, what happened to all of the water? And what are the implications for the possibility of life on Mars?

### **Biography**

Dr. Bell is an Assistant Professor in the Cornell University Astronomy Department. He received his B.S. from Caltech and his Ph.D. from the University of Hawaii, performing research on Mars surface mineralogy and climate variations using infrared and optical telescopes at Mauna Kea Observatory. He spent 3 years as a National Research Council postdoctoral research fellow at NASA's Ames Research Center in California prior to coming to Cornell. In addition to the Pathfinder science team, he is also a member of the imaging teams of the NASA Near Earth Asteroid Rendezvous (NEAR) mission, the Mars Surveyor '98 orbiter investigation, and Cornell's CONTOUR Comet Flyby mission and Athena Mars 2001 Rover mission.

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# **Session MP1**

## **ASIC Applications**

**Session Chair:** Gershon Kedem, Duke University, Durham NC  
**Session Co-chair:** David Braverman, NEC Electronics, Rochester NY

### **Session Summary**

We find ASIC technology in a wide variety of demanding applications where high performance, low power, small weight or low parts count is a driving factor in design.

This session has six papers describing a wide set of diverse applications. We begin with three papers describing ASICs for industrial applications. The first paper describes a precision scale controller that increases position resolution by an order of magnitude over existing methodologies. The second paper describes a 32 bit embedded SPARC microcontroller designed for high performance motor control. The third paper details the utilization of a compact neural net design for precisely controlling electrical motor current.

The forth paper describes FPGA implementation of a Java processor designed to speed up applications written in the popular Java programming language. The FPGA implementation is flexible, allowing the update of the processor design as the Java specification evolves.

The fifth paper describes the memory architecture of a high performance reconfigurable ATM switch supporting advanced features such as backpressure.

The sixth paper describes an ASIC implementation of the IDEA encryption algorithm. The authors describe an implementation that takes advantage of both temporal and spatial parallelism available in the IDEA algorithm. The HiPCrypto ASIC can encrypt/decrypt data at rates of up to 4.4 Gbps.