JSAP CAT. No. AP012316
IEEE CAT. No. 01 CH 37185

JUNE 14–16, 2001/KYOTO

2001 SYMPOSIUM ON VLSI CIRCUITS

DIGEST OF TECHNICAL PAPERS

2001 VLSI CIRCUITS SYMPOSIUM KYOTO

☐ The Japan Society of Applied Physics
☐ The IEEE Solid-State Circuits Society

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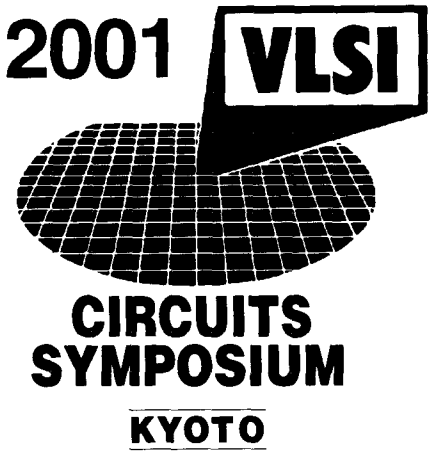

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IEEE

Publication Office

Business Center for Academic Societies Japan
5-16-9 Honkomagome,
Bunkyo-ku, Tokyo 113-8622,
Japan

JSAP CAT. No. AP012316
IEEE CAT No. 01 CH 37185

ISBN 4-89114-014-3 Softbound
ISBN 0-7803-6632-8 Microfiche
ISBN 4-89114-013-5 CD-ROM Edition

Copies of this Digest can be purchased from:
Inside Japan
Business Center for Academic Societies Japan
5-16-9 Honkomagome, Bunkyo-ku, Tokyo 113-8622, Japan
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FOREWORD

Welcome to the 2001 Symposium on VLSI Circuits

The Symposium on VLSI Circuits is sponsored by the Japan Society of Applied Physics and the IEEE Solid-State Circuits Society, in cooperation with the Institute of Electronics, Information and Communication Engineers of Japan and the IEEE Electron Devices Society.

The Symposium will celebrate its fifteenth anniversary, establishing as a major international forum for discussing recent advances in the design of VLSI circuits. This is the first symposium in the twenty first century, and we have expanded the scope to include new concepts in LSI and physical design tools, in addition to microprocessors, signal processors, memories, analog circuits, RF circuits and communication circuits. This year the Symposium has 22 daytime sessions and will present 76 outstanding papers selected from the 153 submitted papers from both industry and universities around the world. In addition, the Symposium will offer a one-day technical short course preceding the Symposium on June 13th. The topic is "Physical Design for Low-Power and High-Performance Microprocessor Circuits".

The Symposium features four invited talks covering its entire scope. The plenary session on June 14th opens with two invited talks. They are, "Digital Vision Chips and High-Speed Vision Systems" and "BSIM Model for Circuit Design Using Advanced Technologies". On June 15th the invited talk, "Development Trend of LTPS TFT LCD for Mobile Applications", is followed by another invited talk describing a unique video system application of MEMs.

VLSI Circuit Symposium evening rump sessions are well known for their selection of timely topics and lively discussions. This year there are four rump sessions. The first rump session, "Which Features of an IC Technology will Benefit Radio SOC?" is a joint rump session with the VLSI Technology Symposium scheduled on June 13th. The remaining three sessions are, "Will Start-Ups Outperform Big Companies?", "Power Supply for Future System LSIs" and "Diverse DRAM Architectures: Why and Who Wins?".

The excellent technical program represents the outstanding efforts of the Technical Program Committees under the leadership of the Program Chair, Masakazu Yamashina, and Co-Chair, Shekhar Borkar. The Committee members, all world-leaders in the field of VLSI design, have solicited strong and interesting papers, selected, and organized them into attractive technical sessions. We express our sincere thanks to all the members for their highly-skilled efforts. We do hope that you not only enjoy the presentation of the papers but join the lively discussions in and outside the sessions.

Next year, the Symposium will return to the Hilton Hawaiian Village in Honolulu, Hawaii, together with the Technology Symposium. We do hope you will attend again.

June 2001

Takayasu Sakurai	David Scott
Symposium Chair	Symposium Co-Chair

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CONTENTS

Thursday, June 14

Session 1: Welcome and Plenary Session I [Suzaku]

Chairpersons: M. Yamashina, *NEC*
S. Borkar, *Intel*

Session 2: RF Front End I [Suzaku]

Chairpersons: T. Mori, *Fujitsu Labs.*
G. Nasserbakht, *Proxim*

Session 3: High Speed Circuits [Suzaku I]

Chairpersons: M. Motomura, *NEC*
J. Goodman, *Chrysalis-ITS*

Session 4: High Performance DRAM [Suzaku II]

Chairpersons: C. Kim, *Samsung Electronics*
H. Pon, *Intel*

Session 5: PLLs and Frequency Synthesizers [Suzaku III]

Chairpersons: T. Kamei, *Oki Electric*
G. Nasserbakht, *Proxim*

Session 6: Design Optimizations and New Technologies [Suzaku I]

Chairpersons: H. Kabuo, *Matsushita Electric*
S. Borkar, *Intel*

Session 7: Memory Redundancy [Suzaku II]

Chairpersons: M. Hiraki, *Hitachi*
D. Scott, *Texas Instruments*

Session 8: Variable Gain Amplifiers [Suzaku III]

Chairpersons: A. Wada, *Sanyo Electric*
K. Azadet, *Agere Systems*

20:00 Rump Sessions:

Organizers: M. Hiraki, *Hitachi*
B. Gieseke, *AMD*

Friday, June 15

Session 9: Plenary Session II [Shunju]

Chairpersons: M. Yamashina, *NEC*
S. Borkar, *Intel*

Session 10: Multimedia and Networking [Shunju]

Chairpersons: M. Matsui, *Toshiba*
C.-T. Chuang, *IBM T.J. Watson Research Ctr.*

Session 11: RF VCOs [Shunju I]

Chairpersons: D.-K. Jeong, *Seoul National Univ.*
G. Taylor, *Intel*

Session 12: Nonvolatile Memories [Shunju II]

Chairpersons: K. Kotani, *Tohoku Univ.*
J. Bowles, *AMD*

Session 13: Voltage and Current Generation [Shunju III]

Chairpersons: Y. Ohtomo, *NTT Electronics*
S. Kosonocky, *IBM, T.J. Watson Research Center*

Session 14: Data Transmission [Shunju I]

Chairpersons: Y. Ohtomo, *NTT Electronics*
A. Abidi, *Univ. of California*

Session 15: Emerging Technology [Shunju II]

Session 16: Sensor and Filters [Shunju III]

Saturday, June 16

Session 17: Clock Distributions and Bus Drivers [Shunju I]

Chairpersons: K. Kobayashi, *Kyoto Univ.*
G. Taylor, *Intel*

Session 18: Passive Elements and Test [Shunju II]

Chairpersons: M. Motomura, *NEC*
K. Azadet, *Agere Systems*

Session 19: ADC and Track/Hold [Shunju III]

Chairpersons: T. Mori, *Fujitsu Labs.*
C.-T. Chuang, *IBM T.J. Watson Research Center*

Session 20: Low Power Design [Shunju I]

Chairpersons: K. Seno, *Sony*
S. Borkar, *Intel*

Session 21: Embedded RAMs [Shunju II]

Chairpersons: N.C.C. Lu, *Etron Technology*
J. Bowles, *AMD*

Session 22: RF Front End II [Shunju III]

Chairpersons: T. Miki, *Mitsubishi Electric*
J. Goodman, *Chrysalis-ITS*

2001 VLSI Circuits Short Course

"Physical Design for Low-Power and High-Performance Microprocessor Circuits"

Wednesday, June 13 (Suzaku)

Organizers: M. Matsui, *Toshiba*
G. Taylor, *Intel*

9:30	Opening	
9:40	Overview of Physical Design	
10:00	Interconnect Design of Athlon™ Microprocessors	J. Moench, *AMD*
11:00	Substrate-Bias Techniques for SH4	K. Ishibashi, *Hitachi*
12:00	Lunch	
13:15	High-Performance SOI Digital Design: from Devices to Circuits	C.-T. K Chuang, *IBM*
14:15	Low-Power and High-Performance Circuit Design of General Purpose DSPs	H. Takahashi, *TI-Japan*
15:15	Break	
15:30	Embedded DRAM SOCs and its Application for MPEG4 Codec LSIs	S. Miyano, *Toshiba*
16:30	Circuit Design of XScale™ Microprocessors	L. T. Clark, *Intel*
17:30	Conclusion	

Digital Vision Chips and High-Speed Vision Systems

Masatoshi Ishikawa and Takashi Komuro

Department of Information Physics and Computing,
Graduate School of Information Science and Engineering, The University of Tokyo
7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan

Abstract

Conventional image processing has a critical limit of frame rate derived from serial transmission of the video signal. In order to overcome the limit, fully parallel processing architecture without scanning has been proposed. In this paper, vision chips with digital circuits and high speed application systems developed in our laboratory will be described.

Vision Chip

In the real world, sensory information is parallel. Especially visual information is high dimensional (3D or 4D) parallel information and is captured and processed parallelly in human retina. However, in the engineering world, a vision system uses serial transmission of video signal from an image sensor such as CCD to a processor. In such a system, transmission speed is limited on the video signal such as NTSC (33ms).

On the other hand, a device called vision chip has been proposed, in which photo detectors (PDs) and processing elements (PEs) are connected in each pixel. It captures and processes images parallelly without serial transmission. Therefore, not only it realizes high speed processing but the benefits of being a system VLSI are expected.

Design Concept

Most of existing research of vision chip use analog circuits in processing element[1-4]. Analog circuits cost lower area and therefore are easier to integrate than digital ones. However, they have demerits that the functions are almost fixed once designed. As a result, many special purpose chips have been developed but there have been few chips for general purpose. To make general purpose vision chip which can process various algorithms on one chip, it is necessary to develop a programmable processing element designed in digital circuits. We call such vision chip as digital vision chip.

On the basis of such concept, Ishikawa et al. proposed an architecture of a digital vision chip[5]. Using a scaled-up model of the vision chip, various application systems have been developed. These systems have realized high speed visual feedback at a sampling period of 1ms.

Research on digital vision chips has been done at a few other laboratories worldwide. In France, a compact digital vision chip called the programmable artificial retina has been proposed, and the researchers have successfully developed chips of 65x76 pixel[6] and 128x128 pixel. In Sweden a unique digital vision chip based on their near-sensor image processing concept was proposed and a 32x32 pixel chip has been developed[7].

One of the problems inherent in designing a digital vision chip is the difficulty of integrating many pixels on a single chip since the digital approach requires more circuits than analog. Therefore, the vision chips mentioned above have taken approach to place a priority on either compactness or performance of the PE, not both.

However, in the background of rapid progress of semiconductor integration technology in recent years, general purpose digital vision chip has become a realizable technology.

Of course, to integrate a large number of pixels in one chip, we have to make an effort to design a compact PE, that is, a design of PE whose area is as small as possible is needed.

Architecture

Following the design concept above, Komuro et al. designed a new architecture S^{3}PE (Simple and Smart Sensory Processing Element) [8] which aimed at further high integration. Fig. 1. shows the architecture of S^{3}PE.

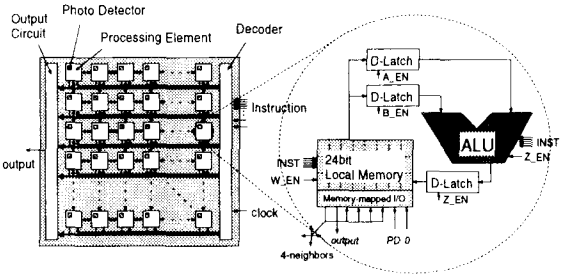

Fig. 1 Architecture of Genaral Purpose Vision Chip

Each PE has an ALU which has bit-serial operation structure and 24 bit local memory in which each bit can be randomly accessed. It communicates with the photo detector and the neighbor PEs via 8 channel I/O which is mapped to memory address space.

The ALU has a simple structure consisting of a full-adder, a carry register and some multiplexers. It can process one of 10 kinds of logical and 8 kinds of arithmetic operations at each cycle. Bit-serial operation is a method that performs each bit of multi-bit operations in order. It is slower than bit-parallel operation but has merits of compact circuits and capability of variable bit length data operation.

In the local memory, 24 bit random access memory (RAM) and 8 bit I/O ports are allocated to the same address space. I/O ports are connected to up, down, left and right PEs, input from the sensor, and zero signal. Introducing the memory mapped I/O, all processing including not only operations but also I/O operation is performed by accessing the local memory.

As a result, the instruction code has a simple form : all

instructions consist of read address A, B (5 bits each), operation code (5 bits), and write address (5 bits). This 20 bit instruction is divided into four steps, and is transmitted and processed in order.

The A/D conversion of the analog signal from the photo detector is performed by measuring the time that the voltage of the capacitor discharged by the photo current crosses the threshold voltage. Using the PE as a counter, A/D conversion is realized without increasing circuit area.

These design policies give priority to the integrity over other performance such as processing speed. They depend on the idea that the power of massive parallelism is enourmous and even if the performance of each PE is a little low, the total performance is still high.

Early Vision Algorithms

We implemented some early vision algorithms for evaluating the performance of this vision chip. Table1 shows the steps and processing time. This table shows that the vision chip can process most of early vision programs at the order of μs, which is much higher than conventional image processing systems.

Table1 Steps and processing time of early vision algorithms

Algorirhm	steps	time
Edge Detection (binary)	8	0.64μs
Smoothing (binary)	14	1.1μs
Edge Detection (6bit)	47	3.8μs
Smoothing (6bit)	41	3.3μs
Thinning (binary) *	12	0.96μs
Convolution (6bit)	986	80μs
Poisson Equation (6bit) *	65	5.2μs

* repeating operation

VLSI implementation and System Development

Based on the architecture, we have designed a schematic and a custom layout using 0.35μm CMOS process[9]. The number of transistor per PE is about 400 and the PE area is as small as 105μm x 105μm. Using this design, we have developed a prototype chip of 64x64 pixels. Fig. 2 shows the chip photo.

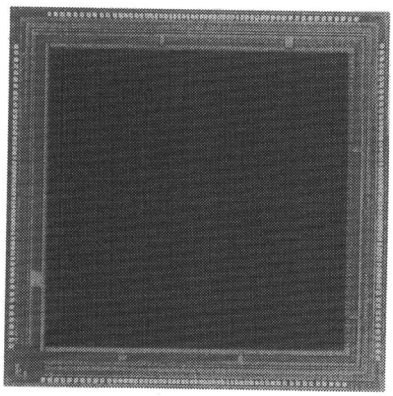

Fig.2 Chip Photo of General Purpose Vision Chip

To make a whole system using the vision chip, we have developed a controller which transmit instructions to the vision chip at the order of 100ns and also manage program control such as conditional jump and loop. The vision chip, controller, and memory are the components of the system.

We have also been developing a C-like programming language of the system (SPE-C) and its compiler. On the development environment, users can simulate and check their programs in a PC or a workstation.

Global Feature Extraction Circuit for Digital Vision Chip

One of the important issues of the vision chip we have to consider is how to output. In principle, the parallel processing in the PE array is transformation from 2D pattern to 2D pattern. However, if we try to output the whole 2D pattern via pins, we face again the I/O bottleneck problem which we solved for the input.

In a real application which requires high speed control, the final output needed is not a pattern but some feature extracted from the pattern in most cases. For example, visual feedback control of the robot gets the position of the target from the sensor and gives feedback to the actuator. In this case, pattern information is only an intermediate expression and the output of the vision chip can be scalar information.

For such purpose, we designed a global feature extraction circuit which calculates moment at high speed. Moment is a value which is widely used in a real application. This circuit has some features : i) it consists of digital circuits, ii) circuit scale is small, iii) it can calcurate moments at high speed iv) it is easy to implement to VLSI. Fig. 3 shows the configuration.

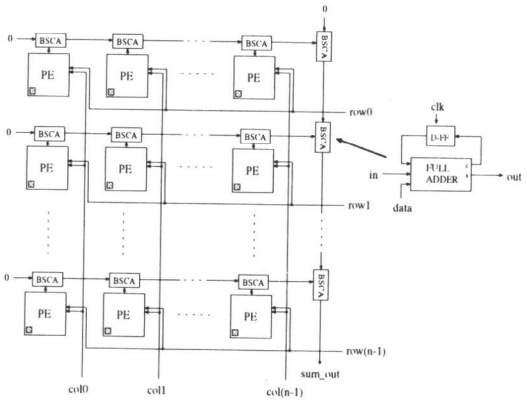

Fig. 3 Moment Extraction Circuit

High Speed Target Tracking Vision Chip

The digital vision chip based on S^3PE is designed putting emphasis on generality to answer to various uses. Therefore, the circuit scale becomes large to some extent though we have made an effort to design a compact circuit. However, there are some applications which require higher resolution. Especially in case to monitor a large range of view or track more than one objects, high resolution sensor is desired.

Then, we propose a new vision chip which aims to improve the resolution and speed by focusing the purpose of the chip to a specific task [10]. In this design we have chosen target tracking as the task with which we have