Proceedings

1995
IEEE Multi-Chip Module Conference
MCMC '95

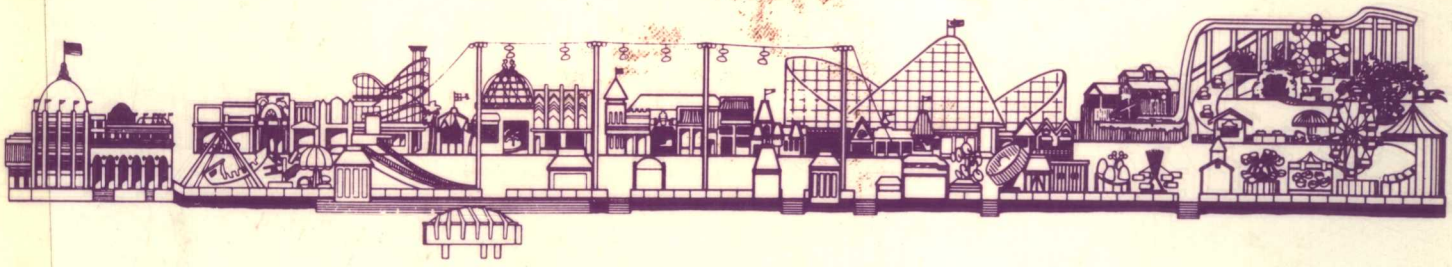
January 31 – February 2, 1995
Santa Cruz, California

Sponsored by

IEEE Circuits and Systems Society

IEEE Components, Packaging, and Manufacturing Technology Society

IEEE Electron Devices Society



IEEE Computer Society Press

The Institute of Electrical and Electronics Engineers, Inc.

Proceedings

1995
IEEE
Multi-Chip Module Conference

January 31 - February 2, 1995

Santa Cruz, California

Sponsored by

IEEE Circuits and Systems Society

IEEE Components, Packaging, and Manufacturing Technology Society

IEEE Electron Devices Society

In cooperation with

IEEE Computer Society

IEEE Computer Society Press
Los Alamitos, California

Washington • Brussels • Tokyo

IEEE Computer Society Press
10662 Los Vaqueros Circle
P.O. Box 3014
Los Alamitos, CA 90720-1264

IEEE Computer Society Press Order Number PR6970
Library of Congress Number 94-72782
IEEE Catalog Number 95CH35726
ISBN 0-8186-6970-5 (paper)
ISBN 0-8186-6971-3 (microfiche)
ISBN 0-8186-6972-1 (case)

Additional copies may be ordered from:

IEEE Computer Society Press
Customer Service Center
10662 Los Vaqueros Circle
P.O. Box 3014
Los Alamitos, CA 90720-1264
Tel: +1-714-821-8380
Fax: +1-714-821-4641
Email: cs.books@computer.org

IEEE Service Center
445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
Tel: +1-908-981-1393
Fax: +1-908-981-9667

IEEE Computer Society
13, Avenue de l'Aquilon
B-1200 Brussels
BELGIUM
Tel: +32-2-770-2198
Fax: +32-2-770-8505

IEEE Computer Society
Ooshima Building
2-19-1 Minami-Aoyama
Minato-ku, Tokyo 107
JAPAN
Tel: +81-3-3408-3118
Fax: +81-3-3408-3553

Editorial production by Regina Spencer Sipple
Cover design by Joseph Daigle/Schenk-Daigle Studios
Printed in the United States of America by Braun-Brumfield, Inc.

The Institute of Electrical and Electronics Engineers, Inc.

Foreword

The 1995 IEEE Multi-Chip Module Conference (MCMC) held in Santa Cruz, California this year, is an annual meeting sponsored by the IEEE Circuits and Systems Society; the IEEE Components, Packaging and Manufacturing Technology Society; the IEEE Computer Society; and the IEEE Electron Devices Society. The goal of this prestigious gathering is to bring together elements of packaging technology and design, circuits and systems design, computer-aided design, modeling, analysis, and education. This conference is unique and well-known for its multi-disciplinary coverage of all these aspects of MCMs.

This year's focus reflects a strong resurgence in activity on modeling and analysis; traditionally, these areas have been a significant focal point for MCMC. As new, higher performance electronic systems push the limits of packaging technology, there is an increasing need in the industry for accurate and powerful modeling and simulation tools. The papers presented at MCMC'95, and included in these proceedings, clearly demonstrate the current dynamic international activity in this field. MCMC'95 offers sessions covering new applications of MCMs and some exciting recent work on programmable modules.

Due to the significant number of submissions this year and our desire to maintain the single-track format, we have instituted a poster session. The papers selected for this session are of a more specialized nature and, therefore, have a more selective appeal. In addition, members of the program committee felt that this forum would permit closer interaction among the presenters and their audience.

The program this year is oriented toward promoting interaction among professionals in the MCM and related areas as well as providing a forum for presenting and discussing the latest developments, immediate needs, and future MCM trends. The conference consists of two days of technical sessions, invited talks, and a poster session that all run as a single track so that everyone may attend the entire program. January 31st will be a full day of tutorials providing in-depth coverage of high-interest topics. Plus, there will be exhibits and demonstrations of state-of-the-art MCM prototypes and products from leading industrial organizations as well as MCM CAD tools from universities and CAD vendors.

Welcome to MCMC'95!

Robert Frye
General Chair

David B. Tuckerman
Technical Program Chair

MCMC'95 Steering Committee

General Chair
Robert C. Frye, *AT&T Bell Laboratories*

Technical Program Chair
David B. Tuckerman, *nCHIP, Inc.*

Tutorials Chair
Paul Franzon, *North Carolina State University*

Exhibits Chair
Wayne Wei-Ming Dai, *University of California, Santa Cruz*

Finance & Local Arrangements Chair
Rui Wang, *Intel Corporation*

Past Chair
David P. LaPotin, *IBM T.J. Watson Research Center*

Asia Liaison
Yuji Okuto, *NEC Corporation*

Europe Liaison
Bernard Courtois, *TIMA — CNRS-INPG-UJF*

S.M. Kang, *Coordinated Sciences Laboratory, University of Illinois*
James Murphy, *Advanced Research Projects Agency*
David W. Palmer, *Sandia National Laboratories*
King L. Tai, *AT&T Bell Laboratories*
Jan Vardaman, *TechSearch International*
Simon Wong, *Center for Integrated Systems, Stanford University*

Technical Program Committee

Technical Program Chair

David B. Tuckerman, *nCHIP, Inc.*

Technical Program Committee

Anthony F. Bernhardt, *Lawrence Livermore National Laboratories*
Eric Bogatin, *Sun Microsystems*
Don Bouldin, *University of Tennessee*
Reed Bowlby, *Motorola Semiconductor*
Philip Chan, *Hong Kong University of Science & Technology*
Jason Cong, *University of California, Los Angeles*
Wayne Wei-Ming Dai, *University of California, Santa Cruz*
Jiayuan Fang, *State University of New York*
Thaddeus J. Gabara, *AT&T Bell Laboratories*
Larry Gilg, *MCC*
Richard J. Higgins, *Georgia Institute of Technology*
Chung W. Ho, *MicroModule Systems*
S.M. Kang, *University of Illinois*
Atsuo Kimura, *IBM Japan, Ltd.*
Paul A. Kohl, *Georgia Institute of Technology*
Teruo Kusaka, *NEC Corporation*
David P. LaPotin, *IBM T.J. Watson Research Center*
Stephen Leanheart, *GTE Government Systems*
Y.C. Lee, *University of Colorado*
Albert W. Lin, *ERSO/ITRI*
Lucius L. Lockwood, *Motorola*
P.R. Mukund, *Rochester Institute of Technology*
Rob Naylor, *Bath Scientific, Ltd.*
Robert Parker, *ARPA/CSTO*
R. Fabian Pease, *Stanford University*
Larry Pillage, *University of Texas at Austin*
John L. Prince, *University of Arizona*
Eugene J. Rymaszewski, *Rensselaer Polytechnic Institute*
Peter Sandborn, *MCC*
Masao Sato, *Waseda University*
Leonard W. Schaper, *University of Arkansas*
Bill Schmidt, *Silicon Graphics, Inc.*
Ashok Seth, *Intel Corporation*
Toshio Sudo, *Toshiba Corporation*
King L. Tai, *AT&T Bell Laboratories*
Yee-Ming Ting, *IBM Microelectronics*
Paul Van Loan, *Hewlett-Packard Company*
Rui Wang, *Intel Corporation*

Table of Contents

Keynote Address:
What Determines the Direction of Packaging Technology?

Akira Masaki
Hitachi Device Development Center
Japan

What Determines the Direction of Packaging Technology?

Akira Masaki

Device Development Center, Hitachi, Ltd.

Abstract

Trend in integration scale of semiconductor IC's strongly influences the direction of packaging technology. Integration level of CMOS VLSI's will continue increasing. In this paper, problems of high-speed technologies are discussed, and it is shown that the direction of integration technologies for computer logic is subject to the fundamental principles of wiring and signal transmission.

1. Introduction

There are many issues related to packaging technology. Even within the scope of computer packaging, we have worried about:

(1) MCM or not ("monolithic circuits vs. hybrid circuits" and "Large-Scale Integration vs. Moderate-Scale Integration" are similar issues),

(2) MCM-C, -D, or -L,

(3) Air-cooling vs. water-cooling,

(4) Area-bonding vs. peripheral bonding,

(5) Controlled Impedance Terminated net signal transmission vs. Resistance-Capacitance net signal transmission, and so on.

It is very difficult to obtain clear perspectives of these issues, because very many factors have to be considered, and solutions are not necessarily unique.

The direction of packaging technology is inseparably related to semiconductor integrated circuit technology. In particular, the trend of integration scale of IC's strongly influences the direction.

Since the introduction of integrated circuits into computer logic in the early 1960's, silicon bipolar technology, particularly emitter-coupled logic (ECL) has been the dominant technology used in most large-scale computers and supercomputers. This technology has been used along with sophisticated high-density packaging technologies indispensable for coping with its large power dissipation and relatively low level of integration. Development of high-heat-density cooling, large-pin-count packaging, and low-dielectric-constant substrates have been pursued.

Now, room-temperature CMOS is becoming the successor to ECL. The first priority is given to "low cost". Packaging technologies that meet the requirement must be developed.

In this paper, the fundamental causes of the transition mentioned above will be discussed, and it will be made clear that the direction of semiconductor IC technology itself is strongly influenced by "wiring and signal transmission", the most common issue of packaging technology.

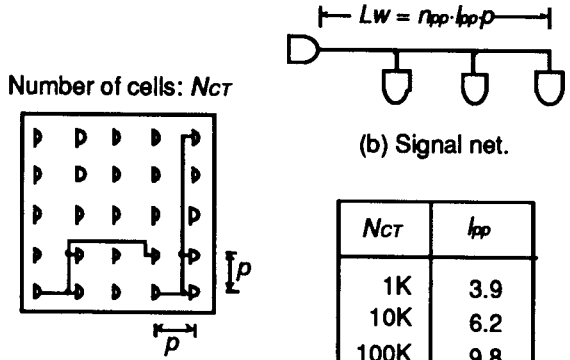
2. Problems of high-speed technology

Why ECL has been used so long, in spite of the hopes on GaAs and Josephson-junction devices widely held as early as in 1970's? One of the most fundamental reasons is that ECL can drive Controlled Impedance Terminated (CIT) nets easily.

Wire length significantly affects the performance of circuits in a system. The signal nets on printed circuit boards are more than ten centimeters long, wire resistance is as small as several ohms per meter, and CIT nets are usually used. The signal nets on LSI chips, on the other hand, are several millimeters long, wire resistance is as large as several tens of ohms per millimeter, and unterminated Resistance-Capacitance nets (RC nets) are used. For module substrates, both CIT and RC nets are used. In any case, to evaluate performance in system environments, we must estimate wire length of logic signal nets.

The LSI chips in many modern computers are mounted on modules, which are then mounted on a large printed circuit board. Each of the LSI chips, modules, and printed circuit boards can be regarded as a two-dimensional (2-D) logic cell array. Figure 1 illustrates a 2-D square array: the semicircular marks represent cells, and each cell corresponds to an LSI chip if the array is a module or to a circuit or a circuit block if the array is an LSI chip. It is assumed that there are N_{CT} cells in the array and that the average center-to-center spacing of the cells in the x and y direction is p.

0-8186-6970-5/94 $04.00 © 1994 IEEE



N_{CT}	l_{pp}
1K	3.9
10K	6.2
100K	9.8
1M	15.0

(c) Wire length of 2-D cell array. (Rent's Rule coefficient r=2/3)

Fig. 1. Wire length significantly affects the performance of circuits in a system. The wire length l_{pp} can be estimated by the equations reported in [1], [2].

The average wire length per signal net L_w is written as $n_{pp} \cdot l_{pp} \cdot p$, where n_{pp} is the average number of loads and l_{pp} is the average pin-to-pin connection length in units of p.

The wire length l_{pp} can be estimated by the equations reported in [1], [2]. Rent's Rule [3] is the basis of these equations.

When the integration level of IC's was very low, the length of the wiring between circuits could be as much as several to several tens of centimeters. The CIT scheme is very effective for high-speed signal transmission in long wires because signals reach the far end of the net with a delay time equal to the electrical length of the wire. The transmission speed is equal to the speed of light in a vacuum divided by the square root of the dielectric constant of the insulator material used in the wires. There is no way to get a smaller delay over a certain distance. Thus even in the age of discrete components, a circuit delay in system of a few nanoseconds could be obtained by using ECL.

The drawback of ECL is its large power dissipation. The driving capability of ECL circuits is mainly determined by the current flowing through the emitter-follower pull-down resistor when the output signal changes from high to low. It is therefore primarily determined by the power dissipation of the circuit. If ECL chips with higher integration level are used without sufficient cooling technology, the driving capability of ECL circuits has to be decreased, and lower system performance is obtained.

This is the reason the level of integration has been regarded as non-essential for mainframe logic IC's. Also, the belief that integration is non-essential has been a basis for the expectation that a novel high-speed device technology such as GaAs or Josephson junction devices will become dominant in the near future.

Contrary to the general belief, careful observation of development history showed that the integration scale of logic IC's used for high-end mainframe computers had steadily increased by ten times every five years, as shown in Figure 2 [4]-[6].

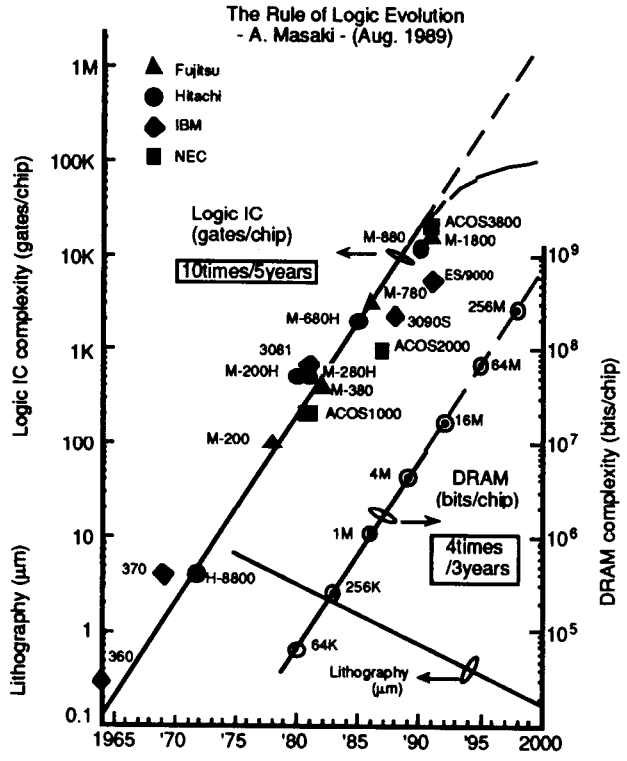


Fig. 2. Integration scale of logic IC's used for high-end mainframe computers has steadily increased by ten times every five years. The prediction that room-temperature CMOS will become the long-pursued post-ECL high-speed device originated in the discovery of this "rule" [4]-[6].

This rate of increase is the same as that for DRAMs, which is usually stated as four times every three years. This clearly tells us that increases in integration scale have been the source of decreasing cost-performance ratio in

computers. If this trend continues, the gate count per chip will reach two million in the year 2000. Novel high-speed devices will not be able to cope with this complexity in a practical way, and it will not be easy for conventional ECL either. Even if individual gate-circuit power is as little as 2 mW, the chip will consume the unmanageably large power of 4 kW.

The driving capability of ECL circuits is primarily determined by the power dissipation of the circuit and cannot benefit from device miniaturization. Because the power of ECL circuits cannot be increased, the driving capability of ECL circuits will be overtaken by that of CMOS in the future.

ECL has been the dominant high-speed technology because it can drive Controlled Impedance Terminated (CIT) nets easily. Using the CIT scheme on an ECL chip is, however, quite unrealistic. Since the characteristic impedance of the wire is about 20 Ω, the power per circuit is as large as about 10 mW, even if the signal voltage and the power supply voltage is as small as 0.5 volt.

Even if the power management is made possible, it should be noted that there is a physical limit to miniaturization for this scheme [6], [7].

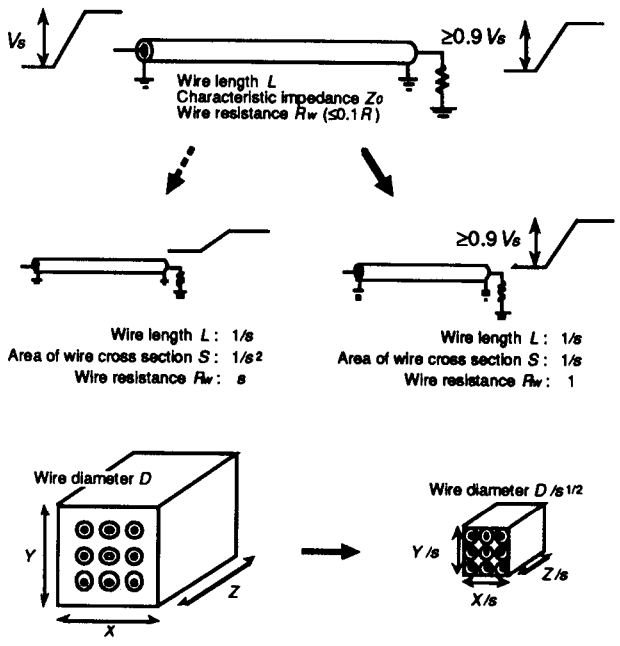


Fig. 3. There is a physical limit to miniaturization for CIT (Controlled Impedance Terminated) net, the highest speed signal transmission scheme [6], [7].

If the total packaging system is scaled down three-dimensionally by a factor of s, the wire resistance increases by the same factor. This is not acceptable for a signal transmission in the CIT net because the ratio of the wire resistance and the resistance of the termination resistor at the receiving end of the net should be no more than about 0.1, in order to keep signal voltage integrity. The wire diameter therefore should be scaled down by a factor of the square root of s. Thus, as shown in Fig. 3, the total packaging space is eventually completely occupied by the wires and we cannot further reduce the physical size of the system.

The only way to cope with this problem is to use super conductors. If Josephson junction devices are used together, the problem of the power dissipation is solved at the same time, because Josephson junction devices require voltages of only a few millivolts.

3. What is coming?

A prediction was made that room-temperature CMOS, which has rarely been considered suitable for very high-speed computer logic, will have sufficient performance to be the long-pursued post-ECL high-speed device when deep-submicron technology is available [4]-[6]. The prediction is becoming a firm reality.

If equivalent system performance can be obtained by CMOS compared with other high-speed technologies, CMOS will win industrial favor, because (1) the basis of the most advanced and solid technology established through development of DRAM is directly applicable, (2) technological compatibility with personal computers, workstations and small-computers benefits R&D of CMOS mainframes in all aspects, (3) the unique feature of CMOS scaling down allows inheritance of circuit design over generations, (4) its low power dissipation cannot be matched by other technologies since a CMOS circuit consumes energy only during switching, occurring once every several machine cycles on average, as discussed below, (5) consequently, the highest integration level is achieved by CMOS.

Now we must discuss to what extent the circuit speed and the integration level of CMOS VLSI'S will increase in the future.

Although there is no physical limit to miniaturization for Resistance-Capacitance (RC) net, the RC delay remains constant when the system is scaled down. Therefore, improvement of the circuit speed in system environments will eventually reach a limit in the future, as long as the average pin-to-pin connection length l_{pp} is not decreased.

Therefore, parallelism has to be pursued for improving system performance, and increase of integration level becomes important all the more.

Among the various factors that impede the increase of the integration level, power consumption and yield of large chips are most crucial.

The most notable characteristic of CMOS is that it consumes energy only during switching. The switching energy E is obtained by integrating the product of current flowing through the driving transistor and the voltage difference between the drain and source of the transistor. The current and the voltage are functions of time. An approximate value of E is given by $(1/2)CV^2$ where C is the total capacitance of the circuit and loads and where V is the power supply voltage. The power dissipation P of the CMOS circuit is given by $(2T)^{-1}CV^2$ where T is the average switching period of the circuits in the system. Since P increases with switching frequency, it has been argued that CMOS will lose its advantage of low power consumption if it is used for very high-speed computer logic in the future.

The problem can be analyzed more comprehensively by introducing a quantity k that is defined by the average switching period T divided by the circuit delay in system t_{sd} [8]-[10]. Then, the power dissipation P of the CMOS circuit is given by $(2k \cdot t_{sd})^{-1}CV^2$. The value k is independent of the hardware technology, and depends solely upon the logical structure of the system—as long as the performance of the circuit is fully utilized. The value k is within the range of several tens to 200 for most computer systems [8], [9].

Since t_{sd} cannot be increased, we must decrease C and V, and increase k, in order to decrease the power dissipation.

There is, however, a certain physical limit to decreasing C, because dielectric constant cannot be smaller than unity. Also, it is not expected that V can be much smaller than 1V. Although decrease of C and V will continue for sometime, it will become more and more difficult in the future.

Usually, k becomes smaller, i.e., switching occurs more frequently, if sophisticated logic is used for improving system performance [8], [9].

Operating each logic block only when it is required is effective for increasing k without decreasing system performance significantly.

Another possibility of increasing k without decreasing system performance is to introduce asynchronous logic design, because a circuit in an asynchronous system is expected to switch only when it is logically necessary [11].

In pursuing increase of integration level, increasing chip size is effective, but it is difficult to realize a defect-free large chip. Therefore, it becomes necessary to introduce fault-tolerant schemes for realizing a very large chip, or WSI (Wafer Scale Integration). Redundancy schemes have already been widely used for DRAM, but not yet for logic.

One example of successful development of WSI is the artificial neural network WSI experimentally designed and fabricated using digital CMOS technology (Fig. 4) [12].

Out of the 40 million transistors prepared on the five-inch wafer, approximately 19 million transistors were used to implement the 576 neuron network. This WSI could solve 16 city Traveling Salesman Problem in less than 0.1 seconds. The inherent fault tolerance of neural networks was actually demonstrated by this development. Also, this development suggests that realizing fault-tolerant logic is not impossible.

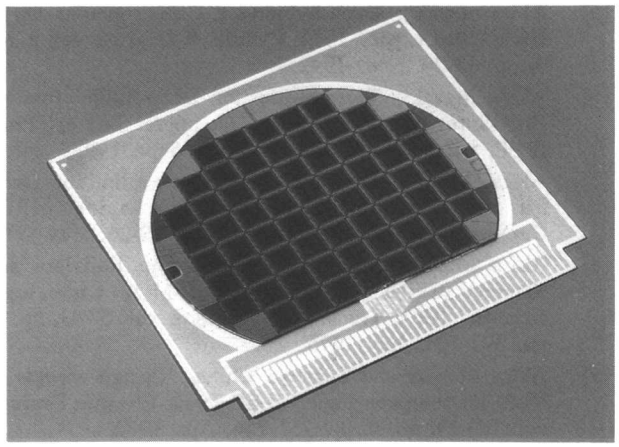


Fig. 4. One example of successful development of WSI: Neuro-WSI fabricated by using 0.8 μm CMOS gate-array wafer [12]. The five-inch wafer contains up to 576 neurons. It is mounted on a ceramic substrate.

For implementing ordinary logic, it is easier to adopt redundancy schemes in PLA's (Programmable Logic Arrays) than random logic. Also, technologies and techniques useful for avoiding and repairing defects will be established through development of FPGA's (Field Programmable Gate Arrays).

The possibilities mentioned above hint to us that integration level of CMOS VLSI's will continue increasing in the late '90s, and into the 21st century. This trend must be carefully watched for considering the direction of packaging technology.

References

[1] Akira Masaki and Minoru Yamada, "Equations for estimating wire length in various types of 2-D and 3-D system packaging structures," IEEE Trans. Components, Hybrids, Manuf. Technol., vol. CHMT-10, no. 2, pp. 190-198, June 1987.

[2] Wilm E. Donath, "Placement and average interconnection length of computer logic," IEEE Trans. Circuits Syst., vol. CAS-26, no. 4, pp. 272-277, Apr. 1979.

[3] Bernard S. Landman and Roy L. Russo, "On a pin versus block relationship for partitions of logic graphs," IEEE Trans. Comput., vol. C-20, no. 12, pp. 1469-1479, Dec. 1971.

[4] Akira Masaki, "Possibilities of CMOS mainframe and its impact on technology R&D," in 1991 Int. Sympo. VLSI Technol. Dig. Tech. Papers, pp. 1-4, May 1991.

[5] Akira Masaki, "Deep-Submicron CMOS Warms Up to High-Speed Logic," IEEE Circuits & Devices, vol. 8, no. 6, pp. 18-24, Nov. 1992.

[6] Akira Masaki, "Possibilities of Deep-Submicrometer CMOS for Very-High-Speed Computer Logic," Proc. IEEE, vol.81, no.9, pp.1311-1324, Sept. 1993.

[7] Akira Masaki, "Electrical resistance as a limiting factor for high performance computer packaging," IEEE Circuits & Devices, vol. 5, no. 3, pp. 22-26, May 1989.

[8] Akira Masaki, Shinji Kadono, Osamu Fujiwara and Tsuneyo Chiba, "Comparison of MOS basic logic circuits," IECE Trans. (in Japanese), vol. 58-D, no. 7, pp. 397-404, July 1975.

[9] Akira Masaki and Tsuneyo Chiba, "Design aspects of VLSI for computer logic," IEEE Trans. Electron Devices, vol. ED-29, no. 4, pp. 751-756, Apr. 1982.

[10] Peter W. Cook, Dale L. Critchlow and Lewis M. Terman, "Comparison of MOSFET logic circuits," IEEE J. Solid-State Circuits, vol. SC-8, no. 5, pp. 348-355, Oct. 1973.

[11] Tam-Anh Chu and Rabindra K. Roy, "Practical Asynchronous Design," IEEE Design & Test of Computers, Summer 1994, pp.6-7.

[12] Akira Masaki, Yuzo Hirai and Minoru Yamada, "Neural Networks in CMOS: a Case Study," IEEE Circuits & Devices, vol.6, no.4, pp. 12-17, July 1990.

Session I:
MCM Manufacturing Issues

Atsuo Kimura
IBM Corporation, Japan