INTERNATIONAL SYMPOSIUM AND EXHIBITION ON

ADVANCED PACKAGING *Materials*

PROCESSES, PROPERTIES AND INTERFACES

Proceedings

CHATEAU ELAN, BRASELTON, GEORGIA
MARCH 6-8, 2000

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International Symposium on Advanced Packaging Materials

Processes, Properties and Interfaces

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1999 Best Paper of Session

Adhesives (Chairs: Tong/Liu)

CONDUCTIVITY MECHANISMS OF ISOTROPIC CONDUCTIVE ADHESIVES (ICAs)

Daoqiang Lu, C.P. Wong, Georgia Institute of Technology; Quinn K. Tong, National Starch and Chemical Company

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MULTI-LAYERED STRUCTURE: ADHESIVE SELECTION AND PROCESS MECHANICS

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Dan M. Scheck, P. Garrou, J. Im, G. Meyers, D. Hawn, Dow Chemical, MCNC; M Vincent, J. Wu, C.P. Wong, Georgia Institute of Technology

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DEVELOPMENT AND APPLICATION BY INK-JET PRINTING OF ADVANCED PACKAGING MATERIALS

Donald J. Hayes, Michael E. Grove, W. Royall Cox, MicroFab Technologies, Inc.

Thermal Management (Chairs: Knudsen/Malshe)

THERMAL ENGINEERING OF ELECTRONICS PACKAGES USING CVD DIAMOND

Philip M. Fabis, Norton Company

Modeling & Simulation (Chairs: Schubert/Chanchani)

ELECTRICAL AND MECHANICAL MODELING OF EMBEDDED CAPACITORS

Yang Rao, C.P. Wong, Jianmin Qu, Georgia Institute of Technology

Integrated Passives (Chairs: Harvey/Lenihan)

INTEGRATION OF NiCr RESISTORS IN A MULTILAYER Cu/BCB WIRING SYSTEM

Michael J. Toepper, K. Scherpinski, F. Krause, K. Halser, R. Hahn, O. Ehrmann, H. Reichl, TUB / Fraunhofer IZM

High Density Substrates & Packaging (Chairs: McKerron/Toepper)

MCM-D/C PACKAGING SOLUTION FOR IBM LATEST S/390 SERVERS

Eric Perfecto, Ronald Shields, Mathias Jeanneret, Ashwani Malhotra, Dale McHerron, IBM Microelectronics

CSP (Chairs: Elenius/Badihi)

SUPER CSP™: WLCSP SOLUTION FOR MEMORY AND SYSTEM LSI

Toshio Hamano, Fujitsu Microelectronics, Inc.; Toshimi Kawahara, Jun-ichi Kasai, Fujitsu Ltd.

Flip Chip Bumping (Chairs: Frear/Williams)

RELIABILITY OF ELECTROLESS NICKEL FOR HIGH TEMPERATURE APPLICATIONS

Sabine Anhock, Andreas Ostmann, Technical University of Berlin; Herbert Reichl, Hermann Oppermann, Rolf Aschenbrenner, Fraunhofer Institute for Reliability & Microintegration IZM

Poster Papers (Chair: Qu)

CONDUCTIVE POLYMER COMPOSITES WITH POSITIVE TEMPERATURE COEFFICIENT
Shijian Luo, C.P. Wong, Georgia Institute of Technology

SMART TOOLING FOR ASSEMBLY OF THIN FLEXIBLE SYSTEMS
Ruijun Chen, Daniel Baldwin, Georgia Institute of Technology

ADHESION STUDIES OF MODEL EPOXY SYSTEMS AND COMMERCIAL UNDERFILL RESINS
R. A. Pearson, P. Komnopad, Lehigh University

MONDAY, MARCH 6

CONTINENTAL BREAKFAST
7 AM - 8 AM

REGISTRATION
7 AM - 5:30 PM

SESSION 1:
ADHESIVES

8AM - 10:05AM
Session Chairs:
Quinn Tong, National Starch and Chemical Company
Johan Liu, IVF

001 Materials and Process Technology: Materials
Richard H. Estes, Polymer Flip Chip Corporation

007 Development of Conductive Adhesives Filled with Low-melting-point Alloy Filters
Daoqiang Lu, C.P. Wong, Georgia Institute of Technology

014 Advancing Materials using Interfacial Process and Reliability Simulations on the Molecular Level
N. E. Iwamoto, Honeywell

018 Novel Conductive Adhesives with Stable Conductivity and High Impact Resistance
Quinn K. Tong, Eric Zhang, National Starch and Chemical Company; Gerald Fredrickson, Roseann Schultz, Emerson and Cuming Specialty Polymers

024 Conductive Adhesives for Solder Replacement in Electronic Packaging
Daoqiang Lu, C.P. Wong, Georgia Institute of Technology

BREAK: 10:05 AM - 10:25 AM

SESSION 2:
INTEGRATED PASSIVES

10:25AM - 11:40AM
Session Chairs:
James Young, Intarsia Corporation
Timothy Lenihan, Sheldahl, Inc.

032 High Dielectric Constant Polymer-ceramic Composite for Embedded Capacitor Application
Yang Rao, S. Ogitani, Paul Kohl, C.P. Wong, Georgia Institute of Technology

038 Materials Options for Dielectrics in Integrated Capacitors
Richard Ulrich, Len Schaper, University of Arkansas, HiDEC

044 Self-consistent Model for Dielectric Constant Prediction of Polymer-ceramic Composite
Yang Rao, Jianmin Qu, C.P. Wong, Georgia Institute of Technology; Tom Marinis, Draper Laboratory

LUNCH: NOON - 1PM

SESSION 3:
UNDERFILL

1:30PM - 3:35PM
Session Chairs:
Daniel Baldwin, Georgia Institute of Technology
Ray Pearson, Lehigh University

050 Reliability Investigations of FCOB Assemblies with Process-Induced Defects
A. Schubert, R. Dudek, J. Kloeser, B. Michel, H. Reichl, Fraunhofer Institute for Reliability and Microintegration IZM; T. Hauck, K. Kaskoun, Motorola - Semiconductor Products Sector, Germany

058 Adhesion Studies of Polymide - Epoxy Interfaces in Flip Chip Assemblies
R. A. Pearson, T. B. Lloyd, Lehigh University

063 Modeling the Mechanical Behavior of Underfill Resins and Predicting their Performance in Flip-Chip Assemblies
R. A. Pearson, Ali Ayhan, Herman Nied, Lehigh University

068 Material Challenges for Wafer Level Packaging
Bodan Ma, Eric Zhang, Sun Hee Hong, Quinn K. Tong, Ann Savoca, National Starch and Chemical Company

074 Adhesion Characterization of No Flow Underfill Baselined with Fast Flow Snap Cure
Jicun Lu, Brian Smith, Daniel F. Baldwin, Georgia Institute of Technology

BREAK: 3:35 PM - 3:55 PM

SESSION 4:
ENCAPSULATION

3:55PM - 5:35PM
Session Chairs:
Ken Gilleo, Alpha Metals/Cookson
S.H. Shi, Georgia Institute of Technology

077 Moisture Uptake and Chemical Compatibility of Semiconductor Plastic Encapsulant Materials
R. K. Lowry, R. Berriche, Intersil Corporation

083 A Novel Epoxy Encapsulant for CSP (µBGA®) - New Hydrophobic Epoxy Elastomer
Frank Y. Xu, Richard Bymark, 3M Company; Bin-Lin Hsu, Tessera, Inc.

090 Evaluation of the Environmental Protection of Photo BCB Polymers (Cyclotene™ 4000)
Jaili Wu, Randy Pike, C. P. Wong, Georgia Institute of Technology; Daniel Scheck, W. Boyd Rogers, Philip Garrou, Dow Chemical @ MCNC

097 Novel Single Pass Reflow Encapsulant for Flip Chip Application
Hui Wang, Torey Tomaso, Kester Solder - Litton Systems, Inc.

EXHIBITS OPEN
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WELCOME RECEPTION IN EXHIBIT HALL
6 PM - 8 PM

SESSION 5:
FLIP CHIP BUMPING

8AM – 10:30AM
Session Chairs:
Phil Deane, MCNC
Rolf Aschenbrenner, Fraunhofer Institute

BREAK: 10:30 AM - 10:50 AM

SESSION 6:
SOLDER

10:50AM – 12:55PM
Session Chairs:
Andrew Strandjord, IC Interconnect
Rajen Chanchani, Sandia National Laboratory

LUNCH IN THE EXHIBIT HALL
1 PM - 2 PM

EXHIBIT OPEN
9:30 AM - 7 PM

POSTERS IN EXHIBIT HALL
3 PM - 7 PM

SESSION 7:
FLIP CHIP

2PM – 4:30PM
Session Chairs:
Jianmin Qu, Georgia Institute of Technology
Li Li, Motorola

BREAK: 4:30 PM - 4:50 PM

Session 8:
Chip Scale Packages

4:50PM - 6:55PM
Session Chairs:
Michael Toepper, TUB/Fraunhofer IZM
Peter Elenius, Flip Chip Technologies

Wednesday, March 8

Session 9:
High Density Substrates

8AM - 10:05AM
Session Chairs:
Petri Savolainen, Nokia-Japan Co., Ltd.
Andreas Schubert, Fraunhofer Institute

BREAK: 10:05 AM - 10:25 AM

SESSION 10:
THERMOMECHANICS

10:25AM – 12:30PM
Session Chair:
Suresh Sitaraman, Georgia Institute of Technology

POSTER PAPERS - TUESDAY, MARCH 7

3 PM - 7 PM
Session Chair:
C.P. Wong, Georgia Institute of Technology

APPENDIX

MATERIALS & PROCESS TECHNOLOGY:

MATERIALS

The precursor to the NCF/NCP assembly technology is the formation of electrically conductive polymer bumps on the bond pads of a wafer. The P_FC^{TM} is used to stencil print the electrically conductive polymer, forming bumps that are 3 – 8 mil in diameter and 2-3 mil in height. The bond pad diameter is dictated by bond pad size, but the height of the bump needs to be a minimum of 50 microns and preferably 75 microns if pitch allows this. The bumps are then polymerized to make them hard and electrically conductive, although Bstage thermoset and high melting temperature thermoplastics can be used as well. The process will work best when the bumps have a peak shape . Table I depicts the properties of the E2101, and Fig. 1 shows the profile of the cured bumps.

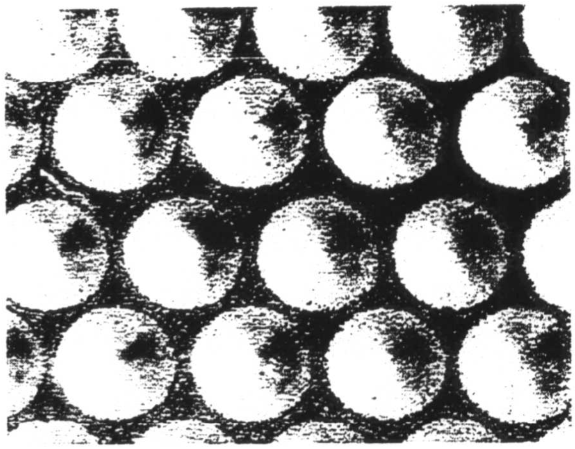
Table I: E2101

TYPICAL PROPERTIES

(To be used as a guideline only)

NUMBER OF COMPONENTS	Two
MIXING RATIO	PARTS BY WEIGHT
Part "A" (silver base)	3
Part "B" (hardener)	1
Stir contents of container "A" thoroughly before mixing with Part "B".	
CURE SCHEDULE (minimum bond line temperature - use one of the following)	
175°C	15 minutes
150°C	1 hour
PHYSICAL PROPERTIES	
Color	silver
Consistency	smooth, thixotropic paste
Specific Gravity	3.1
Viscosity (typical @ 23°C/2.5 rpm)	39,000 cPs
Thixotropic Index	4.8
Glass Transition Temp. (Tg)	100°C
Coefficient of Thermal Expansion	
Below Tg	43 x 10⁻⁶ in/in/°C
Above Tg	140 x 10⁻⁶ in/in/°C
Lap Shear Strength	1,500 psi
Die Shear Strength	> 3,200 psi
Degradation Temperature	420°C
Operating Temperature	
Continuous	150°C
Intermittent	300°C
Shore D Hardness	83
Outgas to 300°C	0.4%
Moisture Absorption (30 min/100°C)	0.35%
Storage Modulus	750,000 psi
Poissons Ratio	0.34
Specific Heat	10.75 x 10⁴ (J/g°K)
ELECTRICAL - THERMAL PROPERTIES	
Volume Resistivity	0.0001 to 0.0004 ohm-cm
Thermal Conductivity	2.0 W/m°K
CATION-ANION ANALYSIS	
Cl^-	29 ppm
Na^+	20 ppm
NH_4^+	25 ppm
K^+	5 ppm
Total Ion Content	0.9 mS/m
POT LIFE	3 days
SHELF LIFE	One (1) year when stored at room temperature.
REFRIGERATION NOT REQUIRED	

Figure 1



Once the wafer has been diced, the individual die are ready for flip chip mounting. The Flip Chip Bonder used for evaluation purposes was the Toray FC-100 , semiautomatic bonder which has a heated bonding head capable of reaching 350°C and alignment accuracy of 12.5 microns. Actual manufacturing assembly is accomplished using a Toray CF-1000 COF line that has multiple heads for high volume.

At this point utilizing a screen printable, Bstage polymer or a dispensable polymer can accomplish the process. Use of a B-stage polymer allows the user to screen print the polymer over the bond pads on the circuit substrate and dry the material. The substrates can be stored until the bonding of the chip is to be performed. These materials are typically solvent loaded, but a non-solvent paste can be screen printed if the chip are to be bonded immediately. In this case there is no need for a drying step . Table II shows the properties of the pre-printable underfill materials used in this study to form the non-conductive film .

The alternative process is to use a dispensable paste that is applied directly over the bond pads of the circuit just prior to placement of the flip chip. No solvent based encapsulants can be used as this will result is voiding and compromise reliability of the flip chip assembly. Table III shows the properties of the TE179-4 that has been used in the study. This material is used for the NCP assembly technique.

Table II: TE179

MATERIAL CHARACTERISTICS (typical)*:	
PHYSICAL PROPERTIES:	
Color:	
Before Cure:	Black
After Cure:	Black
Consistency:	Thixotropic paste – Screen printable
Viscosity (@ 23°C/5 rpm):	41,370 cPs
Specific Gravity:	1.4
Shore D Hardness:	40 – 50
Lap Shear Strength @ 23°C:	712 psi
Die Shear Strength @ 23°C:	8.2 Kg/2,788 psi
Degradation Temp:	309°C
Operating Temp:	
Continuous:	-55°C to 150°C
Intermittent:	-55°C to 300°C
Glass Transition Temp (Tg):	98°C
Coeff. of Thermal Expansion	
Below Tg:	68×10^{-6} in/in/°C
Above Tg:	149×10^{-6} in/in/°C
Outgassing to 300°C:	2.43%
@250°C:	0.72%
@200°C:	0.17%
ELECTRICAL PROPERTIES:	
Volume Resistivity:	$> 1.0 \times 10^{14}$ ohm - cm
THERMAL PROPERTIES:	
Thermal Conductivity:	0.5 W/m°K

Table III: TE179-4

MATERIAL CHARACTERISTICS (typical)*:	
PHYSICAL PROPERTIES:	
Color:	
Before Cure:	Black
After Cure:	Black
Consistency:	Thixotropic paste – Dispensable
Viscosity (@ 23°C/20 rpm)	12,053 cPs
Thixotropic Index:	1.8
Specific Gravity:	
Part A	1.43
Part B	1.05
Mixture:	1.40
Shore D Hardness:	80 - 85
Lap Shear Strength @ 23°C:	2,088 psi
Die Shear Strength @ 23°C	>10 Kg/3,400 psi
Degradation Temp	317°C
Operating Temp:	
Continuous:	-55°C to +150°C
Intermittent:	-55°C to +300°C
Glass Transition Temp (Tg):	92°C
Coeff. of Thermal Expansion:	
Below Tg:	54×10^{-6} in/in/°C
Above Tg	160×10^{-6} in/in/°C
Outgassing to 300°C:	3.4%
@250°C:	2.2%
@200°C:	1.2%
ELECTRICAL AND THERMAL PROPERTIES:	
Volume Resistivity:	$> 1.0 \times 10^{14}$ ohm - cm
Thermal Conductivity	0.5 W/m°K

The chemistry of both fillers allows for snap curing on the bonding stage at temperatures above 200°C.

The advantages of pre-application of the NCF or NCP encapsulants are significant:

ELIMINATION OF VOIDS

LOW CTE - HIGHER FILLER LOADINGS

THERMAL CONDUCTIVE FILLERS

SNAP CURE ABILITY ABOVE 200°C

GAP FILL IS ASSURED

NO POST UNDERFILL CURING

REDUCTION OF CAPITAL EQUIPMENT

HIGHER THROUGHPUT FOR DCA

NO VOIDS IN BUMP AREA

NCF & NCP PROCESS

In this study the test vehicle used was a SMART CARD. A flip chip on flex (CFOF) comprised of a Philips MIFARE chip mounted onto an antenna pattern on PEC. PEC is a co-polyester with enhanced thermal and dimensional stability. A screen printable conductive ink, EpoTek EE162-5, was printed onto the PEC and cured. The NCF or NCP encapsulant was then applied onto the antenna inlet, covering the active circuit pads, and the bump chip was then pushed through the non conductive encapsulant to make electrical contact with antenna pads. At the same time the heated thermode holding and pushing the chip with force was heated to a high temperature which cured the underfill in a few seconds.

The process sequence follows:

APPLY ENCAPULANT ON ANTENNA

DIE COLLET PICKS UP BUMPED CHIP

THERMODE HEATED ABOVE 200°C

CHIP ALIGNMENT AND FORCE APPLIED

CHIP PUSHES THROUGH UNDERFILL

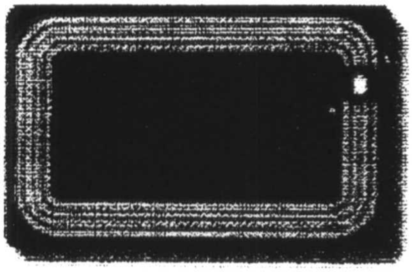
ELECTRICAL CONTACT ESTABLISHED

UNDERFILL CURES INSTANTLY

FLIP CHIP DEVICE FUNCTIONAL

The above process can be accomplished by pre-application of a continuous film, whether Bstage type or not, or by the dispensing of a paste. The finished chip & antenna device is shown in Fig. 2.

Figure 2



These processes have been developed over a two year period in a joint effort between Toray Equipment Corp. of Japan and Polymer Flip Chip Corp. of the United States. The process lends itself to high volume fast assembly of flip chip devices and offers significant cost reduction over the conventional underfill techniques currently practiced in the industry. Figures 3a and 3b illustrate the assembly process and basic parameters of the NCF and NCP processes. The following discussion deals with the experimental data that validated the processes as suitable for attachment of flip chip devices

FIGURE 3a
NON CONDUCTIVE PASTE; NCP*

- Printed underfill process : Polymer Bumps
- PFC, solderless flip chip bump technology
- Lower process steps, increase throughput
- Eliminate voids in underfill : Lower CTE
- Reduce capital equipment cost
- Reduce Flip Chip Assembly time
- Lower Cost & Higher Reliability

*NCP is patent and trademark pending.

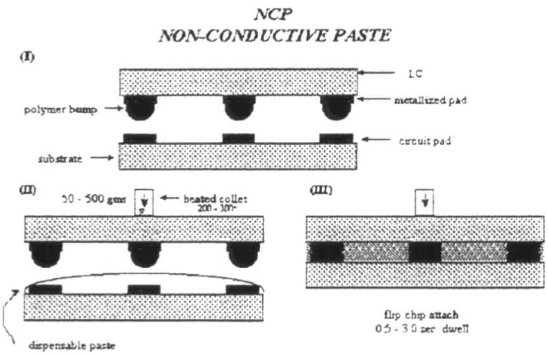
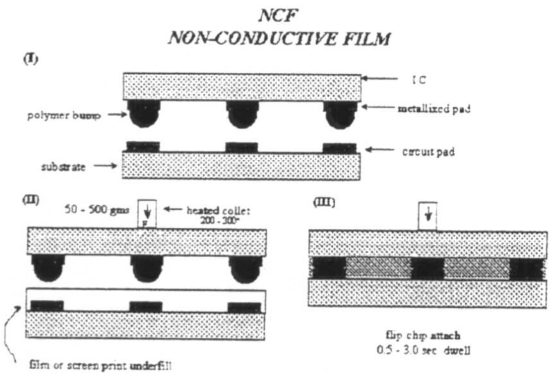


FIGURE 3b
NON CONDUCTIVE FILM; NCF*

- Printed underfill process : Polymer Bumps
- PFC , solderless flip chip bump technology
- Lower process steps, increase throughput
- Eliminate voids in underfill : Lower CTE
- Reduce capital equipment cost
- Reduce Flip Chip Assembly time
- Lower Cost & Higher Reliability

*NCF is patent and trademark pending.



(3b)

PROCESS VALIDATION

This section will deal primarily with the use of NCP as the assembly method as this has been our preferred approach to date. The results achieved with the NCF, pre-applied film, process is similar although the actual temperature and bonding force parameters are different.

A six turn coil antenna was designed for use with the Philips MIFARE chip in order to fabricate contactless smart card devices utilizing flip chip technology. The first set of experiments were conducted using ABS as the flexible substrate material. Table IV shows the antenna printing material used as well as the average NCP thickness after dispensing. In this study the Epo-Tek TE179 was used as the NCP material. The final thickness after bonding averaged 25 – 30 microns as the elastic polymer bumps are compresses during the bonding operation. This is the desired effect as the mountain shaped bumps pierce through the underfill and then expand or flatten to contact the entire bonding pad of the antenna while pushing underfill material out of the way. This insures better electrical contact of the bump to the antenna and a longer reading distance of the proximity card. The schematic in Figure 4 illustrates the areas where the 4 bumps are attached and Table V shows the results achieved after flip chip bonding.

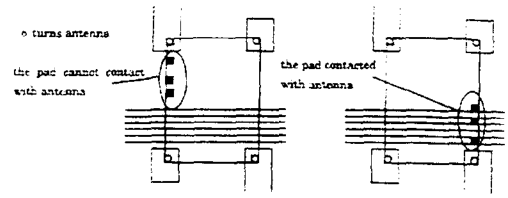
Table IV

NCP no.	pastes	viscosity(cps)
1	TE179	53,739 cps at2.5rpm@23C
2	TE179-1	middle? between 1 and 3
3	TE179 within 3% SiO2	136,476cps at2.5rpm@23C
4	TE179 within 5% SiO2	710,246 cps at0.5rpm@23C

Table V

NCP No	R(ohm)	pre-bond. load(gr)	pre-bond. time(sec)	main-bond. load(gr)	main-bond time(sec)	OD (mm)	sample No.
2	60	100	5	100	10	0	1
	62	80		80		0	2
	54					50	3
	54					85	4
	60	60		80		103	5
	52					131	6
	64	60		60		122	7
	62					131	8
3	57	80	5	80	10	65	9
	60					75	10
	55					131	11
	58					134	12
	48					134	13
	59					135	14
4	57	120	5	120	10	0	15
	60	100		100		75	16
	57					132	17
	61	60		80		115	18
	60					134	19
	61					134	20

Figure 4



The heated bonding tool was kept at a constant temperature of 100°C during a prebond step to contact the chip to the underfill after alignment, and the main bonding temperature was set at 380°C. Bonding times were kept constant and only the bonding force was changed to see the effect on the performance of the devices. On average, the best results were obtained by using a bonding force of 80 grams as evidenced by the reading distances of 120 – 130 mm. Maximum reading distance that can be achieved by this chip is 150 mm. Lower bonding forces were not adequate to make effective electrical contact and the 120gram force may have totally collapsed the bumps as the reading distances are either zero or very low.

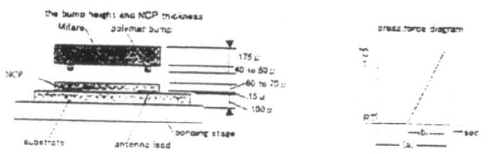
There was also concern that the viscosity of the TE179 may have been too low and there may have been poor wetting and adhesion of the chip to the substrate, this resulting in a lack of bump compression and dimensional stability. Another set of tests were conducted using PEC as the substrate and using the TE179 with an additional loading of 3% fumed silica to improve the thixotropic nature of the adhesive. A 100°C pre-bond and 380°C main bonding temperature were again used and this time a constant load of 80 grams was applied. The dwell times of 5 seconds for pre-bond and 10 seconds for main bonding were again used. A schematic of the NCP chip and substrate assembly is shown in Figure 5. Note that the bump height is 50 microns and the underfill paste thickness is initially set at 60 – 70 microns. When the bumps are pushed through the underfill to make contact with the conductive ink antenna, the final underfill thickness is around 30 microns. Having the underfill paste thicker than the bump height insures good wetting and 100% coverage of the gap between the substrate and chip. Success of the NCP process depends on having adequate force to quickly push the bumps onto the contact pads and piercing / displacing the underfill paste while heating and curing the paste at the same time. The process is accomplished in a matter of seconds; therefore the variables of temperature, force, and time must all be tightly controlled. The results of the second set of experiments is shown in Table VI. All 102 devices tested were functional, with an average operating distance greater than 80 mm. Six of the 102 shows poor operating distances. Subsequent analysis of these six units showed that too little underfill had been applied (dot size too small) and therefore the bumps were not held as tightly in compression by the shrinkage of the adhesive during cure.

Table VI

NO	R	OD	NO	R	OD	NO	R	OD	NO	R	OD
1	37.4	87	27	34.8	86	53	34.5	87	79	35.7	77
2	40.6	84	28	36.4	85	54	32.8	88	80	36.1	84
3	39.1	88	29	39.9	86	55	40.[illegible]	81	81	31.6	79
4	41.7	72	30	37.5	87	56	38.4	89	82	35.7	89
5	37.2	86	31	40.6	87	57	34.9	87	83	34.9	89
6	35.8	87	32	30.5	88	58	36.9	85	84	33.[illegible]	88
7	41.0	44	33	38.9	87	59	34.0	87	85	35.9	88
8	38.3	60	34	41.9	77	60	38.7	86	86	37.6	88
9	37.5	85	35	43.0	86	61	42.0	87	87	36.0	88
10	39.7	76	36	43.9	50	62	33.8	86	88	38.5	88
11	46.2	72	37	47.1	80	63	36.0	89	89	33.9	87
12	38.4	87	38	41.6	81	64	33.4	87	90	32.4	88
13	39.8	85	39	39.8	68	65	35.1	87	91	32.9	88
14	46.4	79	40	36.4	68	66	40.7	81	92	32.0	75
15	43.5	88	41	33.0	89	67	36.5	88	93	38.7	83
16	36.7	88	42	34.8	88	68	44.0	54	94	38.9	87
17	39.0	80	43	33.2	87	69	44.0	62	95	36.6	86
18	39.3	87	44	35.0	87	70	37.5	76	96	36.5	85
19	38.5	86	45	36.9	89	71	39.9	78	97	36.2	78
20	39.0	87	46	39.6	81	72	36.5	79	98	36.2	89
21	40.0	80	47	39.5	87	73	37.2	86	99	41.0	87
22	36.1	87	48	39.2	88	74	36.6	86	100	39.0	87
23	36.0	88	49	36.7	88	75	39.9	60	101	44.8	58
24	43.5	87	50	37.0	85	76	39.9	87	102	42.7	88
25	36.9	86	51	27.6	25	77	40.2	87			
26	39.8	84	52	33.6	87	78	34.0	88			
	ohm	mm		ohm	mm		ohm	mm		ohm	mm

Note : In order to be effective, the material selected for the NCF or NCP process must have snap cure potential . The polymer must be fully cured in less than 10 seconds at the designated

Figure 5



temperature or relaxation of the paste will occur once force is removed. The bumps will not be held rigidly and the device will be unreliable.

Figure 6 shows a photo of a chip bonded using the NCP process. There is excellent wetting of the chip and perfect alignment of the bumps to the antenna pads. What appears to be excessive voiding are actually filler particles in the paste. It should be noted that materials have to be optimized for minimal outgassing in order to reduce any tendency for voiding. In figure 7a and 7b the results of SAM testing are shown. The scanning acoustic microscope picks up voids in the otherwise dense matrix of the flip chip assembly. It is nearly impossible to eliminate voids , especially in a snap curable polymer, but they must be kept to a minimum. Voids in the area of the bumps can result in bump delamination. High molecular weight polymers, air release additives, and aggressive degassing can accomplish this.

Figure 6

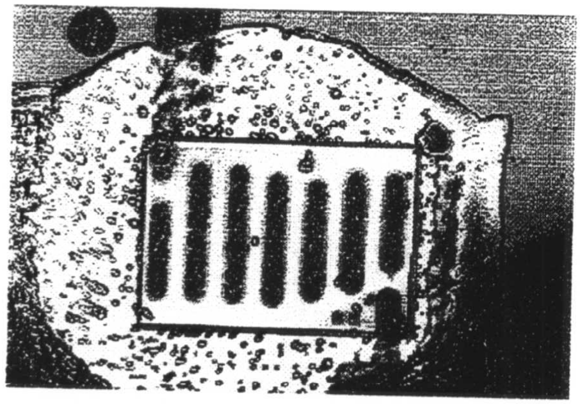


Figure 7a