Pentium™ Family User's Manual

Volume 2: 82496/82497 Cache Controller and 82491/82492 Cache SRAM Data Book

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One good thing

1979 – 8086 and 8088 CPU

leads to another...

1982 – 80286 CPU

and another...

1985 – Intel386™ CPU

and another...

1989 – Intel486™ CPU

and another...

1993 – Pentium™ Processor

1994 – Pentium™ Processor (90 & 100 MHz)

and another...and another...

奔腾™ 系列用户手册

第二卷 82496/82497 超高速缓存控制器与 82491/82492 超高速缓存 SRAM 数据手册

（英文版）

上海科学普及出版社

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Volume 2: 82496/82497 Cache Controller and 82491/82492 Cache SRAM Data Book

NOTE: The *Pentium™ Processor Family User's Manual* consists of three books: *Pentium™ Processor Family Data Book*, Order Number 241428; the *82496/82497 Cache Controller and 82491/82492 Cache SRAM Data Book*, Order Number 241429; and the *Architecture and Programming Manual*, Order Number 241430. Please refer to all three volumes when evaluating your design needs.

1994

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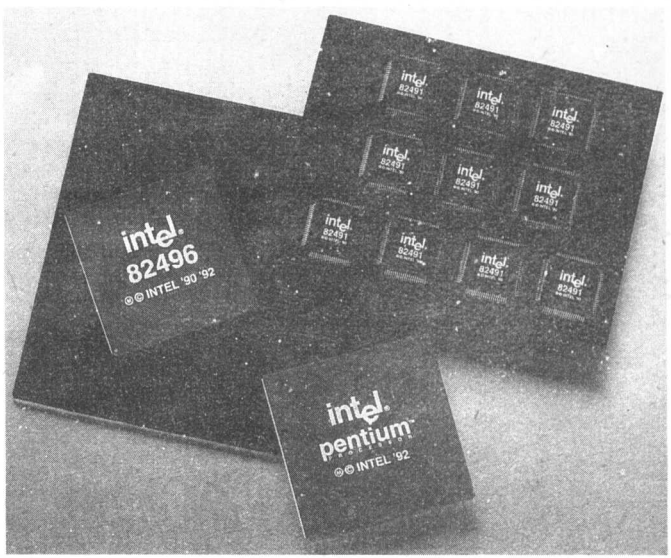
82496 CACHE CONTROLLER AND 82491 CACHE SRAM FOR USE WITH THE PENTIUM™ PROCESSOR (510\60, 567\66)

- **High Performance Second Level Cache**
  - Zero Wait States at 66 MHz
  - Two-Way Set Associative
  - Writeback with MESI Protocol
  - Concurrent CPU Bus and Memory Bus Operation
  - Boundary Scan
- **Pentium™ Processor (510\60, 567\66)**
  - Chip Set Version of Pentium™ Processor (510\60, 567\66)
  - Superscalar Architecture
  - Enhanced Floating Point
  - On-Chip 8K Code and 8K Data Caches
  - See *Pentium™ Processor Family Data Book* for More Information
- **Highly Flexible**
  - 256K to 512K with Parity
  - 32-, 64-, or 128-Bit Wide Memory Bus
  - Synchronous, Asynchronous and Strobed Memory Bus Operation
  - Selectable Bus Widths, Line Sizes, Transfers and Burst Orders
- **Full Multiprocessing Support**
  - Concurrent CPU, Memory Bus and Snoop Operations
  - Complete MESI Protocol
  - Internal/External Parity Generation/Checking
  - Supports Read For Ownership, Write-Allocation and Cache-to-Cache Transfers

The 82496 Cache Controller and multiple 82491 Cache SRAMs combine with the Pentium processor (510\60, 567\66) to form a CPU Cache chip set designed for high performance servers and function-rich desktops. The high-speed interconnect between the CPU and cache components has been optimized to provide zero-wait state operation. This CPU Cache chip set is fully compatible with existing software, and has new data integrity features for mission critical applications.



The 82496 cache controller implements the MESI write-back protocol for full multiprocessing support. Dual ported buffers and registers allow the 82496 to concurrently handle CPU bus, memory bus, and internal cache operation for maximum performance.

The 82491 is a customized high-performance SRAM that supports 32-, 64-, and 128-bit wide memory bus widths, 16-, 32-, and 64-byte line sizes, and optional sectoring. The data path between the CPU bus and memory bus is separated by the 82491, allowing the CPU bus to handshake synchronously, asynchronously, or with a strobed protocol, and allowing concurrent CPU bus and memory bus operations.

82497 CACHE CONTROLLER AND 82492 CACHE SRAM FOR USE WITH THE PENTIUM™ PROCESSOR (735\90, 815\100)

- **High Performance Second Level Cache**
  - **Zero Wait States at 66 MHz**
  - **Two-Way Set Associative**
  - **Writeback with MESI Protocol**
  - **Concurrent CPU Bus and Memory Bus Operation**
  - **Boundary Scan**
- **Pentium™ Processor (735\90, 815\100)**
  - **Chip Set Version of Pentium™ Processor (735\90, 815\100)**
  - **Superscalar Architecture**
  - **Enhanced Floating Point**
  - **On-Chip 8K Code and 8K Data Caches**
  - **See *Pentium™ Processor Family Data Book* for More Information**
- **Highly Flexible**
  - **256K to 512K with Parity**
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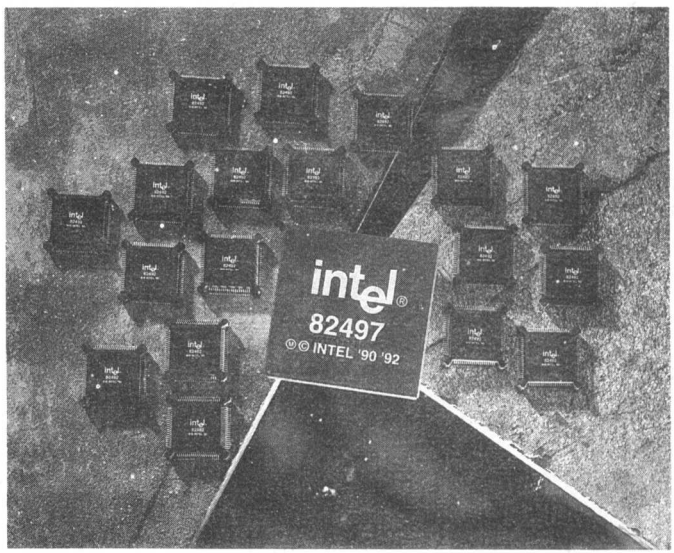
  - **Synchronous, Asynchronous and Strobed Memory Bus Operation**
  - **Selectable Bus Widths, Line Sizes, Transfers and Burst Orders**
- **Full Multiprocessing Support**
  - **Concurrent CPU, Memory Bus and Snoop Operations**
  - **Complete MESI Protocol**
  - **Internal/External Parity Generation/Checking**
  - **Supports Read For Ownership, Write-Allocation and Cache-to-Cache Transfers**

The 82497 Cache Controller and multiple 82492 Cache SRAMs combine with the Pentium processor (735\90, 815\100) to form a CPU Cache chip set designed for high performance servers and function-rich desktops. The high-speed interconnect between the CPU and cache components has been optimized to provide zero-wait state operation. This CPU Cache chip set is fully compatible with existing software, and has new data integrity features for mission critical applications.



The 82497 cache controller implements the MESI write-back protocol for full multiprocessing support. Dual ported buffers and registers allow the 82497 to concurrently handle CPU bus, memory bus, and internal cache operation for maximum performance.

The 82492 is a customized high-performance SRAM that supports 32-, 64-, and 128-bit wide memory bus widths, 16-, 32-, and 64-byte line sizes, and optional sectoring. The data path between the CPU bus and memory bus is separated by the 82492, allowing the CPU bus to handshake synchronously, asynchronously, or with a strobed protocol, and allowing concurrent CPU bus and memory bus operations.

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