

Pentium™ Family
User's Manual

intel®

Volume 2: 82496/82497 Cache Controller and
82491/82492 Cache SRAM Data Book

One good thing

1979 – 8086 and 8088 CPU

leads to another...



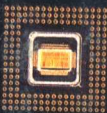
1982 – 80286 CPU

and another...



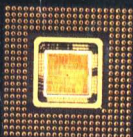
1985 – Intel386™ CPU

and another...



1989 – Intel486™ CPU

and another...



1993 – Pentium™ Processor

1994 – Pentium™ Processor
(90 & 100 MHz)



and another...and another...

奔腾™ 系列用户手册

**第二卷 82496/82497 超高速缓存控制器
与 82491/82492 超高速缓存 SRAM 数据手册**

(英文版)

上海科学普及出版社

Pentium™ Processor Family User's Manual

Volume 2: 82496/82497 Cache Controller and 82491/82492 Cache SRAM Data Book

NOTE: The *Pentium™ Processor Family User's Manual* consists of three books: *Pentium™ Processor Family Data Book*, Order Number 241428; the *82496/82497 Cache Controller and 82491/82492 Cache SRAM Data Book*, Order Number 241429; and the *Architecture and Programming Manual*, Order Number 241430.

Please refer to all three volumes when evaluating your design needs.

1994

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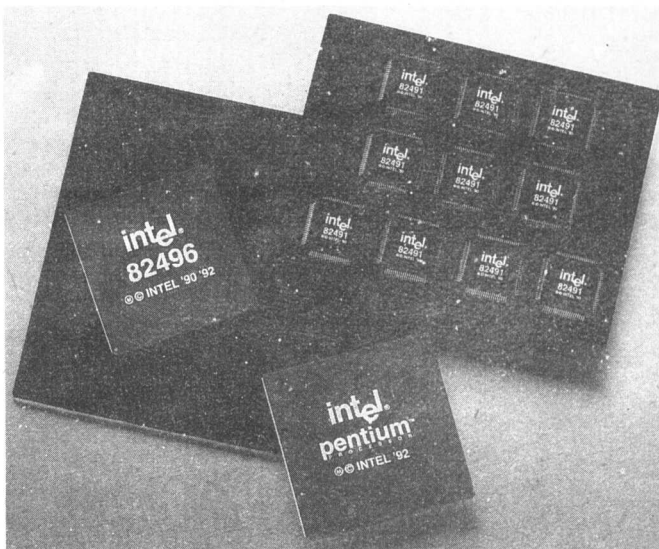
82496 CACHE CONTROLLER AND 82491 CACHE SRAM FOR USE WITH THE PENTIUM™ PROCESSOR (510\60, 567\66)

- **High Performance Second Level Cache**
 - Zero Wait States at 66 MHz
 - Two-Way Set Associative
 - Writeback with MESI Protocol
 - Concurrent CPU Bus and Memory Bus Operation
 - Boundary Scan
- **Pentium™ Processor (510\60, 567\66)**
 - Chip Set Version of Pentium™ Processor (510\60, 567\66)
 - Superscalar Architecture
 - Enhanced Floating Point
 - On-Chip 8K Code and 8K Data Caches
 - See *Pentium™ Processor Family Data Book* for More Information
- **Highly Flexible**
 - 256K to 512K with Parity
 - 32-, 64-, or 128-Bit Wide Memory Bus
 - Synchronous, Asynchronous and Strobed Memory Bus Operation
 - Selectable Bus Widths, Line Sizes, Transfers and Burst Orders
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The 82496 Cache Controller and multiple 82491 Cache SRAMs combine with the Pentium processor (510\60, 567\66) to form a CPU Cache chip set designed for high performance servers and function-rich desktops. The high-speed interconnect between the CPU and cache components has been optimized to provide zero-wait state operation. This CPU Cache chip set is fully compatible with existing software, and has new data integrity features for mission critical applications.

The 82496 cache controller implements the MESI write-back protocol for full multiprocessing support. Dual ported buffers and registers allow the 82496 to concurrently handle CPU bus, memory bus, and internal cache operation for maximum performance.

The 82491 is a customized high-performance SRAM that supports 32-, 64-, and 128-bit wide memory bus widths, 16-, 32-, and 64-byte line sizes, and optional sectoring. The data path between the CPU bus and memory bus is separated by the 82491, allowing the CPU bus to handshake synchronously, asynchronously, or with a strobed protocol, and allowing concurrent CPU bus and memory bus operations.





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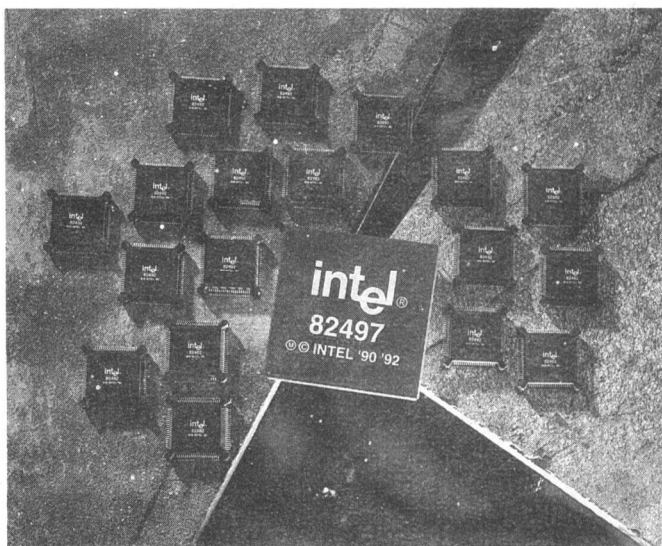


TABLE OF CONTENTS

PART I — 82496 Cache Controller and 82491 Cache SRAM

CHAPTER 1

PINOUTS

	Page
1.1. PINOUT DIAGRAMS	1-1
1.1.1. Pentium™ Processor Pinouts	1-1
1.1.2. 82496 Cache Controller Pinouts	1-3
1.1.3. 82491 Cache SRAM Memory Pinouts	1-5
1.2. PIN CROSS REFERENCE TABLES	1-7
1.2.1. Pentium Processor	1-7
1.2.2. 82496 Cache Controller	1-9
1.2.3. 82491 Cache SRAM	1-12
1.3. BRIEF PIN DESCRIPTIONS	1-12

CHAPTER 2

CACHE ARCHITECTURE OVERVIEW

2.1. MAIN FEATURES	2-2
2.2. CPU/CACHE CORE DESCRIPTION	2-2
2.2.1. 82496 Cache Controller	2-2
2.2.2. 82491 Cache SRAMs	2-3
2.2.3. Memory Bus Controller	2-4
2.3. CONFIGURATION	2-5
2.3.1. Physical Cache	2-6
2.3.2. Snoop Modes	2-6
2.3.2.1. SYNCHRONOUS SNOOP MODE	2-6
2.3.2.2. CLOCKED (ASYNCHRONOUS) SNOOP MODE	2-6
2.3.2.3. STROBED SNOOP MODE	2-6
2.3.3. Memory Bus Modes	2-7
2.3.3.1. CLOCKED MEMORY BUS MODE	2-7
2.3.3.2. STROBED MEMORY BUS MODE	2-7
2.4. Pentium processor BUS INTERFACE	2-7
2.5. 82496 Cache Controller/82491 Cache SRAM OPTIMIZED INTERFACE	2-8
2.6. MEMORY BUS INTERFACE	2-9
2.6.1. Snooping Logic	2-9
2.6.2. Cycle Control Logic	2-9
2.7. TEST	2-10

CHAPTER 3**COMPONENT OPERATION**

	Page
3.1. WRITETHROUGH CACHE DESIGNS	3-1
3.2. WRITEBACK CACHE DESIGNS	3-1
3.3. 82496 CACHE CONTROLLER CACHE CONSISTENCY PROTOCOL	3-2
3.4. MESI CACHE CONSISTENCY PROTOCOL MODEL	3-2
3.5. BASIC MESI STATE TRANSITIONS	3-3
3.5.1. MESI State Changes Resulting from CPU Bus Operations	3-5
3.5.1.1. READ HIT	3-5
3.5.1.2. READ MISS	3-6
3.5.1.3. WRITE HIT	3-6
3.5.1.4. WRITE MISS	3-6
3.5.1.5. WRITE MISS WITH ALLOCATION	3-7
3.5.2. MESI State Changes Resulting from Memory Bus Masters	3-7
3.5.2.1. SNOOPING	3-7
3.5.2.2. CACHE SYNCHRONIZATION	3-8
3.6. MESI STATE CHANGES FOLLOWING CYCLES WITH SPECIAL ATTRIBUTES	3-8
3.6.1. Cacheability Attributes: PCD, MKEN#	3-8
3.6.2. Writethrough Protocol: PWT, MWB/WT#	3-9
3.6.3. Read Only Accesses: MRO#	3-9
3.6.4. Locked Accesses: LOCK#	3-10
3.6.5. Direct-To-Modified Attribute: DRCTM#	3-10
3.7. STATE TRANSITIONS	3-10
3.7.1. CPU Bus Signals	3-11
3.7.2. Memory Bus Signals	3-11
3.7.3. Tag State and Cycles Resulting from State Transitions	3-12
3.7.3.1. TAG STATE	3-12
3.7.3.2. CYCLES RESULTING FROM STATE TRANSITIONS	3-12
3.7.4. MESI State Tables (82496 Cache Controller State Changes)	3-14
3.8. PRIMARY TO SECONDARY CACHE COHERENCY	3-17
3.8.1. Inclusion	3-17
3.8.2. Inquire and Back-Invalidation Cycles	3-18
3.8.3. Write Once Policy	3-19
3.8.4. MESI State Tables (Pentium Processor Cache Chip Set State Changes)	3-19

CHAPTER 4**CACHE INITIALIZATION AND CONFIGURATION**

4.1. CONFIGURATION SIGNAL SAMPLING DURING RESET	4-2
4.1.1. Initialization Required for Chip Set Mode	4-3
4.2. PHYSICAL CACHE	4-4
4.2.1. Memory Bus Width	4-5
4.2.2. Line Ratio	4-5
4.2.3. TagRAM Size	4-5
4.2.4. TagRAM Structure	4-5
4.2.5. Lines per Sector (L/S)	4-7
4.2.6. Cache Size	4-7
4.2.7. Configurable Address Connections	4-7
4.2.8. 82491 Cache SRAM Bus Configuration	4-9
4.2.9. 82491 Cache SRAM Parity Configuration	4-9
4.2.10. CPU to 82491 Cache SRAM Address Configurations	4-10
4.2.11. Bus Driver Buffer Selection	4-10

	Page
4.3. CACHE MODES	4-10
4.3.1. Memory Bus Modes	4-11
4.3.1.1. CLOCKED MODE	4-11
4.3.1.2. STROBED MODE	4-11
4.3.1.3. CONFIGURATION OF MEMORY BUS MODE	4-12
4.3.2. Snoop Modes	4-12
4.3.2.1. CONFIGURATION OF SNOOP MODE	4-12
4.3.3. Strong/Weak Write Ordering	4-13
4.3.3.1. DESCRIPTION	4-13
4.3.3.2. CONFIGURATION	4-13

CHAPTER 5

HARDWARE INTERFACE

5.1. MEMORY BUS CONTROLLER CONSIDERATIONS	5-1
5.1.1. Cycle Control	5-2
5.1.1.1. IDENTIFYING AND EXECUTING CYCLES	5-4
5.1.1.1.1. Read Hit	5-7
5.1.1.1.2. Cacheable Read Miss	5-7
5.1.1.1.3. Non-Cacheable Read Miss	5-8
5.1.1.1.4. Write Hit [E], [M]	5-8
5.1.1.1.5. Write Hit [S]	5-8
5.1.1.1.6. Write Miss: No Allocation, Allocation	5-8
5.1.1.1.7. Replacement	5-9
5.1.1.1.8. Snoop Writeback	5-9
5.1.1.1.9. Locked	5-9
5.1.1.1.10. Cache-To-Cache Transfer	5-10
5.1.1.1.11. Read For Ownership	5-10
5.1.1.1.12. I/O Cycles	5-11
5.1.1.1.13. Special Cycles	5-11
5.1.1.1.14. FLUSH and SYNC Cycles	5-11
5.1.2. Snooping	5-12
5.1.2.1. CHOOSING A SNOOPING MODE	5-12
5.1.2.1.1. Synchronous Snooping Mode	5-13
5.1.2.1.2. Asynchronous Snooping Mode	5-13
5.1.2.1.3. Strobed Snooping Mode	5-14
5.1.2.2. SNOOP OPERATION	5-15
5.1.2.3. SNOOP BLOCKING	5-18
5.1.2.4. WHEN SNOOPING IS NOT ALLOWED	5-21
5.1.2.5. SNOOPING DURING LOCKED CYCLES	5-22
5.1.2.5.1. Snooping during Split Locked Cycles	5-22
5.1.2.6. SNOOP WRITEBACK CYCLES	5-23
5.1.3. Address Integrity	5-23
5.1.3.1. CPU BUS ADDRESS PARITY	5-24
5.1.3.2. MEMORY BUS ADDRESS PARITY	5-24
5.1.4. Data Control	5-25
5.1.4.1. CPU DATA BUS TRANSFER CONTROL	5-25
5.1.5. Memory Bus Mode Selection	5-26

	Page
5.1.6. 82491 Cache SRAM Intelligent Dual-Ported Cache Memory.....	5-27
5.1.6.1. 82491 CACHE SRAM DATA PATH	5-27
5.1.6.2. MEMORY CYCLE BUFFERS.....	5-28
5.1.6.3. WRITEBACK AND SNOOP BUFFERS.....	5-28
5.1.6.4. MEMORY BUS CONTROL SIGNALS	5-28
5.1.6.5. 82491 CACHE SRAM PARITY DEVICES	5-30
5.1.7. Signal Synchronization.....	5-31
5.1.8. Warm Reset	5-32
5.1.9. Handling of Large Caches/Larger Line Sizes.....	5-32
5.1.10. 82496 Cache Controller Guaranteed Signal Relationships.....	5-33
5.1.11. 82496 Cache Controller Cycle Progress Requirements	5-34
5.1.12. 82496 Cache Controller Input Signal Recognition Requirements	5-34
5.1.13. 82496 Cache Controller and 82491 Cache SRAM CRDY# Requirements	5-35
5.1.14. 82496 Cache Controller Cycle Attribute Sampling Requirements.....	5-35
5.1.15. Pentium Processor, 82496 Cache Controller and 82491 Cache SRAM BRDY# Requirements.....	5-35
5.1.16. 82496 Cache Controller Cycle Progress Signal Sampling Requirements.....	5-36
5.1.17. 82491 Cache SRAM Data Control Signal Requirements.....	5-37
5.1.18. Semaphore (Strong Write Ordering) Consistency.....	5-37
5.2. DETAILED PENTIUM PROCESSOR CACHE CHIP SET PIN DESCRIPTIONS	5-39
5.2.1. Signal/Category Cross-Reference	5-39
5.2.1.1. CONFIGURATION SIGNALS	5-39
5.2.1.2. SNOOPING SIGNALS	5-39
5.2.1.3. CYCLE ATTRIBUTE/PROGRESS SIGNALS	5-39
5.2.1.4. CYCLE CONTROL SIGNALS.....	5-39
5.2.1.5. MEMORY ADDRESS BUS AND ADDRESS CONTROL SIGNALS	5-40
5.2.1.6. MEMORY DATA BUS AND DATA CONTROL SIGNALS	5-40
5.2.1.7. CACHE SYNCHRONIZATION SIGNALS.....	5-40
5.2.1.8. CPU SIGNALS.....	5-40
5.2.1.9. TEST SIGNALS	5-40
5.2.1.10. PENTIUM PROCESSOR BUS OPTIMIZED INTERFACE SIGNALS	5-40
5.2.1.11. 82496 CACHE CONTROLLER/82491 CACHE SRAM OPTIMIZED INTERFACE SIGNALS.....	5-40
5.2.2. Pentium Processor Cache Chip Set Detailed Pin Descriptions.....	5-41
5.2.2.1. A[31:3]/A[15:0].....	5-41
5.2.2.2. A20M#.....	5-42
5.2.2.3. ADS#.....	5-43
5.2.2.4. ADSC#.....	5-44
5.2.2.5. AHOLD	5-45
5.2.2.6. AP	5-46
5.2.2.7. APCHK#	5-47
5.2.2.8. APERR#	5-48
5.2.2.9. APIC#.....	5-49
5.2.2.10. BE#,BE[7:0]#.....	5-50
5.2.2.11. BGT#.....	5-51
5.2.2.12. BLAST#.....	5-53
5.2.2.13. BLE#.....	5-54
5.2.2.14. BLEC#.....	5-55
5.2.2.15. BOFF#.....	5-57
5.2.2.16. BP[3:2], PM/BP[1:0].....	5-58
5.2.2.17. BRDY#	5-59
5.2.2.18. BRDYC#.....	5-61

	Page
5.2.2.19. BRDYC1#	5-62
5.2.2.20. BRDYC2#	5-63
5.2.2.21. BREQ	5-64
5.2.2.22. BT[3:0]	5-65
5.2.2.23. BUS#	5-66
5.2.2.24. BUSCHK#	5-67
5.2.2.25. CACHE#	5-68
5.2.2.26. CADS#	5-69
5.2.2.27. CAHOLD	5-71
5.2.2.28. CCACHE#	5-72
5.2.2.29. CD/C#	5-73
5.2.2.30. CDATA[7:0]	5-74
5.2.2.31. CDTs#	5-75
5.2.2.32. CFA[6:0],SET[10:0],TAG[11:0]	5-77
5.2.2.33. CFG[2:0]	5-78
5.2.2.34. CLDRV	5-79
5.2.2.35. CLK	5-80
5.2.2.36. CM/IO#	5-81
5.2.2.37. CNA#	5-82
5.2.2.38. CPCD	5-83
5.2.2.39. CPWT	5-84
5.2.2.40. CRDY#	5-85
5.2.2.41. CSCYC	5-87
5.2.2.42. CW/R#	5-88
5.2.2.43. CWAY	5-89
5.2.2.44. D/C#	5-90
5.2.2.45. D[63:0]	5-91
5.2.2.46. DP[7:0]	5-92
5.2.2.47. DRCTM#	5-93
5.2.2.48. EADS#	5-95
5.2.2.49. EWBE#	5-96
5.2.2.50. FERR#	5-97
5.2.2.51. FLUSH#	5-98
5.2.2.52. FRCMC#	5-100
5.2.2.53. FSIOUT#	5-101
5.2.2.54. HIGHZ#	5-103
5.2.2.55. HIT#	5-104
5.2.2.56. HITM#	5-105
5.2.2.57. HLDA	5-106
5.2.2.58. HOLD	5-107
5.2.2.59. IBT	5-108
5.2.2.60. IERR#	5-109
5.2.2.61. IGNE#	5-110
5.2.2.62. INIT	5-111
5.2.2.63. INTR	5-112
5.2.2.64. INV	5-113
5.2.2.65. IPERR#	5-114
5.2.2.66. IU	5-115
5.2.2.67. IV	5-116

	Page
5.2.2.68. KEN#	5-117
5.2.2.69. KLOCK#	5-119
5.2.2.70. KWEND#	5-121
5.2.2.71. LOCK#	5-123
5.2.2.72. LR[1:0]	5-124
5.2.2.73. M/IO#	5-125
5.2.2.74. MALDRV	5-126
5.2.2.75. MALE	5-127
5.2.2.76. MAOE#	5-128
5.2.2.77. MAP	5-130
5.2.2.78. MAPERR#	5-132
5.2.2.79. MAWEA#	5-134
5.2.2.80. MBALE	5-135
5.2.2.81. MBAOE#	5-136
5.2.2.82. MBE#	5-138
5.2.2.83. MBRDY#	5-140
5.2.2.84. MBT[3:0]	5-142
5.2.2.85. MCACHE#	5-144
5.2.2.86. MCFA[6:0], MSET[10:0], MTAG[11:0]	5-146
5.2.2.87. MCLK	5-148
5.2.2.88. MCYC#	5-149
5.2.2.89. MDATA[7:0]	5-150
5.2.2.90. MDLDRV	5-152
5.2.2.91. MDOE#	5-153
5.2.2.92. MEOC#	5-154
5.2.2.93. MFRZ#	5-156
5.2.2.94. MHITM#	5-158
5.2.2.95. MISTB	5-159
5.2.2.96. MKEN#	5-160
5.2.2.97. MOCLK	5-161
5.2.2.98. MOSTB	5-163
5.2.2.99. MRO#	5-164
5.2.2.100. MSEL#	5-166
5.2.2.101. MSTBM	5-168
5.2.2.102. MTHIT#	5-169
5.2.2.103. MTR4/8#	5-170
5.2.2.104. MWB/WT#	5-171
5.2.2.105. MX4/8#	5-172
5.2.2.106. MZBT#	5-173
5.2.2.107. NA#	5-175
5.2.2.108. NENE#	5-177
5.2.2.109. NMI	5-178
5.2.2.110. PALLC#	5-179
5.2.2.111. PAR#	5-180
5.2.2.112. PCD	5-181
5.2.2.113. PCHK#	5-182
5.2.2.114. PEN#	5-183
5.2.2.115. PRDY	5-184
5.2.2.116. PWT	5-185
5.2.2.117. R/S#	5-186
5.2.2.118. RDYSRC	5-187
5.2.2.119. RESET	5-188

	Page
5.2.2.120. SCYC	5-190
5.2.2.121. SEC2#	5-191
5.2.2.122. SLFTST#	5-192
5.2.2.123. SMI#	5-193
5.2.2.124. SMIACT#	5-194
5.2.2.125. SMLN#	5-195
5.2.2.126. SNPADS#	5-196
5.2.2.127. SNPBSY#	5-198
5.2.2.128. SNPCLK	5-199
5.2.2.129. SNPCYC#	5-200
5.2.2.130. SNPINV	5-201
5.2.2.131. SNPMD	5-202
5.2.2.132. SNPNC#	5-203
5.2.2.133. SNPSTB#	5-205
5.2.2.134. SWEND#	5-207
5.2.2.135. SYNC#	5-209
5.2.2.136. TCK	5-211
5.2.2.137. TDI	5-212
5.2.2.138. TDO	5-213
5.2.2.139. TMS	5-214
5.2.2.140. TRST#	5-215
5.2.2.141. W/R#	5-216
5.2.2.142. WAY	5-217
5.2.2.143. WB/WT#	5-218
5.2.2.144. WBA	5-219
5.2.2.145. WBTP	5-220
5.2.2.146. WBWE#	5-221
5.2.2.147. WRARR#	5-222
5.2.2.148. WWOR#	5-223

CHAPTER 6

MEMORY BUS FUNCTIONAL DESCRIPTION

6.1. READ CYCLES	6-1
6.1.1. Read Hit Cycles	6-1
6.1.2. Read Miss Cycles	6-4
6.1.2.1. WITH CLEAN REPLACEMENT	6-4
6.1.2.2. WITH REPLACEMENT OF MODIFIED LINE	6-7
6.1.3. Non-Cacheable Read Miss Cycles	6-9
6.2. WRITE CYCLES	6-10
6.2.1. Write Hit to [E] or [M] State Cycles	6-10
6.2.2. Write Miss with No Allocation or Write Hit to [S] State Cycles	6-12
6.2.3. Write Miss with Allocation Cycles	6-14
6.3. LOCKED READ-MODIFY-WRITE CYCLES	6-16
6.4. SNOOP HIT TO [M] STATE — SYNCHRONOUS SNOOP MODE	6-18
6.5. I/O CYCLES	6-21

CHAPTER 7

ELECTRICAL SPECIFICATIONS

7.1. POWER AND GROUND	7-1
7.2. DECOUPLING RECOMMENDATIONS	7-1
7.3. CONNECTION SPECIFICATIONS	7-1

	Page
7.4. MAXIMUM RATINGS	7-1
7.5. DC SPECIFICATIONS	7-2
7.6. AC SPECIFICATIONS	7-4
7.6.1. Optimized Interface	7-4
7.6.1.1. FLIGHT TIME SPECIFICATION	7-5
7.6.1.1.1. 66-MHz 256-Kbyte Flight Times	7-9
7.6.1.1.2. 60-MHz 256-Kbyte Flight Times	7-12
7.6.1.1.3. 60-MHz 512-Kbyte Flight Times	7-15
7.6.1.2. SIGNAL QUALITY	7-18
7.6.2. External Interface	7-20
7.6.2.1. 66-MHz AC SPECIFICATIONS	7-21
7.6.2.2. 60-MHz AC SPECIFICATIONS	7-32
7.7. OVERSHOOT/UNDERSHOOT GUIDELINES	7-50

CHAPTER 8

I/O BUFFER MODELS

8.1. OPTIMIZED INTERFACE BUFFERS	8-2
8.2. EXTERNAL INTERFACE BUFFERS	8-5
8.3. INPUT DIODE MODELS	8-6

CHAPTER 9

MECHANICAL SPECIFICATIONS

CHAPTER 10

THERMAL SPECIFICATIONS

CHAPTER 11

TESTABILITY

11.1. BUILT-IN SELT TEST (BIST)	11-1
11.2. BOUNDARY SCAN	11-2
11.2.1. Boundary Scan Architecture	11-3
11.2.2. Test Data Registers	11-3
11.2.2.1. BYPASS REGISTER	11-4
11.2.2.2. BOUNDARY SCAN REGISTER	11-4
11.2.2.3. DEVICE IDENTIFICATION REGISTER	11-5
11.2.2.4. RUNBIST REGISTER	11-6
11.2.3. Instruction Register	11-6
11.2.3.1. Pentium processor Cache Chip Set BOUNDARY SCAN INSTRUCTION SET	11-6
11.2.4. Test Access Port (TAP) Controller	11-8
11.2.4.1. TEST-LOGIC-RESET STATE	11-9
11.2.4.2. CAPTURE-IR STATE	11-10
11.2.5. Boundary Scan Register Cell	11-10
11.2.5.1. PENTIUM PROCESSOR BOUNDARY SCAN REGISTER CELL	11-10
11.2.5.2. 82496 Cache Controller BOUNDARY SCAN REGISTER CELL	11-12
11.2.5.3. 82491 Cache SRAM BOUNDARY SCAN REGISTER CELL	11-13
11.2.6. Boundary Scan Description Language (BSDL)	11-13
11.2.7. Boundary Scan Signal Descriptions	11-13
11.3. 82491 CACHE SRAM TESTING	11-14

PART II — 82497 Cache Controller and 82492 Cache SRAM

CHAPTER 12

PINOUTS

12.1. 82497 CACHE CONTROLLER PINOUTS	12-1
12.2. 82492 CACHE MEMORY PINOUT	12-4

CHAPTER 13

PRODUCT OVERVIEW AND OPERATION

Page

13.1. FUNCTIONAL DIFFERENCES	13-1
13.1.1. BT[3:0] And MBT[3:0]	13-1
13.1.2. JTAG Scan Chain	13-1
13.1.3. Electrical & Thermal Differences	13-1
13.2. CHIP SET INTERFACE	13-2
13.2.1. Interface Overview	13-2
13.2.2. Chip Set Buffer Types	13-3

CHAPTER 14

ELECTRICAL SPECIFICATIONS

14.1. ABSOLUTE MAXIMUM RATINGS	14-1
14.2. D.C. SPECIFICATIONS	14-2
14.3. A.C. SPECIFICATIONS	14-4
14.3.1. Optimized Interface	14-4
14.3.1.1. FLIGHT TIME SPECIFICATION	14-5
14.3.1.1.1. 60-MHz Flight Times	14-6
14.3.1.1.2. 66-MHZ Flight Times	14-10
14.3.1.2. OPTIMIZED INTERFACE SIGNAL QUALITY SPECIFICATIONS	14-14
14.3.1.2.1. Ringback	14-15
14.3.1.2.2. Settling Time	14-15
14.3.2. External Interface	14-18
14.3.2.1. EXTERNAL INTERFACE A.C. TIMINGS	14-19
14.3.2.2. EXTERNAL INTERFACE SIGNAL QUALITY	14-36
14.3.2.2.1. Ringback	14-36
14.3.2.2.2. Settling Time	14-37

CHAPTER 15

I/O BUFFER MODELS

15.1. OPTIMIZED INTERFACE BUFFER PARAMETERS	15-1
15.2. EXTERNAL INTERFACE BUFFER PARAMETERS	15-6

CHAPTER 16

MECHANICAL SPECIFICATIONS

CHAPTER 17

TESTABILITY

17.1. 82497 CACHE CONTROLLER JTAG SCAN CHAIN	17-1
17.1.1. Pentium Processor (735\90, 815\100) JTAG Scan Chain	17-2

CHAPTER 18 THERMAL SPECIFICATIONS

APPENDIX A SUPPLEMENTAL INFORMATION

Figures

Figure	Title	Page
1-1.	Pentium™ Processor Pinout (Top View)	1-1
1-2.	Pentium™ Processor Pinout (Bottom View)	1-2
1-3.	82496 Cache Controller Pinout (Top View).....	1-3
1-4.	82496 Cache Controller Pinout (Bottom View).....	1-4
1-5.	82491 Cache SRAM Memory Pinout (Top View)	1-5
1-6.	82491 Cache SRAM Pinout (Bottom View).....	1-6
1-7.	Brief Pin Description Table Cross Reference	1-14
2-1.	82496 Cache Controller Block Diagram.....	2-3
2-2.	82491 Cache SRAM Block Diagram.....	2-4
2-3.	MBC Block Diagram	2-5
3-1.	State Changes.....	3-5
3-2.	Pentium™ Processor Cache Chip Set Cache Inclusion	3-17
4-1.	82491 Cache Controller/82491 Cache SRAM Configurations with the Pentium™ Processor.....	4-1
4-2.	Configuration Input Sampling.....	4-2
4-3.	CPU-Cache Chip Set Configuration Inputs	4-3
4-4.	Two-Way Set Associative TagRAM Structure.....	4-6
4-5.	Address Latching.....	4-8
5-1.	MBC Block Diagram	5-2
5-2.	Memory Bus Cycle Progress and Attribute Signals.....	5-3
5-3.	Cycle Progress Signals and Responses	5-3
5-4.	Synchronous Snoop Mode.....	5-13
5-5.	Clocked Snoop Mode.....	5-14
5-6.	Strobed Snoop Mode.....	5-15
5-7.	82496 Cache Controller Snooping Operations.....	5-16
5-8.	Fastest Synchronous Snooping.....	5-17
5-9.	Fastest Asynchronous Snooping.....	5-17
5-10.	Snoops without Invalidation.....	5-18
5-11.	Snoops with Invalidation	5-18
5-12.	Snoop Response During Cycles.....	5-19
5-13.	Snoop Response Blocking Using BGT#	5-20
5-14.	Snoop Executing before BGT# is Asserted.....	5-20
5-15.	New SNPSTB# Not Allowed.....	5-21
5-16.	Cycle Progress for Snoop Writeback Cycles	5-23
5-17.	MAPERR# Timing for Synchronous Snoop Mode	5-25
5-18.	MAPERR# Timing for Asynchronous Snoop Modes	5-25
5-19.	BRDY#/BRDYC#/BRDYC1#/BRDYC2# Interconnection	5-26
5-20.	82491 Cache SRAM Read Data Path.....	5-30
5-21.	Pentium™ Processor/82491 Cache SRAM Data Parity Connections	5-31
5-22.	512K Cache, 64-Bit Bus.....	5-33

Figure	Title	Page
5-23.	BLEC# Deassertion Due to ADS# Assertion.....	5-55
5-24.	BLEC# Assertion Due to CNA# or CRDY# Assertion	5-56
5-25.	BLEC# Assertion Due to Hit in 82496 Cache Controller TagRAM	5-56
5-26.	KLOCK# to LOCK# Relationship.....	5-119
5-27.	MAPERR# Timing.....	5-132
5-28.	MFRZ# Sampling.....	5-156
5-29.	Increasing Hold Time of Output Burst Data	5-161
5-30.	MZBT# Sampling.....	5-174
6-1.	Pipelined Read Hits	6-2
6-2.	Read Miss with Clean Replacement.....	6-4
6-3.	Read Miss with Replacement of Modified Line	6-7
6-4.	Non-Cacheable Read Miss	6-9
6-5.	Write Hits to [E] or [M] State Cycles.....	6-10
6-6.	Write Miss with No Allocation or Write Hit to [S] State Cycles	6-12
6-7.	Write Miss with Allocation to Modified Line	6-14
6-8.	Locked Read Modify Write Cycles.....	6-16
6-9.	Snoop Hit to [M] State — Synchronous Snoop Mode	6-18
6-10.	I/O Cycles	6-21
7-1.	Determination of Flight Time	7-6
7-2.	Derating the Flight Time.....	7-7
7-3.	In-System Measurement of Flight Time.....	7-8
7-4.	Driver and Receiver Signal Waveforms Showing Signal Quality Parameters.....	7-19
7-5.	Clock Waveform	7-43
7-6.	Valid Delay Timings	7-43
7-7.	Setup and Hold Timings.....	7-43
7-8.	Setup and Hold Timings in Strobed Snooping Mode	7-44
7-9.	Reset and Configuration Timings	7-44
7-10.	Memory Interface Timings	7-45
7-11.	Setup and Hold Timings to Strokes	7-45
7-12.	Setup and Hold Timings MxST.....	7-46
7-13.	Valid Delay Timings from Strokes	7-46
7-14.	Test Timings.....	7-47
7-15.	Test Reset Timings.....	7-47
7-16.	Active/Inactive Timings	7-48
7-17.	Overshoot/Undershoot and Ringback Guidelines	7-50
8-1.	First Order Input Buffer.....	8-1
8-2.	First Order Output Buffer	8-1
8-3.	Input Diode Model	8-7
8-4.	Complete Input Model Including Diode	8-8
9-1.	Pentium™ Processor Mechanical Specifications	9-3
9-2.	82496 Cache Controller Mechanical Specifications.....	9-5
9-3.	82491 Cache SRAM Mechanical Specifications.....	9-6
10-1.	Technique for Measuring Tcase	10-1
11-1.	Boundary Scan Register Structure of a Component	11-5
11-2.	Device ID Register.....	11-5
11-3.	TAP Controller State Diagram	11-9
12-1.	82497 Cache Controller Pinout Top Side View	12-2
12-2.	82497 Cache Controller Pinout Pin Side View	12-3
12-3.	82492 Cache Memory Pinout Top Side View.....	12-4
13-1.	Chip Set Interface.....	13-2
13-2.	Interface Buffer Types	13-3