1993 IEEE GaAs IC SYMPOSIUM

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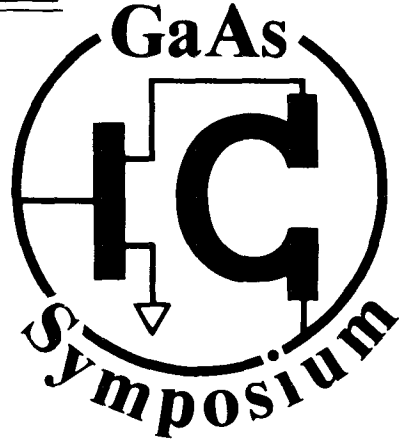
IEEE GALLIUM ARSENIDE INTEGRATED CIRCUIT SYMPOSIUM
Co-Sponsored by The IEEE Electron Devices Society
and The IEEE Microwave Theory and Techniques Society

15th ANNUAL



TECHNICAL DIGEST 1993

• SAN JOSE, CALIFORNIA •

OCTOBER 10-13, 1993

93CH3346-

GaAs IC Symposium
TECHNICAL DIGEST

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WELCOME TO SAN JOSE FOR THE 15th ANNUAL IEEE GaAs IC SYMPOSIUM

Here we are holding a Gallium Arsenide IC meeting in the heart of Silicon Valley! This is perhaps appropriate for a Symposium that is celebrating its 15th birthday, and is recognizing a developing maturity as more and more real GaAs applications are emerging and becoming commercially viable. This fact has had an impact on the type of papers submitted as well as on the criteria used for selection of the technical program. The demands articulated in the participant surveys each year are consistent in their request for more detail on applications and manufacturing of GaAs, and we take this direction as an important part of our mandate, especially in the context of the broad international attendance at this meeting. I am pleased to see a steady improvement of international representation at this conference; out of the 74 contributed and 12 invited papers at this year's meeting, 32 are from authors outside of the U.S. (in comparison to 24 non-U.S. out of the 72 papers at the 1992 Symposium).

Overall submissions were also up this year, and the above program was selected from 153 submitted abstracts. Especial thanks are due to Don D'Avanzo and his Technical Program Committee, who have worked hard as a team to select the best contributed papers, to identify and sign-up an excellent set of invited speakers, and to organize the popular Vendor Product Forums and topical Panel Discussion Sessions that help to make the GaAs IC Symposium your "one-stop shopping" venue for updates on the subject.

The range of subjects covered in the Technical Program emphasizes the tremendous breadth of this field, and in addition to the "here and now" applications, includes many papers discussing next generation technologies. HBT ICs are in greater abundance at this conference than ever before, and (in response to positive reactions from previous years) we have a couple of invited papers on the state-of-the-art capability in CMOS and Silicon Carbide technology.

Since most of us are in the business of innovating, it should come as no surprise to find another new feature in the 1993 program: the Sunday evening "GaAs Primer Course" offers an intensive tutorial on the basics of GaAs ICs, and is delivered by Don Estreich and Steve Long, both well-known experts in the GaAs industry. Art Geissberger is the 1993 Technical Program Vice-Chairman, and is responsible for organizing an excellent Short Course on "Wireless Systems and Applications of GaAs ICs for Telecom, Datacom and Automotive". This subject more than any other in the history of the Symposium will bring GaAs ICs into the hands of the consumer, and will provide the volume markets needed to create a solid commercial base for the technology. Art has compiled a set of expert specialists to give a series of authoritative and up-to-date tutorials in this exciting area.

Symposium participants also have the opportunity to renew their technical contacts with colleagues and suppliers from across the industry at the 1993 GaAs Industry Exhibition. A range of social functions (receptions, complimentary breakfasts and the Tuesday night theme party) also provide more relaxed opportunities for renewing old acquaintances and establishing new ones.

The Symposium program is designed to fit your needs, as perceived by the organizing committees. Please take the time to convey your suggestions and reactions (hopefully non-violent!) to members of the TPC or Executive Committee, and/or complete and return the Symposium Survey form. Your inputs are of great value to us.

Successful operation of the Symposium is a result of a lot of hard work by the volunteers who accept the various committee roles. My sincere thanks go out to them, to the members of the Technical Program Committee, the Executive Committee, the International Advisors, and to our IEEE Adcom representatives, for all the time and energy they devote to making this an excellent Symposium.

Take time to enjoy yourself and sample the offerings of San Jose, even though the conference timetable is *very* full!! Best regards to all of you, thank you for coming to the 1993 Symposium.

Paul R. Jay
Chairman
1993 IEEE GaAs IC Symposium

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WEDNESDAY, OCTOBER 13

PLENARY SESSION A

Monday, October 11, 1993-8:15 a.m.

GaAs ICs IN THE '90's: EMERGING APPLICATIONS AND COMPETITIVE TECHNOLOGIES

Chairpersons: **Elissa Sobolewski, ARPA, Arlington, VA**
Phillip Wallace, Anadigics, Warren, NJ

The $64,000 dollar questions today are "What can gallium arsenide do for me? and What do I get from other competing technologies?" Many within the III/V community have known the wonders of gallium arsenide for many years, but the applications have been slow in coming. Today, however, we are pleased to report that gallium arsenide integrated circuit technology has successfully made the transition from the laboratory to a mature manufacturing process. In many cases, devices with predictable performance are now being produced in large volumes at affordable prices. Impressive results are being obtained. GaAs ICs are being inserted in a variety of applications, both commercial and military.

All the papers in this session are invited papers and were chosen to specifically address emerging applications, to include: high performance computing and communications, high-speed optical transmission systems, and wireless data communications. Two papers in this session will address competing technologies to GaAs and discuss applications in the areas of: radio front ends, and high power microwave and high temperature electronics.

The first invited paper provides an overview of the Federal High Performance Computing and Communications Program. The results of this work will help to define the future of digital GaAs.

The second invited paper describes a new configuration for an ultra-high speed transmitter and receiver utilizing optical amplifiers (erbium doped fiber amplifier) at 20 Gbit/s.

The aim of the third invited paper is to give managers and designers a system overview of wireless data. This paper also discusses the current and near future balance between GaAs, bipolar and BiCMOS.

The second half of this session addresses competing technologies. The fourth invited paper concentrates on efforts in designing and building a state of the art radio front end for the Digital European Cordless Telecommunications (DECT) standard using components fabricated with advanced bipolar and CMOS processes. The final invited paper discusses advances in silicon carbide (SiC) device processing and substrate fabrication.

GaAs OPPORTUNITIES IN HIGH PERFORMANCE COMPUTING AND COMMUNICATIONS

John C. Toole and Richard B. Brown†

Computing Systems Technology Office
Advanced Research Projects Agency, Arlington, VA

†Electrical Engineering and Computer Science Dept.
University of Michigan, Ann Arbor, MI

ABSTRACT

High performance computing and networking are becoming the backbone of the scientific and information infrastructure, incorporating emerging technologies into productive applications at an accelerating pace. These technologies are important both for our national security and as the basis of our future economic competitiveness. The Federal High Performance Computing and Communications Program provides an innovative and coordinated research agenda for the US in these areas. The question of greatest interest to the III/V community is, "What role will emerge for compound semiconductors as computing reinvents itself?" This paper presents some insights, and a sample of the GaAs-related research funded by the Advanced Research Projects Agency. Results of these efforts will significantly contribute to the future role these semiconductors will play in mainstream computing.

INTRODUCTION

Advances in computing have created a new mode of scientific research, computational prototyping, that complements traditional theoretical and experimental methods and reuses the very technologies that are being developed. An example of this is the dependence of integrated circuit designers on computing for simulation and design verification. A similar dependence on computing is appearing in many other technical areas, giving high-performance computing a pervasive influence in engineering and science. The High Performance Computing and Communications (HPCC) Program is aimed at developing the basic information technologies needed to accelerate the commercial availability of computing and networking needed to address certain fundamental problems identified as 'grand challenge' and 'national challenge' problems. Examples of the 'grand challenge' problems (see Fig. 1) are: prediction of weather, climate, and global change; development of new semiconductor and high-temperature superconducting materials; design of microelectronic systems and advanced packages; understanding of molecular dynamics and quantum chromodynamics; design of drugs; and development of human-level machine speech and vision [1, 2].

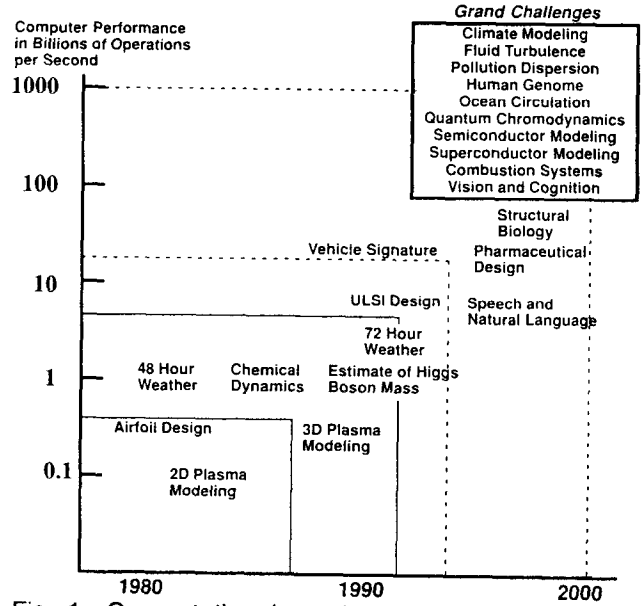

Fig. 1: Computational requirements for 'grand challenge' problems (from [2]).

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HPCC now involves ten different government agencies, and is focused on five complementary components: High Performance Computing Systems, Advanced Software Technology and Algorithms, the National Research and Education Network, Basic Research and Human Resources, and Information Infrastructure Technology and Applications. Among the federal agencies involved in HPCC, the Advanced Research Projects Agency (ARPA) has major responsibility for High Performance Computing Systems. In this area, underlying technologies and design tools are developed in prototype form as early as possible to allow empirical evaluation of alternative solutions. A vigorous research and development program stimulates innovation, develops technology, and assures that new approaches are adequately evaluated. Throughout the development cycle, results are fed back into the design process to refine successive prototypes.

The 'grand challenges' call for high performance systems capable of cost-effective, scalable computing, that is able to sustain trillions of operations per second (teraops) in configurations ranging from networked workstations to supercomputers. The speed and technical characteristics of gallium arsenide FET and bipolar devices offers many possibilities for helping achieve this level of performance. GaAs technologies pose interesting tradeoffs to the computer designer because they provide higher speed but lower integration levels than CMOS or BiCMOS. The complex interactions between technology, architecture, software, and design styles present many opportunities for exploring technology comparisons. Because of these interactions, the only feasible way to compare the effect of technologies on computing system performance is by building systems. A number of ARPA-funded projects are intended to explore the applicability of GaAs circuits to real computing systems, and to help the rapidly emerging GaAs technology base mature to the point that digital processes are stable and commercially viable.

In this paper we survey a few specific examples of ARPA-funded GaAs work. Though the presentation is oriented more toward physical design, (GaAs process technologies, design tools for these technologies, and architectures optimized for GaAs implementation) it is important to note that software and networking are vital aspects of high-performance computing. In high-performance systems, and in new technologies in particular, the importance of understanding the interdependence of hardware and software requires that they be designed concurrently.

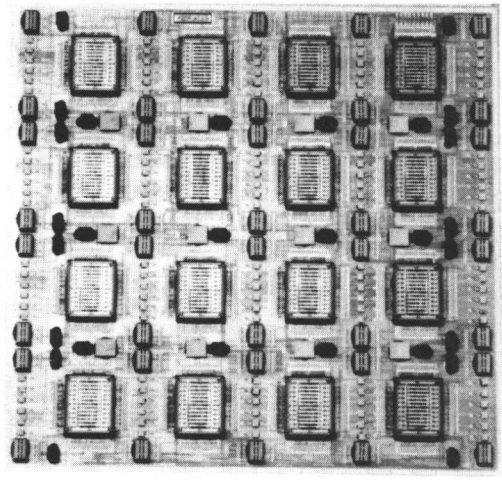

Fig. 2: Packaging test circuit implemented in 16 GaAs ICs fabricated at Vitesse, and mounted on an nCHIP MCM. (Courtesy of Mayo Foundation.)

TECHNOLOGY

At the foundation of high performance computing systems is semiconductor technology. The Computing Systems Technology Office (CSTO) at ARPA generally supports research at a higher level of abstraction than transistors, but it does fund computing research in systems using both FET [3, 4, 5] and bipolar [6, 7] technologies. Much early III/V materials and device (MESFET, MODFET and HBT) work was funded by what are now the Microelectronics Technology Office (MTO) [8] and the Electronics Systems Technology Office (ESTO) of ARPA. ARPA/MTO currently supports HBT development and modeling work with high-accuracy, high-sampling-rate interface electronics (multiplexors, D/As, and A/Ds) as technology drivers. This program will help establish a manufacturing capability for HBTs, and will provide an important demonstration for a variety of applications. Such an HBT A/D converter could, for example, significantly improve the performance of receivers for multiuser spread-spectrum wireless computer networks. ARPA/ESTO, which coordinated the MMIC program, continues to contribute to the technology base by supporting the advanced packaging which is needed to capitalize on the speed of GaAs logic circuits. The 16-chip GaAs test circuit for multichip modules (MCMs) shown in Fig. 2 is an example of the positive research interaction between advanced packaging and GaAs circuits [9]. The GaAs circuits facilitate MCM characterization at frequencies as high as 1 GHz.

Among ARPA's objectives are ensuring that the advanced technologies needed for future computing systems will be available. This entails a determination of where III/V technology fits in computing. In terms of circuit density, flexibility, and compatibility with other system components, silicon logic families have distinct advantages over any of the GaAs logic families. Innovative circuit design is needed to overcome the limitations of GaAs technologies. On the other hand, GaAs gates in both FET and bipolar processes have a significant speed advantage over CMOS. The common view is that CMOS is a lower-power technology than bipolar or FET GaAs, which both dissipate dc power; however, at very high frequencies this is not true [10]. Dynamic power is directly proportional to both the logic swing and clock frequency, and CMOS circuits have large logic swings. In circuits where most nodes have a high duty cycle, a great deal of power is dissipated in high-frequency CMOS circuits. In contrast, MESFET direct-coupled FET logic (DCFL) has a small logic swing (clamped by the diode transistor-gate of the subsequent logic stage), so that total power dissipation is only a weak function of clock frequency. (The dynamic power is still a function of frequency, but it is a small percentage of the total power.) The dc power is about constant because DCFL is current-steering logic. ECL-type HBT circuits dissipate even more low-frequency power, but because they have very well controlled threshold characteristics, they can have even smaller logic-swings. As clock frequencies continue to rise, this effect will become more important.

DESIGN TOOLS

In the design of large digital circuits, the practicality of using a given technology is dependent upon the design tools available. CAD tools can also help designers take better advantage of the performance potential offered by a technology. As noted in [11, 12], one of the most cost-effective approaches for improving circuit performance is development of better design methodologies and CAD tools. ARPA/CSTO funding has led to the availability of electromagnetic modeling and gate-array tools [13], symbolic tools for a high-performance HBT gate-array [7], GaAs logic-gate and interconnect macromodels [14], and a MESFET DCFL circuit compiler which has been commercialized [12, 15].

A new ARPA/MTO high-speed circuit design program encompasses both HBT and CMOS technologies [16]. Better large-signal HBT device models are to be developed and design tools for both HBT and CMOS circuits are to be extended to account for high-speed timing analysis, distributed electromagnetic effects, I/O driver limitations, and other effects that limit performance. A design methodology for GaAs computers should support efficient architectural studies and tradeoff analysis spanning the architecture, integrated circuits and software. It should provide a fast design and implementation cycle and efficient verification of the design. To optimize such circuits, one would like to have tools that allow static timing analysis to operate over all of the chips on an MCM. A recent initiative from ARPA/ESTO and CSTO calls for such design optimization [17].

ARCHITECTURE

For GaAs to compete in computing applications, system and chip architectures must be tuned to take advantage of its strengths and overcome its limitations. Two examples will be presented. The first of these is a RISC microprocessor in development at the University of Michigan [18]. The chip set will include a CPU, floating point accelerator (FPA), memory management unit (MMU), and SRAM. (See [15] for photos of previous GaAs CPUs.) The design has been optimized using trace-driven simulation of the whole system (including multiprogramming-application, OS, and kernel references) and kernel-based simulation of TLBs and caches. To keep yields up, the superscalar CPU chip will be limited to approximately 550,000 transistors. This integration-level restriction limits on-chip memory to a 32×32 register file, a 16k-bit instruction cache, and a few FIFOs and buffers. To compensate for the small primary instruction cache and off-chip primary data cache, the processor will do extensive prefetching of instructions and data. Many such design tradeoffs have been made to fit the architecture of the CPU, FPA, MMU and SRAM to GaAs technology.

The second example is the Tera computer, a major commercial effort which is integrating novel software and communications approaches with MESFET technology to achieve cost-effective high performance computing. The current implementation of the Tera architecture can have as many as 256 processors, each of which can have as many as 128 processing streams. The machine exploits shared memory, heavy pipelining, multithreading, and advanced operating system and compiler techniques to exploit parallelism and keep the processors busy. The architecture is a good match for GaAs circuits because the