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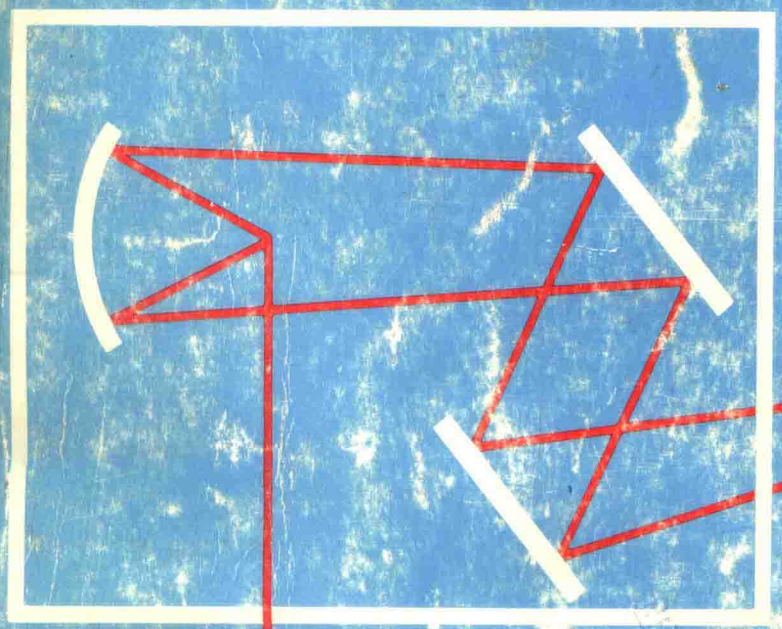

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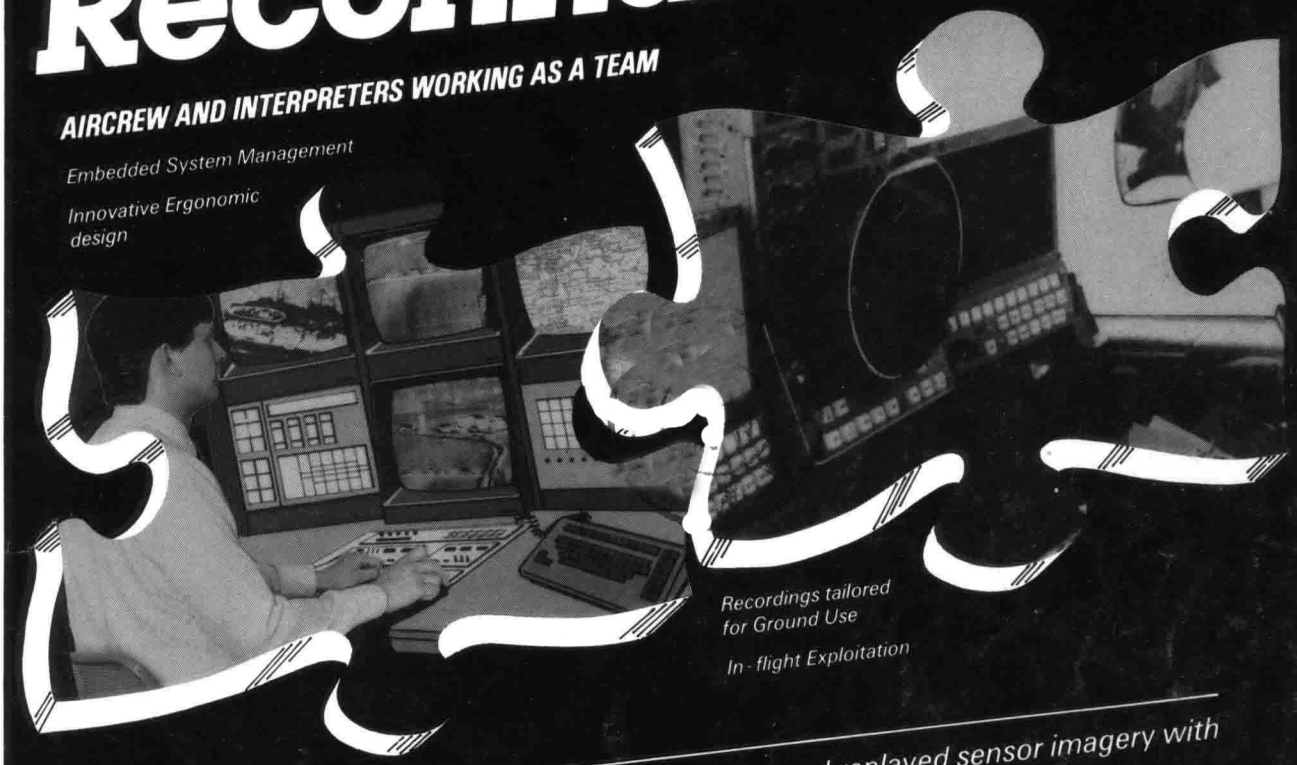

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# SCHOTTKY-BARRIER IR-CCD FOCAL PLANE ARRAYS

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## ABSTRACT

Schottky-barrier IR-CCD focal plane arrays with 128 x 64 picture elements were developed. The device utilizes n-channel CCD shift registers with an interline transfer format. The transfer inefficiency of the CCDs is approximately $2 \times 10^{-5}$. To achieve high photoresponse the Schottky-barrier detectors are constructed with a thin PtSi-layer separated from an aluminum mirror by a layer of $Si_3N_4$. The thickness of the $Si_3N_4$ layer is adapted to the wavelength of about 4 µm. The device is illuminated from the backside. The focal plane arrays show an excellent homogeneity of the responsivity. Quantum efficiencies of several percent are achieved. The black body (500 K) detectivity of the devices is in the order of $1 \times 10^{11}$ cm $W^{-1}$ $sec^{-1/2}$ measured with a cooled filter in the wavelength range 3,3 - 3,5 µm.

## INTRODUCTION

In the last years PtSi Schottky-barrier diodes (SBD) have drawn much attention for infrared (IR) imaging (1-3). Inspite of their relatively low quantum yield they seem to be a very interesting alternative for the 3 - 5 µm range. They have several advantages over other IR detector systems.

As monolithic twodimensional sensor arrays with CCD readout can be made on standard MOS-IC grade silicon it is possible to realize arrays with very high number of pixels (4,5). Furthermore an excellent uniformity of the responsivity and a very low cross talk have been demonstrated. The SBD is used in a self limiting mode, that means antiblooming is automatically included.

With compound semiconductors like CMT or InSb monolithic solutions are not possible in the near future as adequate readout structures like CCDs cannot be realized on these materials. In the case of extrinsic silicon, where indium doped silicon is the preferred material for the 3 - 5 µm range, also monolithic linear and twodimensional arrays with CCD readout have been realized. The main disadvantage of indium doped silicon is its low operating temperature of about 50 K.

This paper describes the construction and the detection mechanism of SBD roughly. IR measurements at simple detector structures are given and possible improvements are discussed. A linear array and a twodimensional array have been realized. The layout and the technological process is explained and some experimental results with these sensors are given.

## DETECTOR STRUCTURE AND EXPERIMENTAL RESULTS

The construction of the PtSi SBD is shown in figure 1. A thin PtSi film is formed on a p-type Si substrate. $n^+$ guard rings are used to reduce the fieldstrength at the perimeter of the diode and to contact the diode. The PtSi film is covered by a dielectric layer (e. g. $SiO_2$ or $Si_3N_4$) of suitable thickness and a reflecting aluminum mirror. The SBD is irradiated through the p-type Si substrate. As only part of the IR radiation is absorbed in the PtSi film the transmitted IR light will be reflected at the Al mirror of the optical cavity resulting in an enhanced optical absorption.

Due to the absorption of IR photons hot holes are generated in the PtSi film. If the hot-hole momentum normal to the barrier corresponds to a kinetic energy that is higher than the Schottky-barrier height, internal photoemission of the hole into the silicon occurs (1). The maximum wavelength $\lambda_o$ required to excite a hole over the barrier is given by the Schottky-barrier height $\Psi ms$.

$$h \cdot c/\lambda_o = \Psi ms$$

If very thin silicide films with a thickness t smaller than the mean free path length L of the hot holes are used multiple reflections of the excited holes at the PtSi-Si interface as well as at the PtSi-dielectric interface have to be considered and lead to an increase of the emission probability (3).

Approximately the quantum yield Y of the SBD can be described by the Fowler equation

$$Y(h\nu) = C \cdot (h\nu - \Psi ms)^2/h\nu$$

where $h\nu$ is the photon energy, $\Psi ms$ the barrier height and C the quantum efficiency coefficient depending on the characteristic of the PtSi film and the optical cavity (6). In figure 2 $(Y \cdot h\nu)^{1/2}$ is plotted against photon energy for simple SBD structures with PtSi films of different thicknesses and without an optical cavity. From these measurements a barrier height $\Psi ms$ of about 0,23 eV and a C-value of about 13 % are determined for the 100 Å thick PtSi film. For this sample a quantum yield of about 1.2 % and a responsivity of about 0.029 A/W are measured at 3 µm. The measurements are carried out at 77 K. The IR sensitive area of the Schottky-contact is 100 µm x 100 µm, and is surrounded by an $n^+$-type guard ring structure. Due to the guard ring the breakdown voltage of the SBD is greater than 40 V and the leakage current is less than 1 pA at a typical reverse voltage of 5 V.

Modelling calculations show that SBDs with thin PtSi layers and an optical cavity on top give an improved sensitivity in the 3 - 5 µm range.

Figure 3 shows the improvement in responsivity for a SBD with a 50 Å thick PtSi layer and an optical cavity. A further improvement of the sensitivity by about 25 % is possible with antireflection coating on the irradiated side of the Si substrate.

## 128 ELEMENT LINEAR ARRAY AND 128 x 64 ELEMENT TWODIMENSIONAL ARRAY

### Construction of 128 element PtSi IR-CCD line sensor

The linear array consists of 128 SBD detector elements, each with an active area of 50 µm x 50 µm. The pitch between 2 detector elements is 80 µm (see table 1). A 4 phase CCD is used for serial readout. At the end of the CCD the charge package is picked up by a floating diffusion and is fed to the gate of a single stage source follower. Additional structures allow skimming or background subtraction directly at the detector elements.

TABLE 1 - Layout data of 128 element PtSi IR-CCD line sensor

| | |
|---|---|
| number of pixels | 128 |
| size of detector element | 50 x 50 $\mu m^2$ |
| pitch | 80 µm |
| length of line sensor | about 10.2 mm |
| readout structure | 4 phase CCD |
| CCD-channel width | 60 µm |

Figure 4 shows the structure of one pixel of the line sensor. The PtSi SBD is surrounded by an $n^+$-guard ring. A transfer gate is used to inject the accumulated charge of the detector under the phase-1 gate of the buried channel CCD and to reset the detector for the next integration period. The transistor structure opposite to the CCD is used for skimming operation. If skimming operation is applied only part of the collected charge is injected into the CCD. The remaining charge is dumped via the second transfer gate to the $n^+$-diffusion. The device is fabricated with a conventional 2-level polysilicon gate process on 17 - 33 Ωcm p-type silicon substrate of <100> orientation. The CCD can be realized as a surface channel CCD (SCCD) or with an additional mask and an n-diffusion step as a buried channel CCD(BCCD). After completion of the CCD structure, but before metallization with aluminum, Pt is deposited by eveporation or sputtering into the opened Schottky-contact areas. After forming the PtSi at temperatures between 400 and 600° C the unreacted Pt is etched in hot aqua regia. Before metallization a $Si_3N_4$ layer is deposited on the silicide. After completion of the frontside processing the wafer backside is polished by conventional methods. Figure 5 shows a microphotograph of a part of the 128 element PtSi IR-CCD line sensor with the source follower output structure.

### Construction of 128 x 64 element PtSi IR-CCD sensor

The 128 x 64 element sensor is an interline transfer IR-CCD using 3 phase surface or buried channel CCDs for the charge transport in the horizontal and the vertical direction. Also with this sensor skimming operation is possible directly at the detector elements. The relevant data of this sensor are summarized in table 2.

TABLE 2 - Data of 128 x 64 element PtSi IR-CCD sensor

| | |
|---|---|
| Mode of operation | photo voltaic, PtSi SBD |
| number of pixels | 128 x 64 |
| size of detector element | 45 x 35 $\mu m^2$ |
| size of pixel | 65 x 130 $\mu m^2$ |
| readout design | interline transfer |
| chip size | 132 $mm^2$ |
| detectivity | about $1 \cdot 10^{11}$ cm $W^{-1} sec^{-1/2}$ |
| operating temperature | 80 K |

A cross sectional view of a pixel in figure 6 illustrates the coupling of the detector element to the horizontal CCD and to the skimming structure which is similar to that of the linear sensor. The PtSi SBD detector elements have a size of 45 µm x 35 µm. An optical cavity consisting of a dielectric layer of suitable thickness and an aluminum mirror is used to improve the sensitivity. The pitch between 2 detector elements is 65 µm in the horizontal and 130 µm in the vertical direction. The total chip area is about 132 $mm^2$ with an imaging area of about 70 $mm^2$. A 1 mm wide rim is used to mount the chip with good thermal contact on to a special ceramic frame which allows back side IR-illumination.

The device is fabricated similar to the line sensor except that a 3-level polysilicon gate process is applied with self alignment for the gate to drain and source overlap. Microphotographs of the complete sensor chip and an magnification of the top right part with the single stage source follower output structure and a schematic electric diagram are given in figures 7 and 8.

### Device Measurements

The performance of both sensor arrays are evaluated with experimental set ups which allow to change clocking frequency and integration time as well as the operating temperature. The output signals can either be monitored with an oscilloscope or be measured with a 12 bit transient recorder.

When using the transient recorder correlated double sampling is applied to reduce the influence of external noise sources. Typical integration times are in the range of 10 to 50 ms. To reduce electrical crosstalk miniaturized coaxial cables are used for the clocking pulses, the dc voltages and for the output signal. Most of the measurements are done with cold filter (band width 3.3 - 3.5 µm).

For both types of sensors the operating temperature can be varied between 70 K and 90 K without any degradation of the responsivity and the detectivity. The transfer inefficiencies of the CCDs are about $2 \cdot 10^{-4}$ for the SCCD and about $2 \cdot 10^{-5}$ for the BCCD.

Nonuniformities of responsivity below 2 % have been measured so far. The uniformity can be improved by optimization of the process steps of the SBD. The excellent uniformity is one main advantages of SBD sensors compared to other common used IR-sensitive materials.

For the 128 x 64 element sensor array with a 50 Å thick PtSi film a detectivity of about $1 \cdot 10^{11}$ cm $W^{-1}$ sec $^{-1/2}$ has been measured at 80 K (500 K black body with 3,3 - 3,5 µm cold filter). In figure 9 the dependence of the output signal on the irradiance is given for one detector element of the 128 x 64 sensor array. Within the dynamic range a linear relationship is found. Saturation of the output signal ocurrs at about 2.0 V for the 128 x 64 sensor array as well as for the line sensor.

The crosstalk of PtSi SBD IR-CCDs has been evaluated with a focussed HeNe-laser beam at a wavelength of 3.39 µm. With a laser spot size of about 25 µm in diameter one detector element of the line sensor is irradiated. The output signal of a part of the IR-CCD line sensor is shown in figure 10. The optical crosstalk between adjacent detector elements is about 5 %.

## SUMMARY

PtSi Schottky-barrier diodes seem to be a real alternative for IR imaging in the 3 to 5 µm wavelength range. A linear CCD sensor array with 128 pixels and a two-dimensional CCD sensor array with 64 x 128 pixels have been realized. The main advantages of such a system are monolithic construction with CCD readout on the chip, the possibility to use standard MOS-IC grade silicon as starting material and the good uniformity of responsivity. Therefore it is predestinated for the realization of imaging arrays with a great number of pixels(>$10^5$). The relatively low quantum yield has been improved by the use of an optical cavity and very thin PtSi-layers. Further improvement will be possible with an antireflection coating on the irradiated side and measures to reduce the barrier height.

This development is supported by the German Ministry of Defence.

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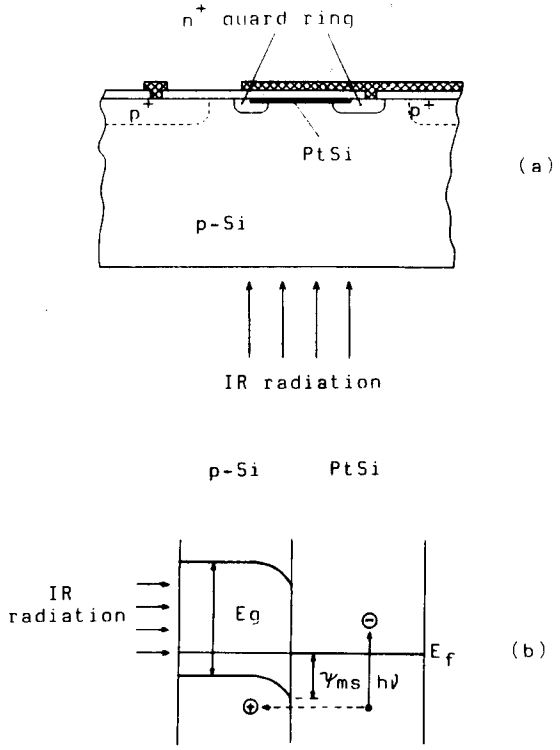



Figure 1 Detector structure with optical cavity (a) and simplified energy band diagram of Schottky-barrier diode (b)

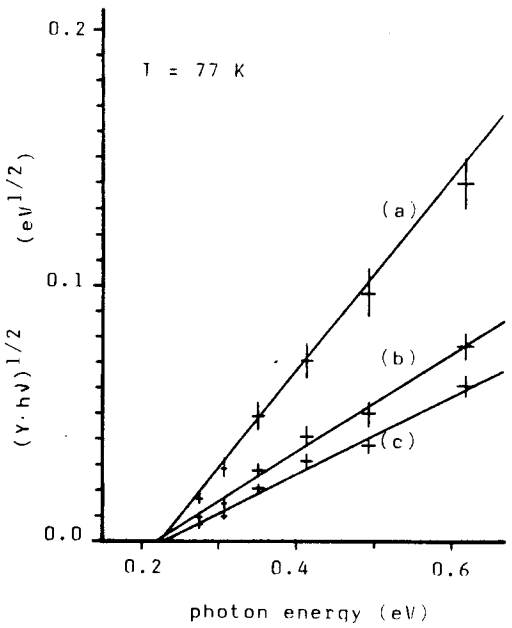



Figure 2 Fowler plots for SBDs without optical cavity (thickness of PtSi films : (a) 100 Å, (b) 200 Å, (c) 400 Å)

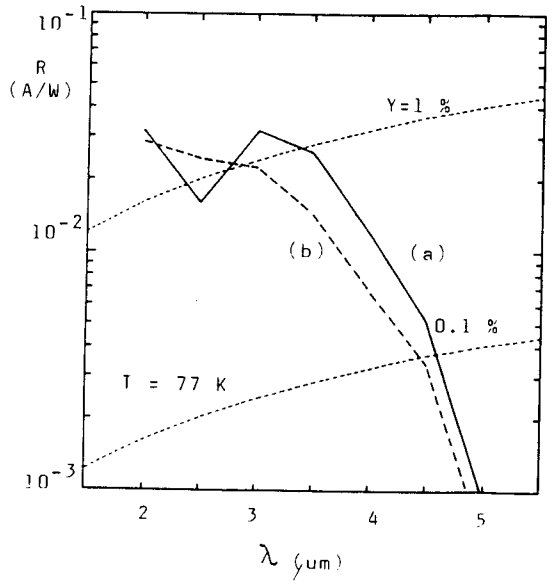



Figure 3 Measured responsivities for SBD detectors with (a) and without (b) Al reflector on top of 0.63 μm $Si_3N_4$ ($t_{PtSi}$ = 50 Å)

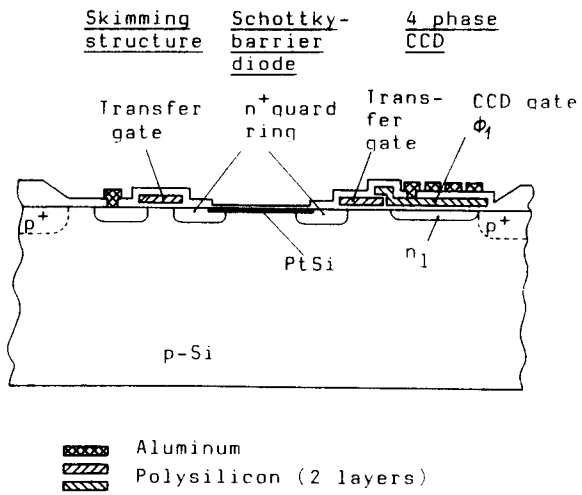



Figure 4 Cross sectional view of 128 element PtSi IR-CCD line sensor without optical cavity

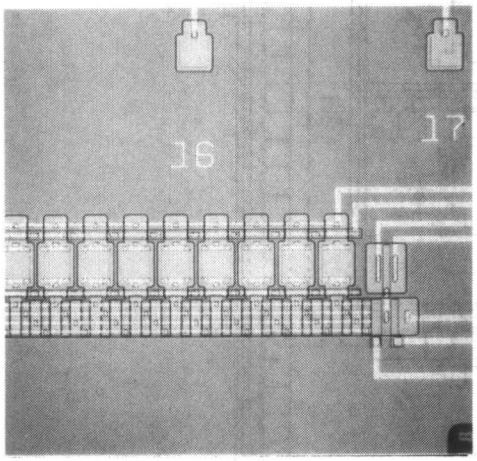



Figure 5 Microphotograph of 128 element PtSi IR-CCD line sensor showing part of the sensor array with the source follower output structure

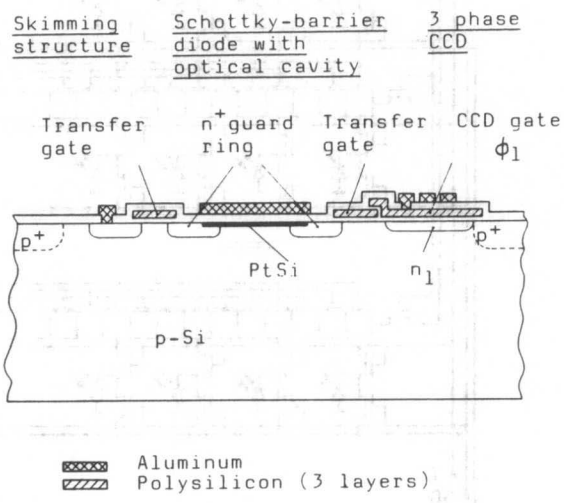
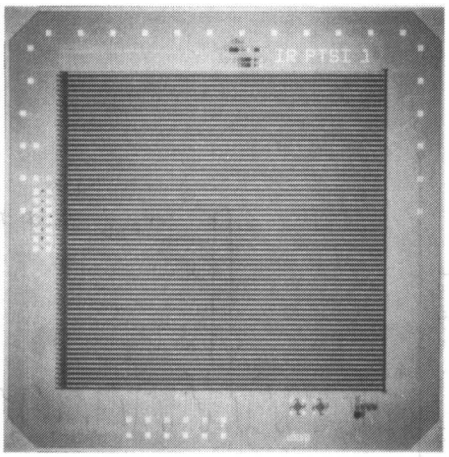
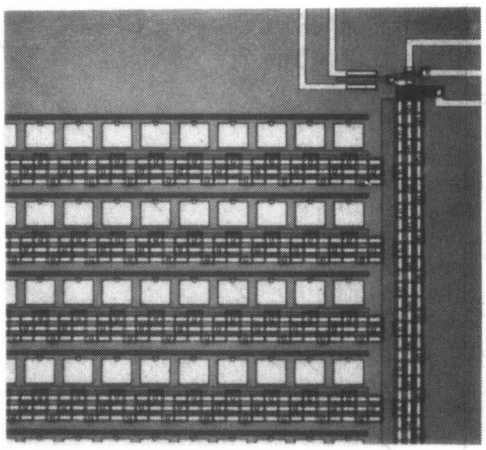



Figure 6 Cross sectional view of pixel 128x64 element PtSi IR-CCD sensor with optical cavity



(a)



(b)

Figure 7 Microphotographs of 128x64 element PtSi IR-CCD sensor, (a) complete view and (b) cut out of top right part with source follower output structure

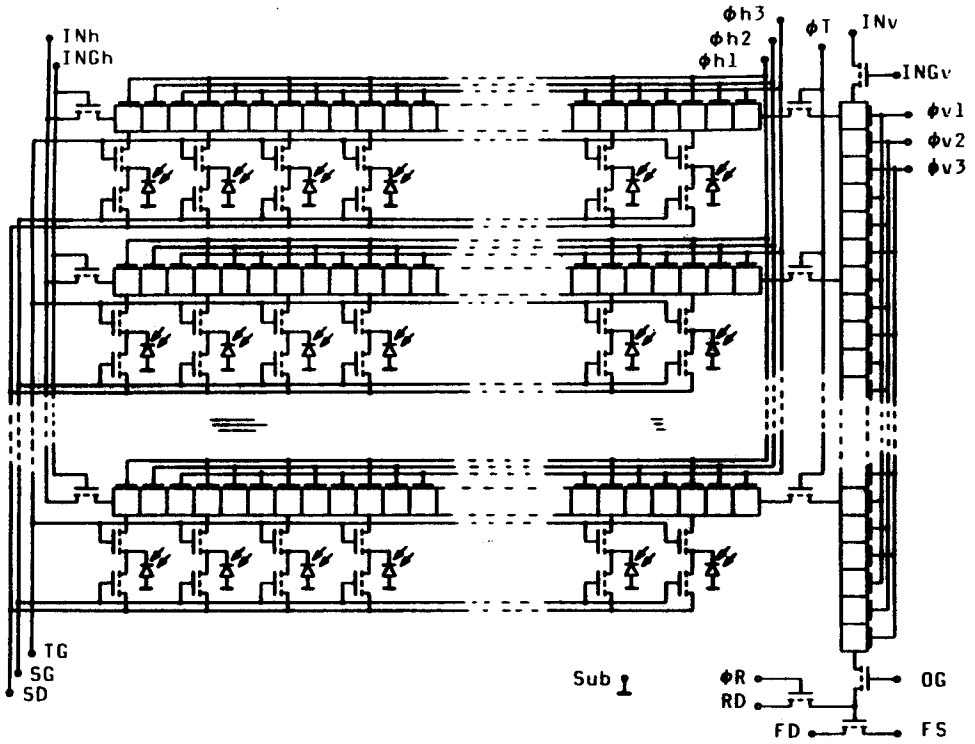



Figure 8 Schematic electric diagram of 128 x 64 element PtSi IR-CCD sensor

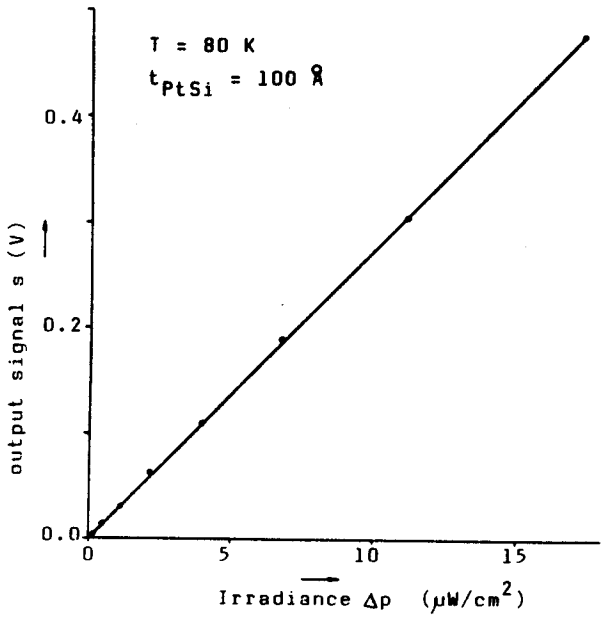



Figure 9 Output signal s versus irradiance Δp for one pixel of 128 element PtSi IR-CCD line sensor

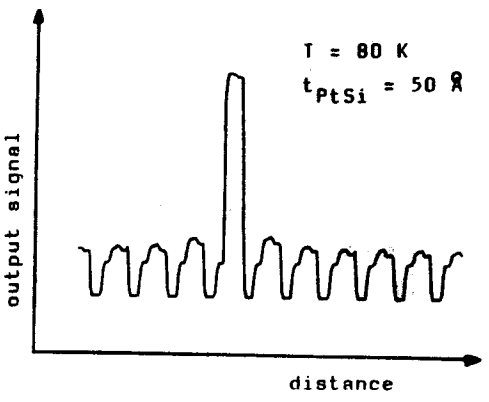



Figure 10 Crosstalk of 128 element PtSi IR-CCD line sensor irradiated with focussed HeNe laser beam( λ = 3,39 μm beam spot size: 25 μm )

# THERMAL IMAGING USING INDIUM DOPED SILICON

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## INTRODUCTION

The requirements for future thermal imagers compared with actual systems are higher spatial and thermal resolution. Nearly all materials for infrared applications in the 3-5 µm or 8-12 µm wavelength range have reached the physical limits concerning sensitivity. Therefore the only possibility to reach a better performance is to increase the number of picture elements, to reduce the size of picture elements and to increase the fill factor. Although materials like InSb or CMT offer superior detector performance at higher operating temperatures, at present silicon has the advantage in the realisation of the final device structures, because of its well developed technology. Today silicon is the only material to develop monolithic integrated infrared devices with very high numbers of picture elements.

## MATERIAL

The intrinsic silicon itself is only sensitive to photons of wavelength less than about 1 µm. So it is not suitable for thermal imaging, especially not in the required wavelength ranges 3-5 µm and 8-12 µm corresponding with the atmospheric windows.

However it is possible to introduce centres into the silicon that produce energy levels in the silicon band gap that make it sensitive to infrared wavelengths of interest. Several impurities for this purpose are explored, a survey is given by Sclar (1). In consideration of the applicability the element indium was chosen. Indium in Silicon acts as a simple acceptor lying about 0,155 eV from the valence band edge. With a peak sensitivity at 5,0 µm and a cut off wavelength of 7,4 µm indium doped silicon is well suited for the 3-5 µm band.

In the indium doped silicon there are always some shallower impurities like B, Al or X-level, an indium carbon complex. These shallower impurities require lower operating temperatures if the device shall remain background limited, unless they are compensated out. Compensation is achieved by adding a shallow donor, like P, to fill the shallower acceptor levels with electrons in order that their occupation does not change with temperature. Since the concentrations of the unwanted impurities can be made very low (about $2 \times 10^{13}/cm^3$) traditional doping methods, such as doping from the melt, are not suitable for compensation. The use of neutron transmutation doping (NTD) with thermal neutrons in a nuclear reactor gives a very exact and homogeneous compensation. Figure 1 shows the photocurrent as a function of temperature for compensated indium doped silicon. Below 50 K the material is background limited, that means the thermal generation rate of carriers is lower than the optical generation rate.

The responsivity of the material is proportional to the indium concentration devided by the phosphorus excess concentration. The noise current, if only background limited performance is considered, is proportional to the square root of the indium concentration divided by the phosphorous excess concentration. This leads to a detectivity D*, that is only proportional to the square root of the indium concentration and therefore independent of the compensation concentration. That means, that it is possible to reduce the responsivity without decreasing the detectivity. This fact is very important for applications in CCD infrared imagers, because the responsivity can be tailored to give suitable sized charge packets in a given integration time without affecting the detectivity. In conclusion indium doped silicon is well suited to develop monolithic integrated circuits for infrared applications.

## FORMATS OF FOCAL PLANE ARRAYS

In a monolithic infrared device detectors, transfer structures and read out structures have to be integrated on the same chip. Some of the requirements for such devices are high fill factor, low optical crosstalk, capability for antiblooming and substraction of carriers generated by background radiation. Since these parameters depend on the format of the focal plane array mainly some possible design features are discussed.

An interline transfer (ILT) design with the division between detectors and transporting CCD is very space consuming. As well a frame transfer (FT) design as a line transfer (LT) design do not require additional space for the detectors because they are part of the transporting CCD. For both structures all phases of the CCD have to be of sizes matched to the generated charge packets. The narrow transport lines of a resistive gate sensor (RGS) beside the detectors give the best fill factor among the mentioned formats.

To avoid additional gates and drains for antiblooming and storage punch-through detectors have been used.

### Punch-Through Detector (2)

On the p-type indium doped silicon an n-type epitaxial layer is grown (Fig.2). The picture element is defined by a gate that is separated by a thin oxide layer from the epitaxial layer. The voltage at this gate must be chosen in a way, that the epitaxial layer is fully depleted and the p-n junction is forward biased to achieve punch through to the substrate. Increasing the voltage leads to a drop across the substrate which supports the flow of photogenerated holes. The photogenerated holes are collected under the gate at the $Si/SiO_2$ interface. Under punch through

conditions the holes are never in contact with electrons and no recombination takes place. As charge accumulates in the potential well the voltage across the oxide increases, causing the voltage across the p-n junction and the substrate to decrease or even to fade. Thereby the device is selflimiting and an automatic inherent antiblooming is given. Once a well is filled charge collection terminates and there is no excess charge to be split into adjacent wells.

Besides this feature, the punch-through detector needs no additional storage gate. Only a transfer gate is needed to connect punch-through detectors to adjacent transport structures.

For this type of detector used in a focal plane array the incident flux must pass through several layers (e.g. doped polysilicon gate, oxide, nitride) of the device. Photons can be absorbed by free carrier absorption and interferences can occur (3). By a proper choice of doping concentrations and thicknesses of the layers these effects can be reduced.

Resistive Gate Transfer (4)

Charge carriers can be conducted in a channel under a resistive gate. The resistive gate is a long and narrow high ohmic structure, made of polysilicon, which is separated by a thin oxide layer from the underlying n-type epitaxial layer. In order to take advantage of a buried channel, a thin layer of the opposite conductivity type is introduced under the $Si/SiO_2$ interface (Fig. 2).

Across the resistive gate only a DC voltage has to be applied to form a potential gradient in the channel under the gate. The injected carriers will follow this gradient. The velocity of the carriers depends on the field strength along the channel only. The resistive gate transfer time is proportional to the square of the gate length divided by the voltage across the gate.

Charge packets injected under a resistive gate diverge because of the repulsive Coulomb forces. Therefore it is necessary to collect the charge at the end of the resistive gates again. Groups of three gates, can be used for this purpose, as shown in figure 3. Adding single gates towards drains on the other side of the CCD permits to perform background substraction outside the detection area. Also remaining carriers from the resistive gate channels can be removed before injection of the next charge packet.

## FOCAL PLANE ARRAY WITH 64x64 PICTURE ELEMENTS

For the realized staring array with 64x64 picture elements the resistive gate format has been used to achieve a high fill factor. This format, shown in figure 4, consists of the punch-through mode picture elements, transfer gates, long vertical resistive gates, groups of three gates and a horizontal CCD with an output amplifier, an additional line of gates along the CCD and a line selector.

All 64 resistive gates are connected parallel, so only two connections are required. After the resistive gate transport the charge carriers are collected again using the groups of three gates. For performing a background substraction, also known as skimming, an adjustable part of the charge packets can be retained under the buffer gates. The significant parts of the charge packets are injected into the horizontal four phase CCD and shifted to the output. After the CCD transport of a complete line the retained charges can be forced by the skimming gates towards the drains.

The line selector is a digital shift register with analog output circuitry. It drives the punch-through gates and the transfer gates adjacent to the picture elements line after line to make shure that only one charge packet is under each resistive gate at the time.

The CCD requirements are: low noise, high transfer efficiency, high speed operation and the ability to function at the low focal plane temperatures. In the case of the 64x64 array a four phase buried channel CCD is used. Transfer inefficiencies of about $10^{-5}$ per transfer are achieved down to 50 K. At lower temperatures of about 30 K an increase of the transfer inefficiency due to freeze out effects has been noted.

The most significant data of the array are given in table 1. Indium doped silicon is well suited to make monolithic focal plane array for infrared applications in the 3 - 5 µm wavelength range.

TABLE 1 - Significant data of focal plane array on indium doped silicon.

| | |
|---|---|
| Mode of Operation | Photoconductive |
| Number of Picture Elements | 64 x 64 |
| Size of Picture Elements | 55 µm x 65 µm |
| Pitch | 85 µm |
| Fill Factor | 50 % |
| Read Out Design | Resistive Gate Transfer |
| Chip Size | 56 $mm^2$ |
| Detectivity | $2 \times 10^{11}$ cm $W^{-1}$ $sec^{-1/2}$ |
| Wavelengths | 3 µm - 5 µm |
| Operating Temperature | 50 K |
| Number of Connections | 24 |

## OUTPUT SIGNAL RECOVERY

The horizontal CCD ends in an on-chip charge detection circuit, briefly mentioned above as output amplifier. This circuit, as shown in figure 5, consists of an output gate (OG) after the last CCD phase and a diode for charge extraction from the CCD. This diode is connected to the source of a MOS transistor (TR) for reset purposes and to the gate of a second MOS transistor (TF), normally operated in the source follower mode with an external resistor load. The output gate is DC biased for decoupling the charge from the CCD pulses.

In figure 5 a section of the pulse timing diagram relevant for this circuit is given.

Prior to the charge output from the CCD a reset pulse is applied to the gate ($\phi$R) of the reset transistor in order to charge the node capacitance (CF) to the potential of the reset drain (RD). This potential turns the second transistor (TF) on and the output voltage rises towards $V_{FD}$, as shown in figure 6. After the reset pulse a feedthrough of the reset voltage takes place and forms the reference level at the output. Then charge is transferred from the CCD into the node capacitance and partially discharges it. This potential change causes the conductance of the output transistor to decrease and the output voltage changes proportionally.

The significant output signal has to be recovered from the difference between the charge detection level and the reference level. A circuitry for this purpose is given in figure 6. A sample-hold device holds the reference level to be substracted from the latter charge detection level. The resulting waveform is relieved from the reset transitions by a second sample-hold device and thereafter can be used as a video signal for display or further conversion. This procedure, known as correlated double sampling, will also reduce noise picked up at the DC connections to the output circuit.

## NONUNIFORMITY CORRECTION METHODS

Although, as has been shown, the inhomogeneities of the responsivity and detectivity are low and although it is expected to reduce them by a factor five they lead to a fixed pattern noise in the picture that is too high to achieve the required resolution of future thermal imagers. These nonuniformities act as offset and gain variations. Therefore they have to be compensated by an electronic signal processing circuitry performing a two point correction.

With the detector viewing a uniform reference temperature T1 the offset variations can perfectly be compensated at temperature T1 with a simple pixel by pixel substraction. With this single point correction, as shown in figure 7, the compensation will generally not be complete over the entire focal plane dynamic range. To achieve this, measurements with the detector viewing a second uniform reference temperature T2 have to be done. Therewith the relation between incoming flux and output voltage can be computed for each picture element. The operations to be performed on each pixel are a substraction and a multiplication. To use this compensation approach the relation between incoming flux and output voltage of the focal plane array must be linear within the desired compensation accuracy. For punch through devices on indium doped silicon such a linear approximation is valid over a wide dynamic range.

## THERMAL IMAGER WITH OFFSET CORRECTION

For the use with the realized focal plane array with 64x64 picture elements, an experimental camera set-up was built. The required cooling to 50 K is provided by a laboratory cryostat, but also a portable cooling engine is announced to be available. The lens system has a focal length of 200 mm and an f-number of 1.5.

The camera, whereof a block diagram is given in figure 8, consists of the pulse generator, circuitry for signal recovery and correction and an interface belonging to a display. The signal recovery is done by correlated double sampling, as mentioned above, followed by analog to digital conversion. For nonuniformity compensation only a digital offset correction is built into the set-up, consisting of an arithmetic unit and a memory for the reference frame. This first step furnishes with a lot of experience and performs satisfactory imaging.

Figure 9, a photo taken from the display shows the good thermal resolution of the focal plane array.

## CONCLUSION

Compensated indium doped silicon is well suited to develop monolithic integrated focal plane arrays. Because of the well developed silicon technology arrays with more than $10^5$ picture elements are possible. The remaining nonuniformities are easy to correct within the required accuracies. These devices will meet the requirements of future thermal imagers.

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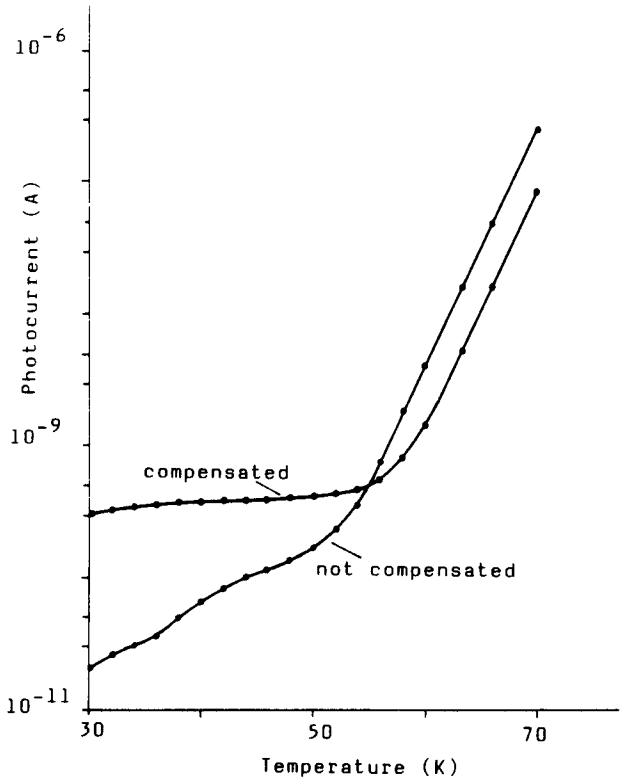


Figure 1 Photocurrent versa temperature for detectors on indium doped silicon

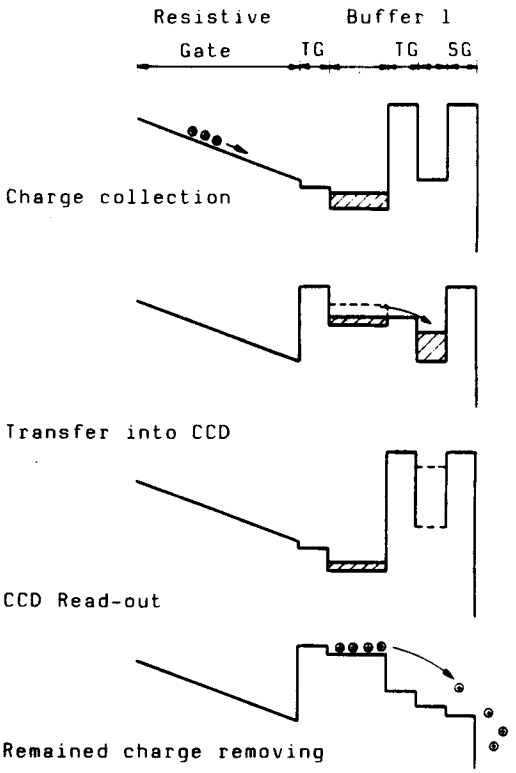


Figure 3 Schematic drawing of resistive gate transport with skimming

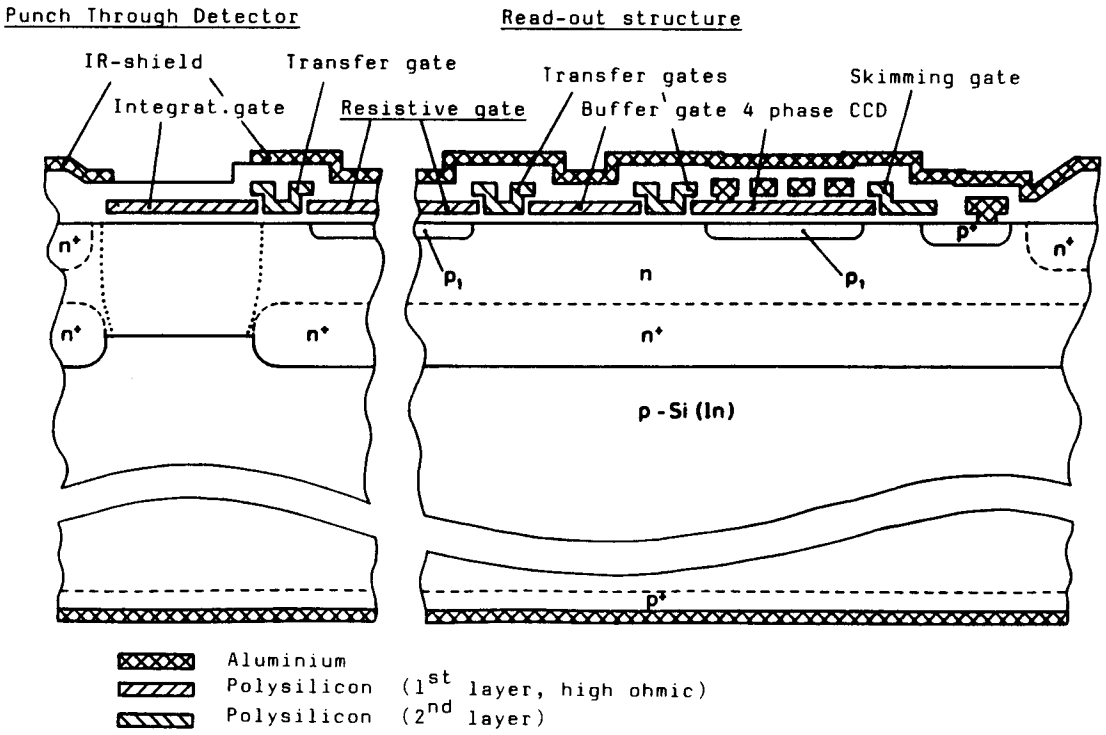


Figure 2 Cross section of resistive gate sensor with punch through detectors